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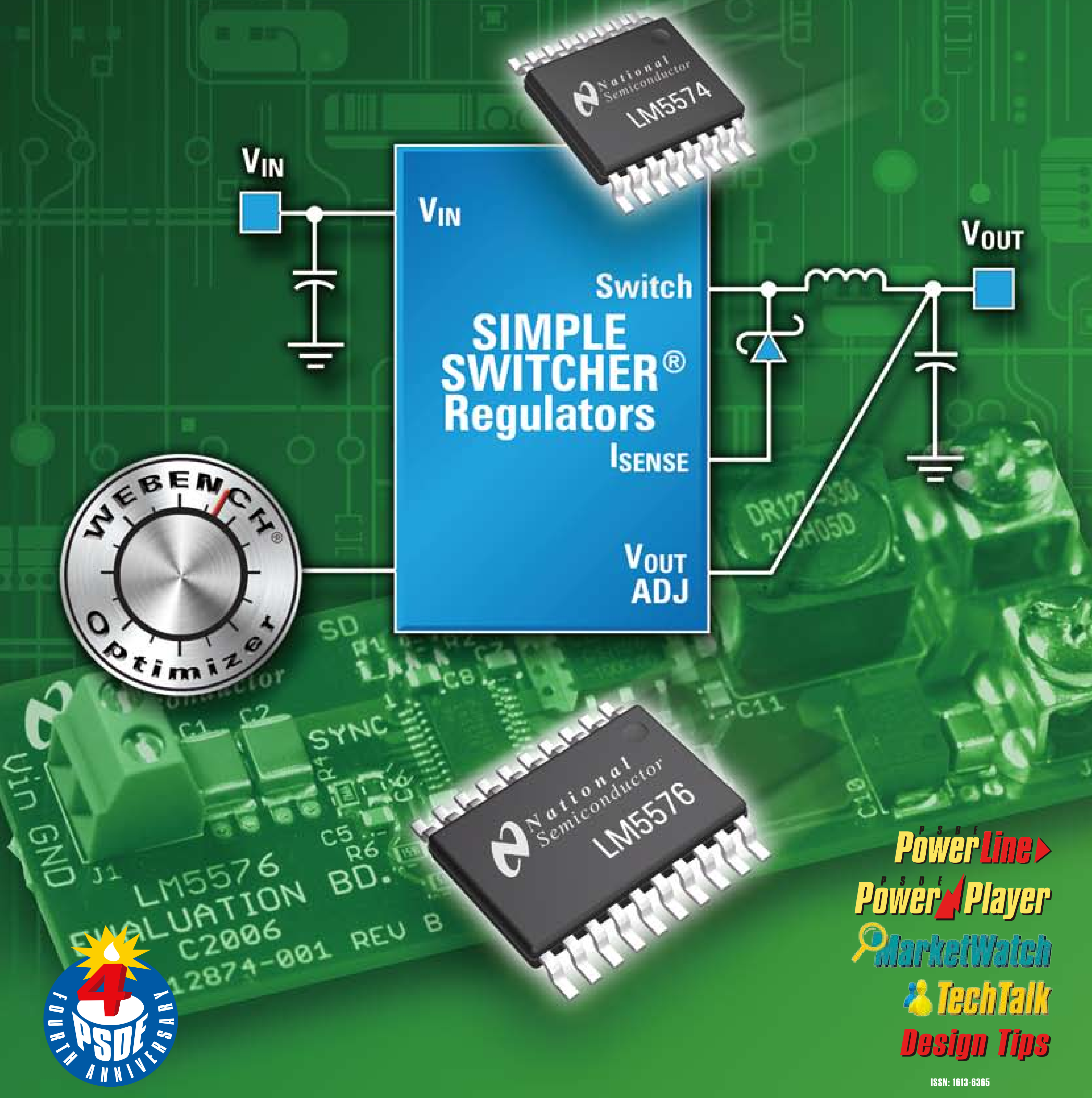
EUROPE

Empowering European Innovation

January/February 2007



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Volume 4, Issue 1

Welcome to the future...

We start the year with a birthday! It is the 4th anniversary year of PSDE which started off life after the closure of the PCIM Europe magazine, familiar to many of us as a source of info as to what was going on in the power industry in those times. Much has happened since then and I would never have guessed I would be editing the offspring of this popular and respected industry magazine today.

But, moving on, I was surprised and pleased to see the high level of activity last year carrying through right to the end of the year. No 'holiday slow-down' the information from our industry just kept on coming. As editor, I was receiving news and calls right up to the traditional closure. Great business and great products and technology are as strong as ever.

We, I have found, in the power industry have not lost our sense of humour. Much of my in-mail is based on anecdotes from engineers and leaders alike. It's heart-warming to know that no matter the challenges and outright pressure applied to our daily work-lives, the people in the industry take it all in good heart and deal with it in a way that puts it into perspective.

The leaders in our industry, often not born as such, bear a great responsibility for our industry. We have already been catapulted directly into the face of a world that demands better efficiency, smaller board occupancy and fast delivery to market. In this world only the rare individuals who stay in our memories like the best teachers, lecturers and professors in our college days will motivate us to the degree where we achieve great things because we are inspired to. Hopefully, top ranking leaders see it in time to get the very best out of the talent we are fortunate to have here in the power design engineering community.

I must mention the cover story in this issue from National. I just came back from the official press conference here in Munich where Mal Humphrey, product line Director for National's high-voltage power products, gave us the rationale behind the next-generation 'simple switcher' regulator family. It really is a piece of wizardry, when you look at the silicon available and the tools that wrap it into a real product, one appreciates the fact that someone has understood the real needs of the designer. It's a bit like getting an instruction manual that really works in your own language. I tried to bust it on their 'WEBENCH' internet design tool but it kept giving me a successful design!

The CES in Las Vegas has again re-instated itself as the pearl within the consumer oyster. Although out of our geographic area, with many reports coming in just now, there is a predictably healthy interest in the power and power management industry's contribution. With press info too vast to cover in the depth I would like, it shows clearly that our industry is not just on the periphery, but central to the 'must have' portable devices developed and marketed such as the much publicized iPhone from Apple.

Las Vegas saw the launch of the Apple iPhone and I received an interesting report from iSuppli. This is an excerpt…

"For Apple, such a strong hardware profit is par for the course, with the company having achieved margins of 45 percent and more in products including the iMac and iPod nano, according to iSuppli. However, because Apple is facing extensive competition in the music-phone market, the company may need to cut into its margins to reduce pricing in the future. "With a 50 percent gross margin, Apple is setting itself up for aggressive price declines going forward," said Jagdish Rebello, PhD, director and principal analyst with iSuppli."

Interesting stuff for us Apple followers.

So, back to the issue in hand, I hope you enjoy the content this time round. There was more actual news than I could cover and I hope we can catch-up in the forthcoming issues. In the meantime, please keep your valuable suggestions, comments and news stories coming and I'll try to do them justice. Have a great 2007!

Cliff Keys

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Maxwell Technologies Receives Largest-Ever 3 Million-Unit "D Cell" Ultracapacitor Order

Maxwell Technologies Inc. announces that a leading European producer of wind energy systems has placed a purchase order for 3 million BOOSTCAP® BCAP0350 E "D cell" ultracapacitors to provide backup power for wind turbine blade pitch systems.

Alain Riedo, senior vice president and general manager of Maxwell's Swiss subsidiary, Maxwell Technologies SA, noted that the order, which is expected to be drawn down over two years, is for double the quantity of the company's previous largest D cell order, a 1.5 million-cell order for a wind energy application in February 2006.

The ultracapacitors are used for backup energy storage and power delivery in wind turbines ranging in output up to 2.5 MW. Each of the turbines' three blades has an independent braking and pitch adjustment mechanism incorporating a bank of from 200 to 700 BOOSTCAP cells for backup power to ensure continuous operation in the event of a power failure.

"Strong global demand for wind energy systems is driving increased demand for ultracapacitors, and we are pleased that one of the world's largest and most innovative wind turbine producers has selected our BOOSTCAP products to enhance the performance and reliability of their systems. Ultracapacitors' high reliability, robustness and long operating lifetime have now been proven in daily operation over the last three years in wind farms around the world" Riedo said.

www.maxwell.com

Microsemi Opens Taiwan Design Center

Microsemi

Microsemi has opened a new design center in Taiwan to provide closer technical support in Asia, the site of its highest-growth customer base.

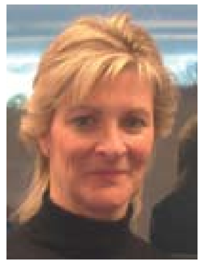
The new Taipei facility will house Microsemi application and system engineering staff, customer service, and Asia sales management.

Opening of the new design center reflects the continuing growth of Microsemi's analog mixed signal products throughout Asia. These product lines include backlighting, wireless LAN power amplifiers, and DC-DC integrated circuit products which have shown increased penetration into a variety of end markets including notebook computer and LCD TV markets. The new design center includes a systems engineering lab in support of these applications.

"We have a strong commitment to our customers in Asia that justifies this significant investment in facilities and personnel," said James J. Peterson, Microsemi President and CEO. "Our aggressive plan for the region also includes more than doubling the number of Microsemi field application engineers in Asia," he added.

www.microsemi.com

Rutonik and Infineon Expand their Distribution Agreement



In 2007 Rutronic extends its activities to UK, Ireland, Spain and Portugal and South Africa. With this agreement, both companies are strengthening their long-term partnership, already covering Germany, Switzerland, Italy, France, the Benelux states and Eastern Europe. RUTRONIK now serves Europe's four largest distribution markets (Germany, UK, Italy and France) with Infineon products, thus taking an important step in the pan-European harmonisation of its line-card. Jezel Hardern, Country Manager UK & Ireland, commented: "Naturally, we want to incorporate our competence as a systems and solutions provider, not just our product spectrum. Customers from the automotive industry especially want complete packages. Thanks to our balanced line-card, we are capable of providing our customers with objective consultancy and a complete spectrum of components for their applications."

www.rutronik.com

www.Infineon.com

TTI Achieves More than Double Industry Growth

TTI Europe is on target to achieve year-on-year growth figures which are more than double that predicted for the industry. The company is moving up the top 10 largest European distributor rankings.

"This year, the distribution industry is experiencing solid growth of around 15%", details Glyn Dennehy, TTI's VP Europe. "We are on track to grow by 35% in revenue terms this year. What's more, if we look at our performance over the last three years, we will have achieved a CAGR of 28.9% in a market (passives and emech) where the European TAM has only grown by around 3%. In other words we are rapidly gaining market share. If you just look at passive components, TTI is Europe's second largest distributor."

The relationship TTI has with its suppliers is represented by the number of awards the company has received this year. Murata, FCI, Kemet, Bourns, Harwin, Amphenol and Phoenix Contact have all named TTI Europe in a roll call of honours.

Notable investments in 2006 included a $1M Warehouse Control, System at TTI Europe's headquarters in Maisach-Gernlinden, Germany with benefits of improved productivity and efficiency.

www.ttieurope.com

UR Group Appoints New Area Sales Manager for Northern England

UR Group has appointed Peter Melling as Area Sales Manager for northern England. Peter, who lives in Lancashire, UK, joins the company from Acal plc and has 20 years' experience in electronics sales, with 10 years specialising in the power sector.

"I'm delighted to have joined UR Group," said Peter. "The company is really going places, with a great line-up of prestigious franchises in power, semiconductors and fibre-optics. UR also offers considerable design-in expertise to customers in a wide range of industries."

www.ur-group.co.uk

PSMA Releases 2006 Technology Roadmap Workshop Report

The Power Sources Manufacturers Association (PSMA) has announced the release of its Power Technology Roadmap Workshop Report. This Fifth Edition provides detail of the individual presentations and group discussions that took place prior to the Applied Power Electronics Conference 2006 organized by Bob White (Artesyn Technologies/ Emerson Network Power) and Chuck Mullett (ON Semiconductor) to project technology trends in power supplies.

The report gives projections for the next 3-5 years in key technologies with special emphasis on Digital Power Control.

The technology trend analysis and roadmap covers:

- AC-DC front end power supplies – 1 kW from a single phase AC source
- External AC-DC power supplies
- DC-DC bus converters
- Non-isolated DC-DC converters

For each of these product categories, parametric trend analysis is provided for:

- General product requirement: Power density, $/watt, delivery time
- Circuit design and implementation: PFC, DC-DC
- Component technology: PFC, DC-DC
- Packaging, physical design, thermal management and assembly technology.

www.PSMA.com

Anderson Power Products® Announces Enhanced Web Site

Anderson Power Products (APP), has announced the launch of their new website, www.andersonpower.com. Incorporating several enhanced features, the new look and functionality of the web site will better serve APP's global customer base and further highlight all available product offerings. A tremendous global presence for power interconnect solutions, APP is now able to provide consistent quality and delivery for all manufacturers and sub-contractors around the world.

APP's new web site provides easy access to all the information necessary for its customers to successfully engineer power interconnect products into their designs. The site will provide visitors with enhanced access to detailed information about APP, making it easy for visitors to obtain a number of features at all hours of the day or night, including the ability to search for RoHS products, download product information and specifications, access technical information, view temperature charts, create, modify and view line drawings, review tooling information, reference assembly instructions, and identify sales contacts and distributor information. In addition, the new site offers an Online Store for purchasing APP products and several additional features.

In 2007, APP will also feature multiple versions of the site translated in to several different languages, which will further extend APP's customer service.

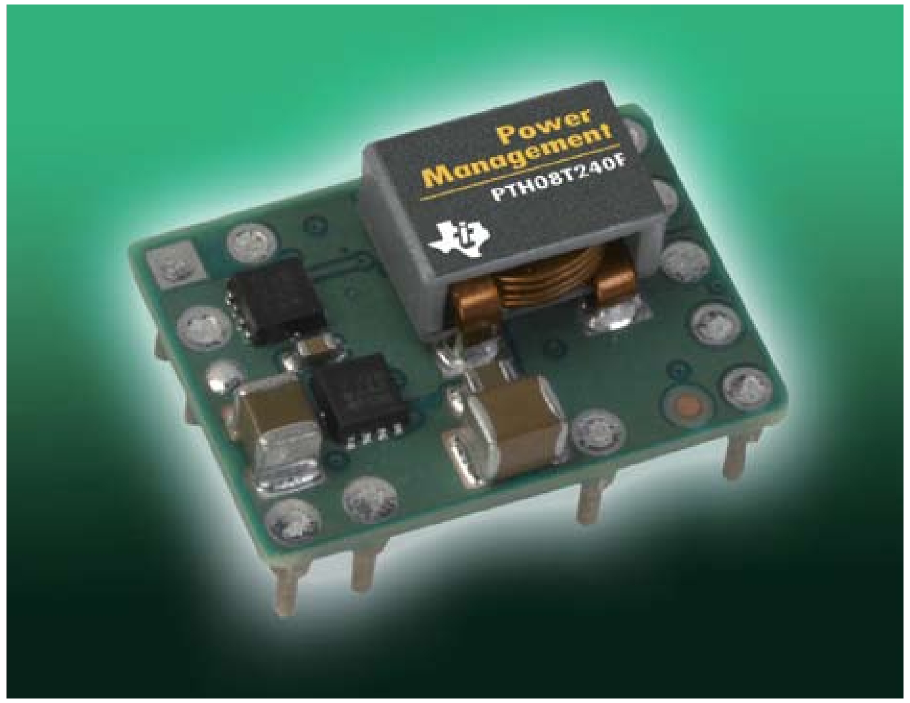
www.andersonpower.com

Power Events

- ***APEC 2007,*** *Feb 25 - March 1, Anaheim, California, USA, www.apec-conf.org <http://www.apec-conf.org/>*
- ***PCIM China 2007,*** *March 21-23, Shanghai, China www.pcimchina.com <http://www.pcimchina.com/>*
- ***electronicaChina 2007,*** *March 21-23, Shanghai, China http://www.global-electronics.net/?id=21317*
- ***PCIM Europe 2007,*** *May 22-24, <http://en.wikipedia.org/wiki/N%C3%BCrnber g_%28disambiguation%29> Nürnberg, Germany http://www.mesago.de/en/PCIM/main.htm*
- ***The China International Power Supply Show (CPS EXPO),*** *June 13-15, Shenzhen, China <http://expo.dianyuan.com/>*

Fast Transient Response DC/DC Power Module for 3-GHz DSP & High Performance POL Systems

Texas Instruments has launched a 10-A, non-isolated DC/DC power module with fast transient response and high performance. The plug-in module meets the strict three percent accuracy core voltage tolerance requirements of their newest 3-GHz digital signal processors (DSPs), such as the TMS320TCI6487, with only 3,000 µF external output capacitance. The device supports point-of-load systems that use high-performance DSPs, Microprocessors, ASICs and FPGAs.



Based on TI's extensive T2 family of devices, the new PTH08T240F incorporates TurboTrans™ technology, which optimizes the power module's transient response and reduces the amount of output capacitance by up to eight times. The technology significantly reduces the peak output voltage deviation under transient load conditions, while saving the customer the cost and board space for additional capacitors.

The PTH08T240F has a wide input voltage range of 4.5 V to 14 V, and provides up to 92 percent power efficiency at 1.8-V output. The module's output voltage is adjustable from 0.7 V to 2 V, and features over-current protection and programmable under-voltage lockout. In addition, the module offers over-temperature protection, on/off inhibit control, differential remote sense and 1.5 percent DC output regulation.

This module is the first power management device that meets the core voltage tolerance requirements of TI's new TCI6487 DSP. As an example, this single chip, multi-core, 3-GHz DSP requires a core voltage rail between 0.9 V and 1.1 V with a source impedance of 2 milliohms. The TCI6487's voltage tolerance requirement for transient loads of up to 5 A is only 15 mV. The PTH08T240F easily supports this with only 3,000 µF external output capacitance. This achievement allows wireless infrastructure base station OEMs using the new DSP to simplify their power system designs, while achieving optimal power performance and efficiency.

SmartSync, another element of this module, allows for switching frequency synchronization of multiple modules, thereby simplifying electromagnetic interference (EMI) noise suppression tasks and reducing input capacitor ripple current requirements. The PTH08T240F also includes the Auto-Track™ sequencing feature, which simplifies simultaneous power-up and power-down of multiple power modules in the system.

The PTH08T240F is sampling now and is scheduled to be available in volume production early this year from TI and its authorized distributors. The module comes in surface-mount and through-hole packages.

power.ti.com

The Challenge of Powering Deep Sub-Micron CMOS Loads

By Paul Greenland, Vice President Marketing, Enpirion

All engineers are familiar with Moore's Law, the empirical observation that the number of transistors on an integrated circuit for minimum component cost doubles every 24 months, attributed to Gordon E. Moore a co-founder of Intel. It implies, from the power management perspective, decreased supply voltage and until recently, increased dI/dt. Moore's Law applies to digital circuits, particularly CMOS; unfortunately there is no equivalent rule that applies to analog. As CMOS feature size decreases the quality of the devices available for use in analog peripherals is restricted. Smaller devices have non-ideal VI characteristics, increased gate leakage and inherently higher 1/f noise. These characteristics degrade matching and gain which in turn reduce common-mode and power supply ripple rejection. These effects are compounded by the CMOS Designer's use of single-ended rather than differential circuits to conserve die area. Sub-90 nm CMOS ICs with analog peripherals such as Phase-Locked Loops (PLL), commonly used for clock synthesis and recovery, are particularly susceptible to supply noise and ripple, glitches and substrate noise. This poor Signal to Noise Ratio (SNR) can be seen in the familiar Eye Diagram, a tool used for the qualitative analysis of a digital transmission signal. The eye diagram provides a first order approximation of signal to noise ratio, clock timing jitter and skew. Another issue at smaller geometries is the density of metal interconnect. This tight coupling increases inter-device capacitance providing a sneak-path for high frequency noise and cross talk. Common resistance effects such as ground bounce and line drops are also more significant as supply voltages and gate thresholds fall, to the extent that sub circuits cannot communicate reliably across the full width of the die without exploiting differential techniques.

Fortunately the solution to many of these issues lies in providing a clean power supply. A particular case is one of the new digital Set-Top-Box ICs which latches up if the core supply has more than 20 mV_{p-p} ripple and noise. The obvious solution is to filter the conventional switching regulator feeding it, which is costly, reduces bandwidth and changes output impedance characteristics. Unfortunately when the firmware is changed, effectively working the core harder, the noise increases further still, requiring a large margin on noise attenuation to future-proof the design. A better solution is to "tune" the power supply to its load, matching noise, ripple, transient response and output impedance characteristics. This is achieved by switching at higher frequency, which increases control loop bandwidth and constraining noisy switching currents to the smallest loop possible by integrating the filter inductor. Enpirion point-of-load solutions switch at 5 MHz; control loop unity gain bandwidth is 500 kHz, giving lightning-fast transient response and low output impedance for switching loads. Many system designers are at the transition stage, changing from LDOs to switching regulators to raise efficiency. Integrated inductor solutions make the design process as simple as using an LDO.

The multi-layer ceramic filter capacitors are virtually the same for a high performance LDO; developing an efficient Enpirion solution is just a matter of eliminating the heat-sink. Many new designs are space-constrained, so the simplicity of the solution has to be complemented by smaller footprint and profile, a true point-of-load regulator has to be practically on the supply terminals of the load IC with minimal interconnect parasitics. Some IC manufacturers even recommend independent pi-filters on all supply, control and some I/O pins of their IC for reliable operation. If the filters are un-damped, particularly if the inductor is not lossy at harmonics of the load switching frequency, this may actually make the situation worse.

In summary powering deep submicron CMOS loads is a complex issue, where an appreciation of the challenge facing the analog peripheral designer is a real advantage. Now, more than ever, the power management solution is enabling the technology. Final customers for these devices pay for signal to noise ratio and Bit Error Rate (BER) as they have a vested interest in the performance of the end equipment. Enpirion point-of-load solutions are the right product at the right time, making possible the promise of increased bandwidth, content and functionality that smaller process geometry brings.

www.enpirion.com

Rise of Portable Devices a Powerful Concern

Battery life becomes a huge issue for consumers

By Marijana Vukicevic, iSuppli Corporation

Portable electronic devices, a huge part of our everyday lives, with most consumers toting at least one mobile phone and usually at least one other device. When adding notebook computers—which will represent 40 percent of total PC unit shipments by 2010, iSuppli Corp. predicts—this becomes a vast number of portable products. Because of this, several types of portable devices, including notebooks, mobile phones, MP3 players and Personal Digital Assistants (PDAs), have become significant drivers of the power-management market.

What distinguishes portable devices from other electronic products is that their power is supplied from a limited source: the battery. In such devices, battery life is a major concern for consumers.

This problem can be handled in three different ways: software, firmware and hardware, with a combination of all three approaches employed in order to ensure successful power management.

From the software side, Microsoft Corp.'s new Windows Vista operating system is one of the newest tools for managing power more efficiently.

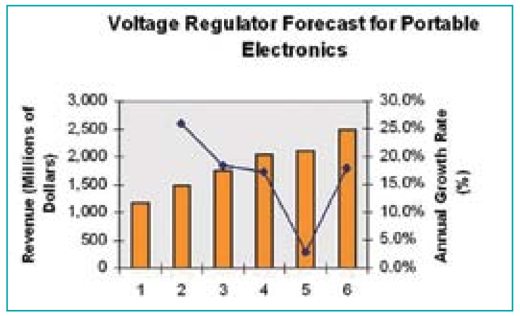


Figure 1 presents iSuppli's five-year forecast for voltage regulators in portable devices.

Microsoft's previous operating system, Windows XP, was a big improvement over Windows NT in terms of power management, but Vista is steps beyond.

In portable devices such as mobile phones, there is a trend toward adding software performance analyzers that conserve power by optimizing code so that it takes less time to execute a given task. These analyzers are unique to specific operating systems and hardware.

However, software-driven improvements in power efficiency are meaningless unless they are accompanied by intelligent hardware designs. Such designs are cooperative and responsive to the software's commands to adjust the frequency or voltage—processes called voltage scaling and frequency scaling. These factors can be adjusted to save precious battery life with communication achieved via a variety of protocols, most commonly the Inter-Integrated Circuit (I2C) and Power Management Bus (PMBus) standard.

Improvements now

One trend among mobile-phone manufacturers is the integration of power-management functions into the analog baseband circuitry. Leading suppliers in this arena are Freescale Semiconductor Inc., Qualcomm Inc. and Texas Instruments Inc., with more companies are expected to announce similar offerings later.

Notebook PCs have power-savings features implemented at all levels of their hardware. Microprocessor technology advancements are helping to save more energy. Advanced Micro Device Inc.'s PowerNow technology can throttle down the microprocessor to only 25 percent of its full potential, delivering power consumption savings. Meanwhile, Intel Corp.'s Centrino Duo platform operates with 28 percent less energy compared to the previous Centrino platform.

The key ICs in power management are voltage regulators. Because of this, the market is expected to grow at a rate of 16 percent during a five year period.

While there is plenty of work to be done to ease consumer concerns about battery life, companies are taking steps to make further strides in the future.

Marijana Vukicevic is senior analyst for power management at iSuppli Corp. Contact her at mvukicevic@isuppli.com For more on power management, see Vukicevic's latest report: Turbulence on Horizon Among Power MOSFET Suppliers. For more see http://www.isuppli.com/catalog/detail.asp?id=7832

www.iSuppli.com

High Frequency Power Transformer Measurement and Modeling

This article points out some of the issues involved in designing, measuring, and modeling high-frequency magnetics for switching power supplies.

Despite efforts from some magnetics vendors to provide off-the-shelf components to power supply designers, almost all high-performance magnetics are custom. There are many deep and complex issues involved in the design of magnetics. I will try to cast some light on just a few of these issues.

By Dr. Ray Ridley, Ridley Engineering

Transformer Design Example

Figure 1 shows a simple 1:1 transformer. The transformer uses an ungapped EPC-25 core from TDK, made from PC-44 material. This transformer was designed for use in a 60 W forward converter with 36-60 V input and 12 V output.

Figure 2 shows the winding layout, with just a single layer of 18 turns for the primary winding, a layer of thin insulation tape, and a single layer of 18 turns for the secondary winding.

This is a very straightforward, easy-to-manufacture design of a two-winding transformer. However, as you will see below, the resulting circuit element created is anything but simple.

Transformer Model

Figure 3 shows a commonly-used model for a two-winding transformer. On the primary side, the winding resistance is represented by R_p, the leakage inductance by L_{lk}, magnetizing inductance by L_m, core loss by R_c, and self-capacitance by C_p.

The secondary winding resistance is R_s, the secondary self-capacitance is C_s, and the primary to secondary capacitance is C_m.

The elements of this transformer model are used for several purposes-characterizing components, identifying problem design areas, and circuit simulation. However, this apparently simple model is complicated by the fact that all of the resistors and inductors of the model are nonlinear functions of either frequency, or excitation level, or both. The capacitors can also exhibit minor nonlinearities, but are further complicated by the fact that the lumped elements shown in Fig. 3 are a very crude approximation to the true multiple interwinding capacitance effects that really exist in the component.

Transformer Frequency Response Measurements

It is very useful to make frequency response measurements on a high-frequency power transformer, using a wide range of frequencies. For a two-winding transformer such as the example above, the most common measurements are impedance measurements from the primary side, with the secondary both open-circuited, and short-circuited.

Fig. 4 shows a typical test setup for impedance measurements, using the AP200 frequency response analyzer. More detail of this test can be found in [1]. While many manufacturers only

Figure 1: A simple 1:1 transformer designed for a 100 kHz, 60 W forward converter.

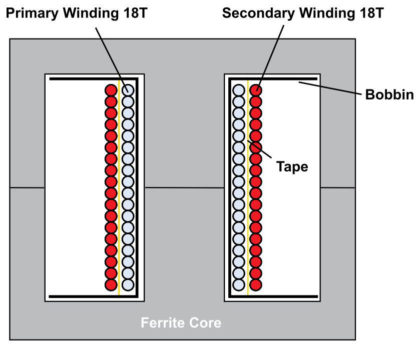


Figure 2: Winding layout of the transformer of Figure 1.

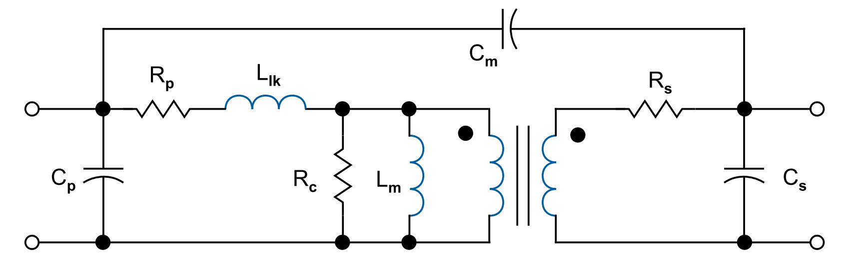


Figure 3: Equivalent circuit model used for 2-winding transformer.

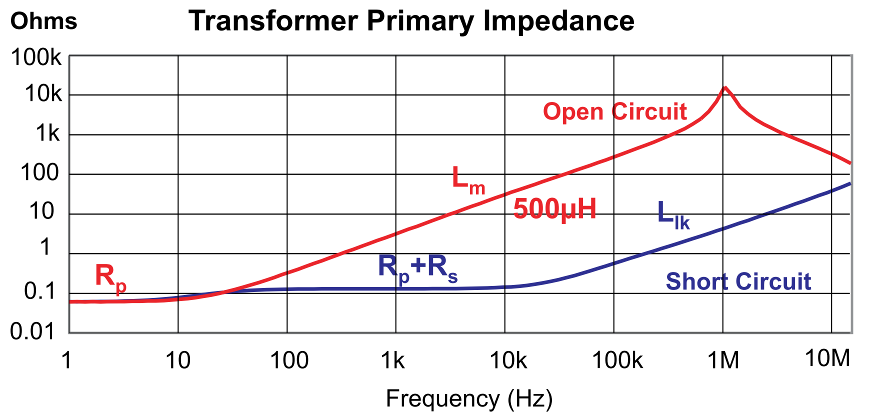


Figure 5: Primary impedance measurements with the secondary both open-circuited and short-circuited.

characterize their parts at a single frequency, we will see that it is important to measure characteristics over a very wide range in order to capture some of the important effects of the magnetic structure. For a 100 kHz transformer, important features show up in the measurement when it is swept from 1 Hz all the way to 15 MHz.

Fig. 5 shows the two impedance curves with the secondary open and short-circuited. The open-circuit measurement gives information on the primary resistance, magnetizing inductance, and capacitance (via the resonant frequency seen at about 1 MHz). The magnetizing inductance can vary significantly from one transformer to another due to material variations, temperature and frequency. However, for the sake of keeping this article short, the magnetizing inductance is treated as a constant over our frequency range of interest, and its value from the measured impedance is 500µH.

Core loss is a quantity that we will also not consider in detail in this article due to the complexity of the topic. The

Figure 4: Impedance measurement test setup using the AP200 frequency response analyzer.

reader is encouraged to refer to [2,3] for more information on advanced modeling and measurement of core losses.

Leakage Inductance

The short-circuit measurement of Fig. 5 contains a wealth of useful information which will strongly affect the performance of the transformer. At very low frequencies (below 5Hz) we can directly measure the primary dc resistance. Beyond 10Hz, we see the value of the primary and reflected secondary resistance.

At frequencies above 10 kHz, the impedance rises due to an increase in resistance, and the leakage inductor impedance. From the impedance curve, we need to separate out the real and imaginary parts to establish the contribution of each of these elements.

Fig. 6 shows the imaginary component extracted from the short-circuit impedance measurement, used to calculate the value of the leakage inductance. This is a very interesting curve in that it does not produce a fixed value of leakage inductance versus frequencies as many engineers would expect.

Below 5 kHz, the reactive component of the short-circuit measurement is small compared to the total impedance, and accuracy of measurement is lost at these lower frequencies.

Above 40 kHz, the inductance starts to decrease significantly from just above 0.8 µH to 0.4 µH above 10 MHz. The change in inductance is due to proximity effects in the windings. At high frequencies, the current in the primary and secondary are not distributed evenly through the wire. In fact, they move closer to the surface of the wire at the isolation boundary between the

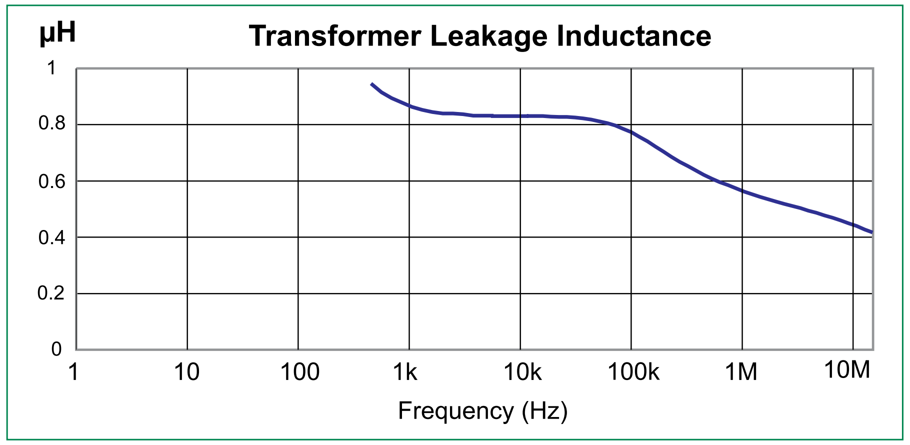


Figure 6: Leakage inductance calculated automatically from the transformer short-circuit impedance measurement.

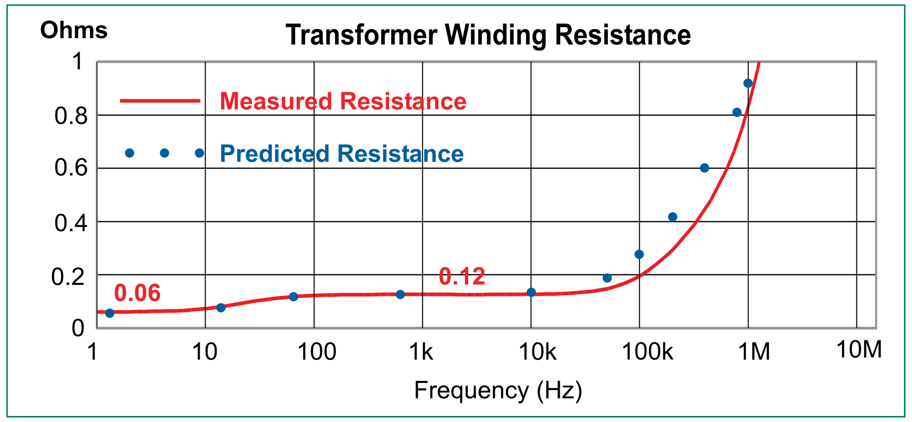


Figure 7: Transformer winding resistance found by extracting the real component of the short-circuit primary impedance measurement.

winding layers. This drops the leakage inductance.

This leads to the interesting question—which value to use? The leakage inductance will cause ringing in the circuit at high frequencies, so it is essential to know the value at the ringing frequency in order to be able to design a proper snubber. However, for production design verification, you might want to use the fixed value between 5 kHz and 40 kHz as a specification to the manufacturer, but you must specify the measurement frequency if you want the parts built with good tolerance.

There is an industry rule of thumb that I often see quoted: "The leakage inductance should be 1% of magnetizing inductance for a transformer." In our design example, the leakage is less than 0.2% of magnetizing inductance at 10 kHz, and 0.1% at 10 MHz. Never accept the 1% figure from a manufacturer as a design objective. Make the best transformer you can with tightly coupled windings, measure your prototype, and expect the manufacturer to match it closely.

Measured Winding Resistance

Fig. 7 shows the real component extracted from the short-circuit impedance measurement, used to calculate the value of the winding resistance.

Proximity effects in the windings affect the resistance even more than the inductance, and the increase in loss at high frequencies can be very severe. The DC resistance of the primary and secondary wires in series is 0.12 ohms, as shown in the curve up to about 10 kHz. Beyond this, the resistance rises steeply, and at 1 MHz, the resistance of the wire is about 7-8 times higher than the DC resistance. At 100 kHz, the switching frequency of the converter, the wire resistance is almost double its DC value.

This increase in AC resistance will directly affect the losses in the transformer, and it is crucial to quantify this before settling on a transformer (or inductor) design. You can even estimate this effect before building the transformer, and this is shown in Fig. 7 by the blue dots. Calculations are done using a form of Dowell's equation and you can read more about this in. [4]

Summary

When designing transformers and inductors, you should always be aware that these seemingly simple structures are in fact very complex electromagnetic devices. Linear circuit models are a very crude approximation to the real component, and most of the elements of the circuit models have strong nonlinearities in them. For this reason, you can only expect very limited results in trying to run circuit simulators on power supplies.

You should always make extended frequency response measurements on transformers when you are developing components. This will show increase in resistance with frequency, and change in leakage inductance, allowing you to properly specify the test conditions for a tightly-controlled part.

The changes in the winding resistance and leakage inductance will be strongly dependent upon the physical winding layouts of the transformer, and great care should be taken to control this as tightly as possible during design and manufacturing.

Additional Reading

[1] "Measuring Frequency Response", Ray Ridley, www.switchingpowermagazine.com/downloads/Measuring Frequency Response.pdf.

[2] "Core Loss Modeling and Measurement", Chris Oliver, Micrometals, www.switchingpowermagazine.com/downloads/New Core Loss Model.pdf.

[3] "Modeling Ferrite Core Losses", Ray Ridley, www.switchingpowermagazine.com/downloads/7 Modeling Ferrite Core Losses.pdf.

[4] "Proximity Loss in Magnetics Windings", Ray Ridley, www.switchingpowermagazine.com/downloads/13 Proximity Loss.pdf.

www.ridleyengineering.com

Have Bricks Hit the Wall?

Power sources undergo surgery for the future

The venerable brick has been around for over twenty years and now faces many challenges. I asked Patrick Le Fèvre, Marketing Director for Ericsson Power Modules, to review their evolution and give us a look into the future.

Reported by Cliff Keys, Editor-in-Chief, PSDE

Since their introduction, with accelerating technology, power bricks have become progressively smaller, saving valuable board-space. Introduced in 2004, the sixteenth brick module has been on the market for two years with DOSA, the Distributed-power Open Standards Alliance established by leading DC-DC converter manufacturers. Most indications indicate that the 'new' package is taking off slowly and there has been little discussion to-date on further size reductions. At the other end of the spectrum, full bricks offering 700+W have become too powerful for many applications.

Distributed Power Architectures (DPAs) such as the Intermediate Bus Architecture (IBA) are eroding what was understood as the traditional brick opportunities by providing isolation in a separate stage from the power conversion. Even Vicor, the original power mason, is pushing a new form factor based on its Factorized Power Architecture. Additionally, power semiconductor manufacturers are increasing their presence in the market and we are seeing more discrete solutions finding their way into new telecom applications, such as ATCA based boards.

So, Patrick, have bricks finally hit the wall?! Give us a sense, from your perspective, of what's to come for the rest of the decade.

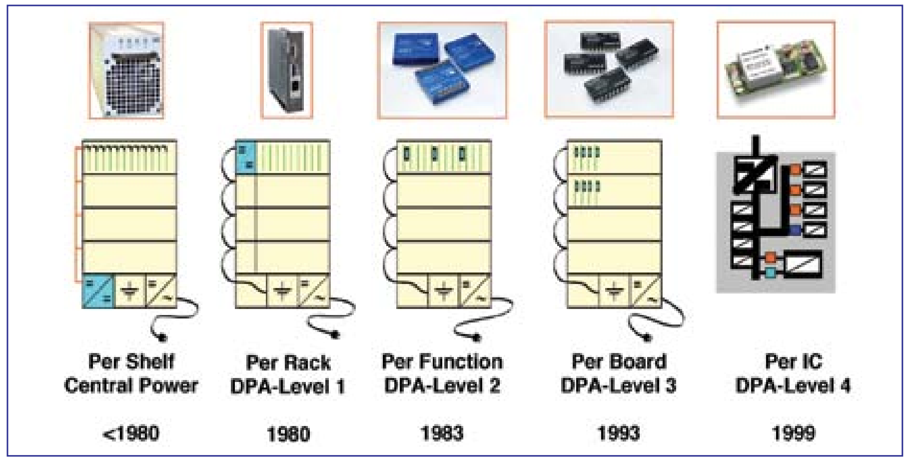
"Certainly they have not. The evolution of the BMP (board mounted products) industry has been driven by several complex factors, all tightly related to end-users' applications but also related to macro-economics and business globalization. Another very important factor that has influenced the emergence of new architectures and bricks, is the speed of technology-shift that results from high competition, pushing system integrators to offer higher capacity to customers and operators. This trend, in combination with different environments (system cooling moving from still air to forced convection and now liquid cooling) as well as new topologies (from diodes to synchronous rectification) has created a lot of room for development and innovation.

Caption: Patrick Le Fèvre, Marketing Director for Ericsson Power Modules

Among the many trends, three are dominating the BMP world. These have, and will continue, to contribute to the next generation of bricks profiled for 2010 applications with highly integrated functionalities."

What have been the drivers in this 'forced-evolution'? In my engineering span, I remember when a power brick really was like a brick, in terms of size, weight -and in comparison to today's offerings- in relative functionality too!

"DPA architectures followed customers' developments and the migration from analog (c1980) to digital (c1990) and to intelligent power (c2000), driving new developments in the business and the creation of more innovative bricks. Throughout, the trend has been towards higher power density and smaller size.



Caption: DPA history

Caption: Ericsson bricks have reduced in size from half, quarter, eighth, down to sixteenth, all of similar power rating.

One of the most important steps in bricks' evolution has been the migration from free air convection to forced air cooling, which combined with new topologies – for example synchronous rectification – and the availability of smaller components, has made it possible for manufacturers to dramatically increase power density while reducing size.

This has also been pushed very strongly by end-users to decrease the amount of valuable board space allocated to power conversion, to make room for core applications (e.g. ASIC, DSP and other processors).

It's also worth noting that not so long ago that high-efficiency half-bricks underwent a drastic size reduction and a simultaneous increase in power density. In 1999 Ericsson Power Modules received the 'Product of the year' award from Electronic Products magazine when it introduced a half-brick design using a synchronous rectifier, highly optimized for efficiency, yet only six years later, today's bricks are challenging the very same power levels in less than a quarter of the real-estate!

Cost reduction is another driving factor that has forced brick evolution to adopt new mechanical platforms and innovative topologies. In 1999, the half-brick at 100W was about $95, in 2003 the same form factor and power level was just $40. At the same time, product development had to take into consideration new legislation such as RoHS, and new ways of working related to manufacturing delocalization such as the US and EU going to Asia, and wide outsourcing to various CEMs."

What about point of load (POL)?

"Bricks associated with POL have gained enormously in functionality, for example in sequencing and tracking. I am convinced that the production of new generations of bricks and POL devices that include such functionalities and trends in order to increase the level of embedded functionalities will continue, until bricks and POL become part of the digital loop."

So, where does this leave the brick industry? Will progress slow-down to a stop here, so that they are to be simply the bulk power module with the rest left to the semiconductor chip industry to provide the 'super-innovative' digital and analog control functions?

"No. I believe that due to globalization and increased competition from all over the world, and, of course, these new developments you mention from the semiconductor industry, bricks will develop by increasing their level of integration. Close relationships between silicon and brick manufacturers will certainly result in new generations of products that are highly integrated into the end-customers' digital loop and will form the 'heart and brain', absolutely central to the power allocation throughout a system.

If, as you imply, the challenge is to create standardized bricks with embedded functionalities allowing customers to have full control over their power management and interoperability between the processor and BMP, where do we go from here?

"The brick market is not a monolith. It will continue to address different applications, segments, customer needs and applications. Embedded functionalities will continue to develop to support many applications, although a significant number of others will not require such a high level of sophistication and will simply focus on other basic areas such as cost and size.

I believe that the challenge for brick manufacturers is to move forward now on standardization and to find a route to offer without compromise, high quality such as 100% yield concept and higher specification bricks in terms of power density and system power efficiency, all at highly competitive prices required by end-users. At Ericsson, we are very active in standards bodies and user groups and are ahead of the curve on where our focus needs to be. Legislation, as well as customer and environmental needs, tell us that we have to put power management and energy conservation high up on our agenda.

But with this backdrop of over 20 years evolution and technical innovation, bricks have reached a level of maturity where they will surely stay, haven't they?

"No. Now the challenges facing BMP designers have never been so demanding. With the latest evolution of digital control and highly integrated power management, bricks have already moved forward dramatically in embedding functionalities and controls, increasing the level of integration, making them available to communicate with key system components such as today's processors and power management controllers.

Additionally, as well as bricks talking with the rest of the board, the migration to digital controllers now makes them more efficient in terms of power consumption, a vital contribution to overall levels of energy preservation, very high on the agenda in every market sector and region.

Despite voices predicting the end of standardized bricks in favour of alternative architectures, recent developments based on a digital controller are proving, without doubt, that bricks are continuing to develop in terms of performance and integration, totally in line with the best interests of telecom and datacom manufacturers.

So, with regard to your provocative question "have bricks hit the wall?" The answer is a resounding 'NO!', though tomorrow's bricks will most certainly have significantly different form factors than the full bricks that we now know."

www.ericsson.com/powermodules/

The "Simple" Legacy Continues… and Flourishes

Simple switcher regulator family has healthy offspring

National's Simple Switcher regulators have come of age The famous family of devices that helped many power designers through the transition from linear regulators to switching regulators, have now made another leap forward offering more flexibility, efficiency and faster design-time.

By Frederik Dostal, Applications Engineer, National Semiconductor

Both the term and product, Simple Switcher®, has changed the low voltage DC to DC switching power supply market since the idea was first introduced in early 1990. It was a time when much of the lower power DC to DC voltage conversion was carried out using linear regulators. Simple Switcher regulators enabled circuit designers who then had little experience in switch mode power design to build their power supplies. The enormous success of this family of products and the current release of a new dimension to the family, today calls for a 'stroll down memory lane' to the very beginnings of this switching regulator concept.

National introduced the Simple Switcher family roughly 16 years ago. It was the first family of its kind, where a host of support elements were prepared so that very little power supply expertise was required from potential customers. First of all, the devices included an easy, step-by-step guide to enable selection of critical external components. Not only component values were suggested, but exact component device numbers could be chosen from external component

Figure 1: Early Simple Switcher regulator from the mid-1990's

lists included in the datasheets. The need to select a power transistor was reduced to selecting the Simple Switcher regulator with the appropriate current rating and because the power transistor was included, the selection process was greatly simplified.

The Simple Switcher devices themselves were built with only very few pins and external components for the power designer to worry about. A major concern regarding power supply design at that time was taken out of the equation by integrating the loop compensation into the IC. The customer was given a range of external components to work with and the internal compensation of the device was set so that the finished circuits would stay within a stable range. This eliminated the design considerations and risk in designers' minds, at that time, of their circuits going unstable.

To top it all off, each Simple Switcher evaluation kit was sent out with a computer disc containing 'SMS' which, in the early 90s, did not stand for 'Short Message Service' in mobile phones, but for 'Switchers Made Simple®'. This was the predecessor of National Semiconductor's Webench® online simulation tool. Switchers Made Simple software is still available for download from National's website and just like Webench, enables a customer to simulate a switch mode power design. This helps designers select external components for the design as well as to optimize a circuit for its end application, saving time and money compared to an iterative approach on a lab bench.

The first release in 1990 of the Simple Switcher family consisted of just a handful of devices. Different current ratings and various fixed output voltage versions existed for both step down as well as step up switchers. The switching frequency was set to 52 kHz and was well suited for the target market 16 years ago. The family was developed with a wide input voltage bipolar transistor process allowing input voltages from 4.5V to 40V and on special HV (high voltage) devices, up to 60V.

Shortly after, the switching frequency was increased to 150 kHz to decrease the amount of inductance and capacitance required in a given circuit. This was geared to help a customer save board space and reduce component cost. The third wave of products within this family was a series of 260kHz switching regulators, again, available in many fixed output voltage versions as well as current options. Compared with the first 50kHz switchers, these devices were also available with new features. If someone needed a softstart, he could get an option with softstart. If someone needed to do frequency synchronization, he could buy an option with frequency synchronization. This family of devices is designated LM267X where X is a place-holder for a number from 0 to 9 representing different basic options. These devices were the first Simple Switcher regulators to use a MOS internal power switch rather than a bipolar power switch. This change was made mainly for higher efficiencies, especially at higher switching frequencies, compared with the previously released family members. Using a MOS process with an N-FET pass transistor requires a gate voltage higher than the drain voltage. Since a typical buck regulator has the drain of the power switch connected to Vin there is voltage available in the system to make the gate turn on. This is when the simple switchers started using a Cboot capacitor, a small capacitor connected from the switch node to a dedicated Cboot pin. This charge pump provides

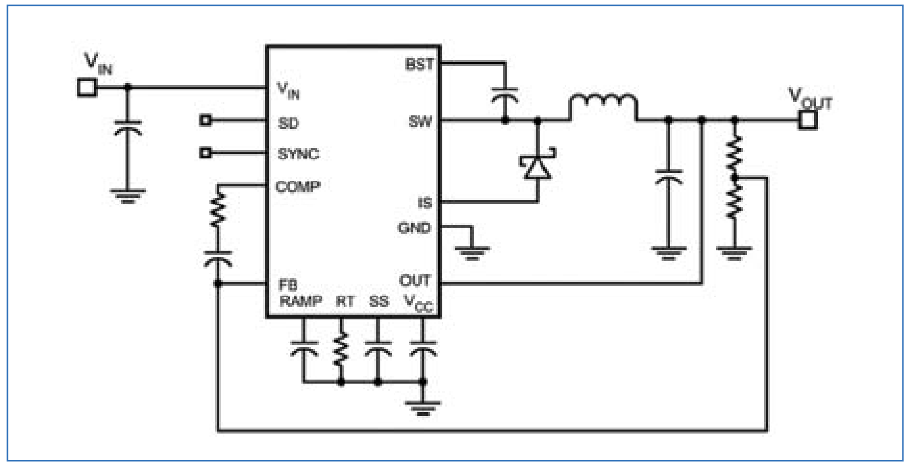
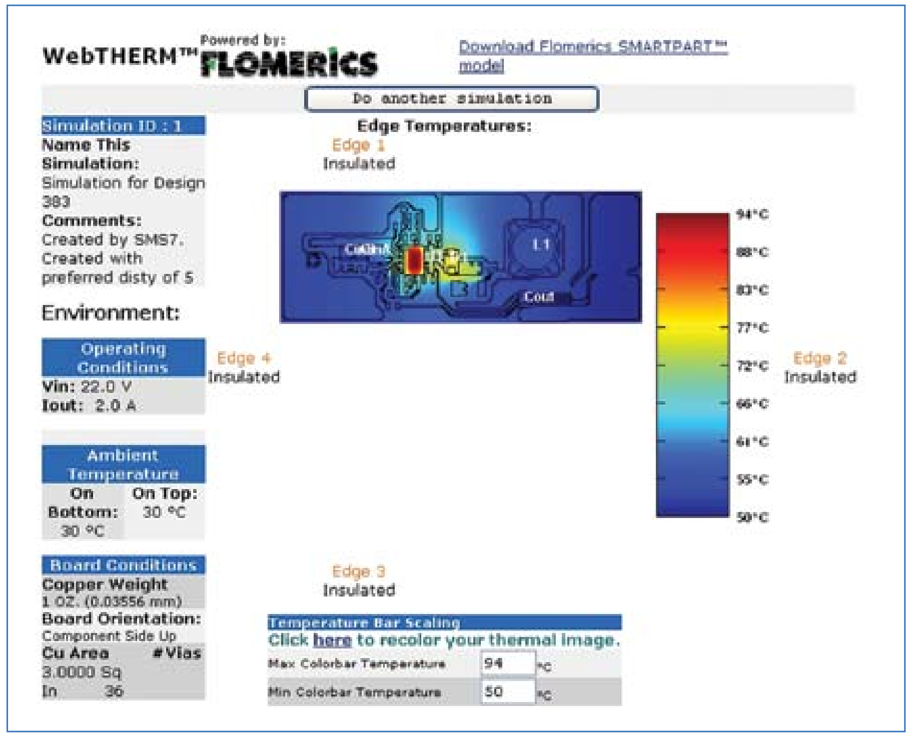


Figure 2: Simple Switcher regulator circuit.



Caption: Webench provides vital information for higher power designs.

enough voltage for the driver to turn the internal N-FET on completely. These changes in the architecture introduced a minimum off-time in which the Cboot capacitor would have to be recharged after each cycle, limiting how close Vin could get to Vout without losing regulation. The result of these changes was also an increased regulator efficiency of up to 96%. Switching losses were reduced significantly by very short transition times of only about 20ns. Older devices had transition times of 70ns or more.

Today, National Semiconductor has introduced a new wave of Simple Switcher regulators picking up where past generations left off. Again, the devices are manufactured in a high voltage process with an N-FET power switch allowing an input voltage range from 6V to 75V. The switching frequency of these modern devices is now adjustable on every device of the family. Frequencies up to 1MHz are possible. This will make the design process more flexible and enable very small-size solutions. Users familiar with the early Simple Switcher family members will enjoy the added flexibility of these new devices. Though they are still 'simple' to use, the designer has more flexibility in optimizing for board size (high switching

Caption: Today's Simple Switcher regulator evaluation board.

frequency) or efficiency (low switching frequency).

Since packaging technology has advanced significantly over the last few years, the seemingly bulky TO-263 packages are now replaced by a low temperature resistance TSSOP exposed pad package. This package combines a relatively low thermal resistance with a higher pin count than the older designs. These extra pins enable many simultaneous features that early Simple Switchers could not provide due to the pin restrictions in the older packages. There is an adjustable softstart available, externally adjustable switching frequency, a sync pin to synchronize the switching frequency of one device with another device, as well as a shutdown pin. Considering this flexibility one could call these Simple Switcher ICs the 'advanced simple switcher'. But even though functionality is vastly increased, the user design process stays as simple as possible, just like working with the original Simple Switcher regulators. To accomplish this, comprehensive design support has been put in place to enable free online simulations with Webench, providing both electrical and thermal simulation capability. Especially for designers of higher power systems, the thermal simulations can be extremely valuable. There are special step-by-step guides in application notes to help a designer decide very quickly which external components to select.

Behind the scenes of the new Simple Switcher launch, there is a very interesting control topology implemented. So far, most Simple Switcher devices have been voltage mode regulators. It is a control architecture in which the error voltage from the error amplifier is compared to an internally generated sawtooth waveform. The Simple Switcher regulators intended for boost and flyback topologies use current mode control. Here, the error voltage from the error amplifier is compared with a signal which is proportional to the actual inductor current.

In the new Simple Switcher devices, an interesting control loop concept is used which is called 'Emulated Current Mode Control'. This behaves very

Product ID	Eval Board ID	V_{IN} Range (V)	V_{OUT} (V) Min	I_{OUT} (A)	f_{SWITCH} Range	Packaging
LM5576	LM5576EVAL	6 to 75	1.225	3	50 kHz to 500 kHz	TSSOP20-EP
LM25576	LM25576EVAL	6 to 42	1.225	3	50 kHz to 1 MHz	TSSOP20-EP
LM5575	LM5575EVAL	6 to 75	1.225	1.5	50 kHz to 500 kHz	TSSOP16-EP
LM25575	LM25575EVAL	6 to 42	1.225	1.5	50 kHz to 1 MHz	TSSOP16-EP
LM5574	LM5574EVAL	6 to 75	1.225	0.5	50 kHz to 500 kHz	TSSOP-16
LM25574	LM25574EVAL	6 to 42	1.225	0.5	50 kHz to 1 MHz	TSSOP-16

Caption: Six New Simple Switcher Regulators.

similarly to a conventional current mode control but makes up for some of the disadvantages of common current mode regulation.

In general, peak current mode control has three key advantages over voltage mode:

1. In peak current mode control, one has automatic input voltage feed forward. In other words, when Vin changes, the loop detects this change directly by the inductor current ramp changing. A voltage mode regulator without feed forward would have to wait until the output voltage has risen (due to the input voltage rise) and could only then counteract by adapting the duty cycle to the new input voltage. In current mode control these variations of the output voltage due to input voltage variations are minimized.

2. Peak current mode regulators have a direct cycle-by-cycle current limit. When the peak inductor current becomes larger than a certain threshold, the on-time is terminated immediately. Voltage mode regulators need a separate current sensing circuit to limit peak currents.

3. Loop compensation is easier with current mode regulators than with a voltage mode control regulator. A voltage mode regulator is a two pole system, whereas a current mode regulator is single pole.

Conventional current mode regulators have the drawback however, that the current can not be accurately sensed immediately after the start of the on-time. There is some switching noise which first needs to settle before an accurate current measurement can be taken. This delay time is called 'blanking time'and the minimum value for this is always a compromise between fast and accurate current measurements, without premature on-time terminations. The long delay hurts the input to output voltage ratios possible. Especially at higher switching frequencies, the blanking time limits the converter's Vin to Vout ratio. A typical value for this blanking time is around 200ns.

Emulated current mode uses an emulated control ramp rather than the real inductor current ramp reducing noise sensitivity of the PWM circuitry. This means that the blanking time of each cycle can be reduced without having to worry about picking up switching noise with the current sensing circuitry. This gives a designer all the advantages of peak current mode control, yet it reduces the blanking time significantly. The typical minimum on-time length of the new LM5576 with emulated current mode is 80ns. This makes a conversion from 60V to 5V possible at 1MHz switching frequency without running into minimum on-time issues.

In detail, the emulation of the actual inductor current is done by a sample and hold circuit which samples the diode current before the power switch is turned on. This current measurement is then used as a starting point for a ramp which is emulated by an external capacitor and added to it. The external capacitor is charged by a current source which is controlled by the input and output voltages of the power supply, emulating the 'real' inductor current without actually measuring it directly.

The new additions to National Semiconductor's Simple Switcher family will help designers to build power supplies in a very short and economic timescale. The added flexibility of the new devices, combined with the comprehensive technical support elements in place, will help design engineers tackle today's demanding power circuit challenges with confidence.

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PORTABLE POWER

Moving to Smaller Solutions

How many rails do you need?

This article details recent developments in power supply circuits. The devices outlined show how improvements in circuit topology and packaging help the designer to develop much smaller solutions for today's power supply challenges.

By Thomas Schaeffner, Systems Engineer for Power Management Unit, Texas Instruments, Freising, Germany

There is a trend in Portable equipment such as PDAs, portable navigation systems (GPS) and smartphones for the integration of different functions into one single chip. Some years ago, there was one stand-alone power converter for each power rail needed. As the functions of battery powered devices became more complex, the power supply design changed too. There is now a clear trend towards integration. Besides the power needed for the processor, there are other functional blocks such as Bluetooth modules, WLAN modules or the power needed for the display, which require separate power rails, in addition to the processor. There are different power concepts that can be found in such applications:

- Power supply chips that contain additional functions such as CODEC, ADC, audio amplifier, battery charger etc.
- One single power supply chip for all power rails needed
- Dedicated converters for a functional block

This article will show solutions that cover the last two of these concepts. Designing with converters for a dedicated block gives several advantages. Firstly they can be placed on the board more easily directly next to a processor or WLAN module they provide power to. Secondly, layout is simplified as signals do not have to be routed throughout the whole board. In addition to this, the coupling of other sources to and from these power rails is minimized. This is especially important for sensitive

power rails like GPS modules or PLLs (phase locked loops). There is also an advantage for follow-on projects that are based on the current solution. In the case where the design is upgraded to a new generation, the changes can be applied on a block level - just the blocks that have to be upgraded need to be touched by the designer, all other blocks can stay as they are. With one single power supply chip for the whole application, there is much more effort to adopt the design to new requirements. With shorter development cycle time being key for product success, this power concept gives a clear advantage. In order to provide a complete solution for this, the power supply chip needs to fulfill several requirements. There must be a family of devices available that can provide exactly the rails required while retaining the smallest footprint possible in order to conserve board space. Furthermore, these chips should be flexible in order to allow easy adoption of the solution to different requirements. One example is the TPS6502x family and TPS6505x family of devices from Texas Instruments. These devices are optimized for power application processors in handheld devices. As the requirements between different processor families change, there are different chips that are dedicated to a processor or processor family as well as to the application.

Device	converter1	converter2	converter3	LDO1	LDO2	QFN package	For processor
TPS65020	3.3V/1.2A*	1.8V/1A*	1.3V/0.8A*	1.3V	1.1V	6mm x 6mm	PXA270
TPS65021	3.3V/1.2A*	1.8V/1A*	1.3V/0.9A*	adj.	adj.	6mm x 6mm	PXA270, DM320
TPS65022	3.3V/1.2A*	1.8V/1A	1.3V/0.9A	adj.	adj.	6mm x 6mm	PXA270
TPS65023	1.2V/1.5A*	1.8V/1.2A	3.3V/1A	adj.	adj.	5mm x 5mm	DaVinci™ Processors

**The output voltage of converter 1 to converter 3 can be changed by an external resistor divider, the LDO voltage if set by two digital input pins. In addition to this, the I2C interface allows to set the output voltage of all converters and both LDOs.*

Table1: TPS6502x device family overview.

In general, high efficiency over a wide range of output currents is key in battery powered applications. Therefore, all devices are optimized for low quiescent supply current – the current the chip needs without providing any current to the output, but still maintaining the output voltage. This parameter is critical for applications that are operated in standby mode over a long period of time. A low quiescent supply current not only improves standby time – when the application does not require any supply current, it is also an important parameter when it comes to efficiency at very low output current of a dc/dc converter. The efficiency of a dc/dc converter, e.g. a step-down converter, is influenced by three factors. At a high output current, the efficiency is mainly determined by the resistance of internal power switches, so a low resistance is important in this operating range.
In step-down converters, operated in fixed frequency pulse width modulation mode (PWM), the duty cycle depends on the input to output voltage ratio. For low output voltages, the internal low side switch (NMOS) is turned on for a much longer time than the high side switch (PMOS), whereas for high output voltages, the high side switch is turned on most of the time. Therefore it makes sense to adopt the size and hence the resistance of the switches to the output voltage, to which the converter is targeted, assuming the input voltage is the same for all converters, typically a Li-ion cell in portable applications with a voltage range from 4.2V down to about 3.0V, with the trend to lower voltages down to 2.5V in the future. For an output current in the range of 10mA to 200mA, the resistance of the switches does not account for the majority of the losses any more, however, the gate charge for the power switches and inductor losses determine the efficiency in this operating range. Adopting the switching frequency to the output current is the key technique to maintain high efficiency over the operating range – called "pulse frequency mode" (PFM). PFM simply provides a constant portion of energy to the output, resulting in a higher switching frequency at high output current and a low switching frequency and therefore low switching losses at low output current. At a very low output current on the converters, the constant loss caused by the quiescent supply current determines the efficiency as mentioned above. All family members of the TPS6502x and TPS6505x family are designed in such a way that the losses are minimized resulting in best efficiency over a wide voltage and current range. Table 1 shows an overview on the TPS502x family. The devices contain 3 step-down converters for system voltage, memory voltage and processor core as well as 2 LDOs for PLL and SRAM or other functional blocks within the processor. There are other features like backup battery support, I2C interface and reset functions that are not listed in the table.

To support application processors that require even more power rails, the TPS6505x family is available. These devices contain 2 step-down converters and 4 LDOs with a high power supply rejection ratio (PSRR). The LDOs drive noise sensitive blocks, like PLLs, GPS modules or WLAN modules. The TPS6505x family allows the design of the smallest power supply solutions due to its small package small external components. The TPS6505x family is available in a small 4mm x 4mm QFN package. The pitch of 0.4mm allows a pin count of 32. This high pin count in addition to the power pad – a thermal pad on the bottom of the QFN package enables highly integrated solutions with excellent thermal performance.

Figure 1 shows the block diagram of TPS65052. This device was optimized for Samsung application processors which require a core voltage of 1.0V in low power mode and 1.3V in normal operating mode. In order to minimize the amount of external components, step-down converter 1 has a fixed 3.3V output dedicated for the I/O voltage. Converter 2 is for the core voltage and can be set to an output voltage of either 1.0V or 1.3V, depending on the status of a digital input called DEFDCDC2. Therefore, no external components are needed to set the voltage for the step-down converters. The same is true for the LDOs. Four digital input pins – DEFLDO1 to DEFLDO4 - set the output voltage according to a table, decoded internally. Three of the four LDOs come with a separate input voltage pin, allowing them to be powered from any input voltage in the range of 1.5V to 6.5V. One LDO can be powered from the battery another could be powered from the output of step-down converter 1 or any other supply voltage rail available in the system. Selecting the lowest possible input voltage for an LDO allows the engineer to optimize the design for high efficiency. For higher flexibility, other members of the family are able have the output voltage set by external resistor dividers. Table 2 shows the options available with the TPS6505x family.

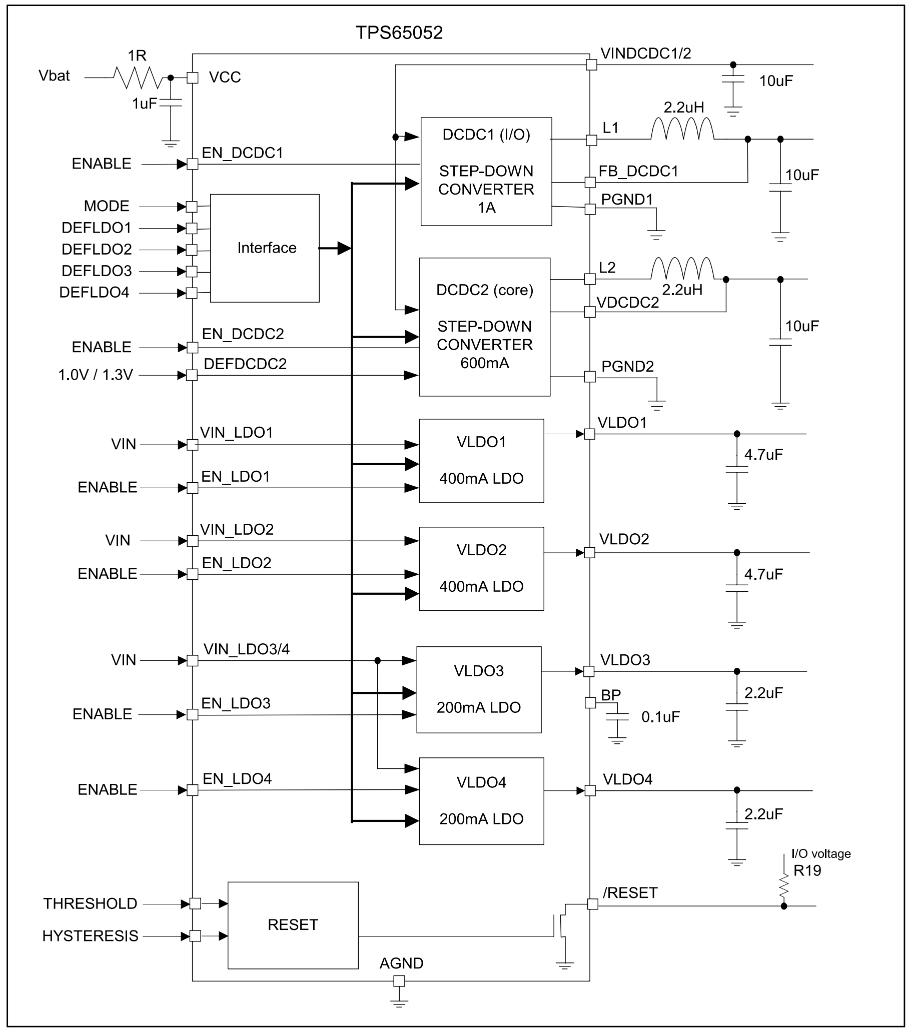

Figure 1: Block diagram of TPS65052.

In addition to the step-down converters and LDOs, the TPS6505x family has a comparator with a 100ms delay time. This block can sense an input voltage to a 1V threshold and generate a reset signal on it s open drain output. With a separate pin, a hysteresis can be programmed. The circuit can also be used to turn the LDOs or dc/dc converters on, once the threshold voltage is exceeded by connecting its output to one of the enable pins of the converters or LDOs. With the TPS6505x from Texas Instruments it is possible to generate 6 different power rails and to generate the reset to a processor with just one small chip.

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Device	converter1	converter2	LDOs	QFN package	For processor
TPS65050	adj. voltage / 0.6A	adj. voltage / 0.6A	adjustable with DEFLDO pins	4mm x 4mm	Generic, S3C2410/2/3
TPS65051	adj. voltage / 1.0A	adj. voltage / 0.6A	adjustable with resistor divider	4mm x 4mm	Generic, OMAP850
TPS65052	3.3V / 1.0A	1.0V or 1.3V / 0.6A	adjustable with DEFLDO pins	4mm x 4mm	S3C2410/2/3
TPS65054	adj. voltage / 0.6A	1.05V / 1.3V / 0.6A	adjustable with resistor divider	4mm x 4mm	OMAP1710
TPS65056	3.3V / 1.0A	1.0V or 1.3V / 0.6A	adjustable with resistor divider	4mm x 4mm	S3C2410/2/3

Table 2: Options for TPS6505x.

Designing for Point of Load Without Mystery

Reference design of a power system with No-Bus™ POL converters

Designing with No-Bus Digital POL converters is as easy as assembling a well known child's building block toy says Mikhail Guz. It requires neither years of analog design experience nor intimate knowledge of Z-transformations. Here we find out how in easy steps.

By Mikhail Guz, Director of Strategic Marketing and Applications Engineering, Power-One Inc

The first step is to select POL converters with appropriate current ratings for your application. If the required output current exceeds the current rating of any single POL converter, then place a number of them in parallel, by connecting CS pins as shown in the schematic (POL1 and POL2).

Next, program the output voltage by adding a resistor between TRIM and VREF pins. The value of the resistor is calculated based on the required output voltage:

$$R_{TRIM} = \frac{20 \times (5.5 - V_{OUT})}{V_{OUT}}, \text{k}\Omega$$

Now, decide on sequencing. Should all POL converters turn-on and off simultaneously? If yes, connect OK lines of the POL converters together as shown in the schematic. If a power-up delay is required, add a delay capacitor between the DELAY pin of any POL converter and the ground. Only one capacitor is required per a group of POL converters that have the same power-up delay. The capacitor is calculated from the equation:

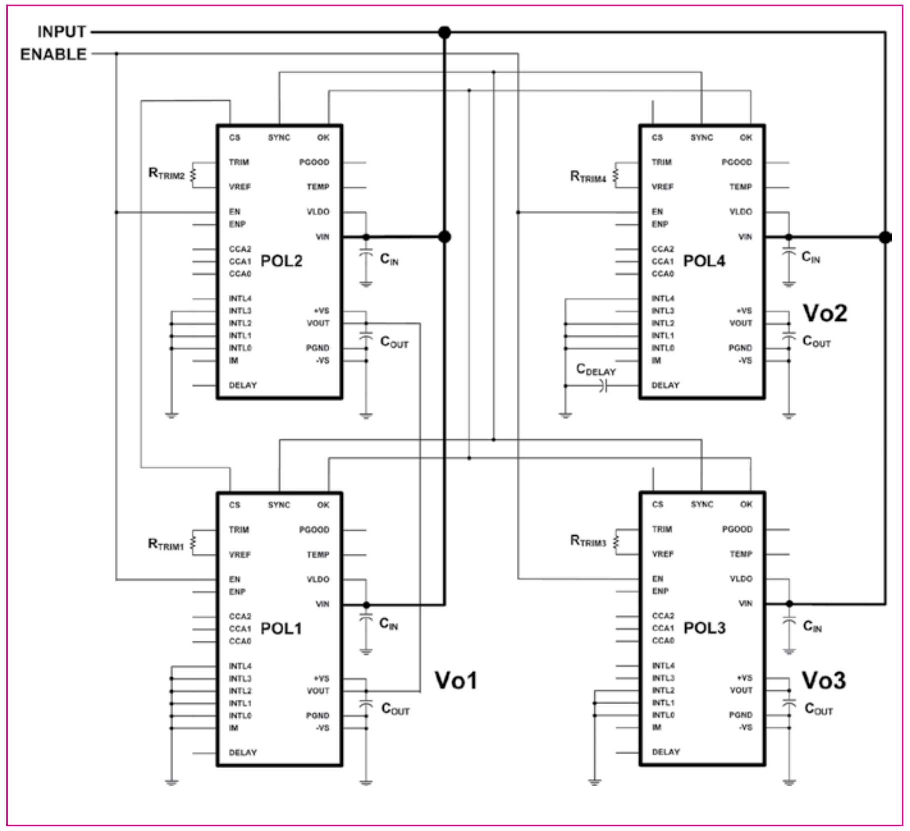
$$T_{DELAY\_25C} = (240 + 0.65 \times T) \times C_{DELAY}, \text{ms}$$

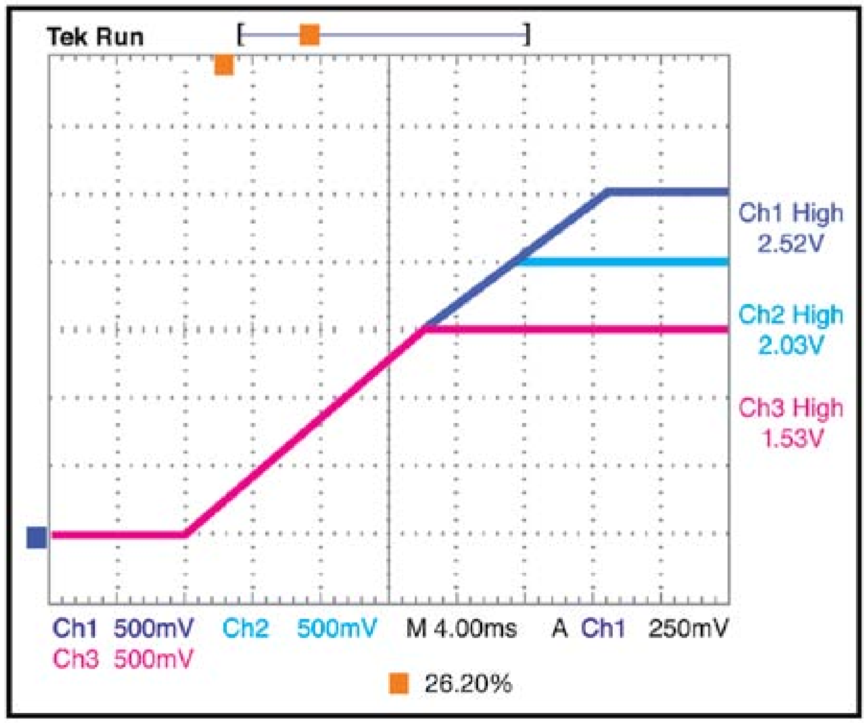
where C_{DELAY} is the value of the delay capacitor in μF and T is the temperature of the POL converter at power-up in degree Celsius. Therefore, for example, a 0.47μF capacitor at room temperature will set the power-up delay to approximately 120ms.

If no capacitor is connected and the EN pin is left floating, all POL converters will start ramping up as soon as the input voltage reaches the UVLO threshold.

To accomplish cascading, interconnect EN and PGOOD pins of POL converters. In this case a POL converter will turn on only after the other POL converter is fully operational and its Power Good signal is high.

No-Bus Z-One™ digital POL converters have advanced power management





No-Bus Z-One™ digital POL converters have advanced power management capabilities such as frequency synchronization, interleave, and feedback loop compensation. The user does not have to activate and program any of those features, however by utilizing them it is possible to optimize system performance and reduce the number of external components.

To synchronize switching frequency of multiple POL converters, connect SYNC pins of all POL converters together and to an external clock. If there is no clock available, a POL converter can be configured to be a clock master by connecting its INTL pins and the IM pin to the ground. In the schematic, the POL1 is the master.

The user can program an interleave or phase shift for each POL converter in the system to accomplish reduction of both input and output noise. The interleave is determined by the decimal number encoded by INTL[0:4] pins. To calculate actual phase shift multiply the number for a respective POL converter by 11.25°. For example, the POL2 has a phase shift of 180°. Such phase shift between two POL converters connected in parallel dramatically reduces the output noise by canceling the switching frequency ripple. POL4 and POL3 have the phase shift of 90° and 270° respectively attenuating the noise reflected back to the input source.

The number encoded by the pins CCA[0:2] recalls a set of digital filter coefficients determining characteristics of the feedback loop. There are 7 sets of coefficients optimized for different input voltage ranges and types and amount of external capacitance. All POL converters in the schematic have CCA=7 which is the best setting for the 8 to 12V input voltage range and the output capacitance comprising of both tantalums and ceramics.

This completes the design process for a power system utilizing No-Bus Z-One™ Digital POL converters. The picture on the left illustrates the turn on process of the power system designed according to the schematic above.

It is possible to further optimize performance of the power system and accelerate the design process by leveraging design resources provided by Power-One Inc. A sophisticated designer can take advantage of the SPICE and IBIS models available for each POL converter. Interactive Excel-based Z-1000 and I/O filter design tools allow completing a design and selecting filters for specific application conditions by answering a few very basic questions. Visit www.power-one.com to download these and other useful design tools and application notes.

www.power-one.com

Trends in Industrial Communications

Availability of 3V isolators enables designers to eliminate one supply and save costs

New transceiver generations are moving towards lower supply voltages, especially in the control area where noise is not so much of a problem. Supply voltage in the range of 3V is becoming standard now.

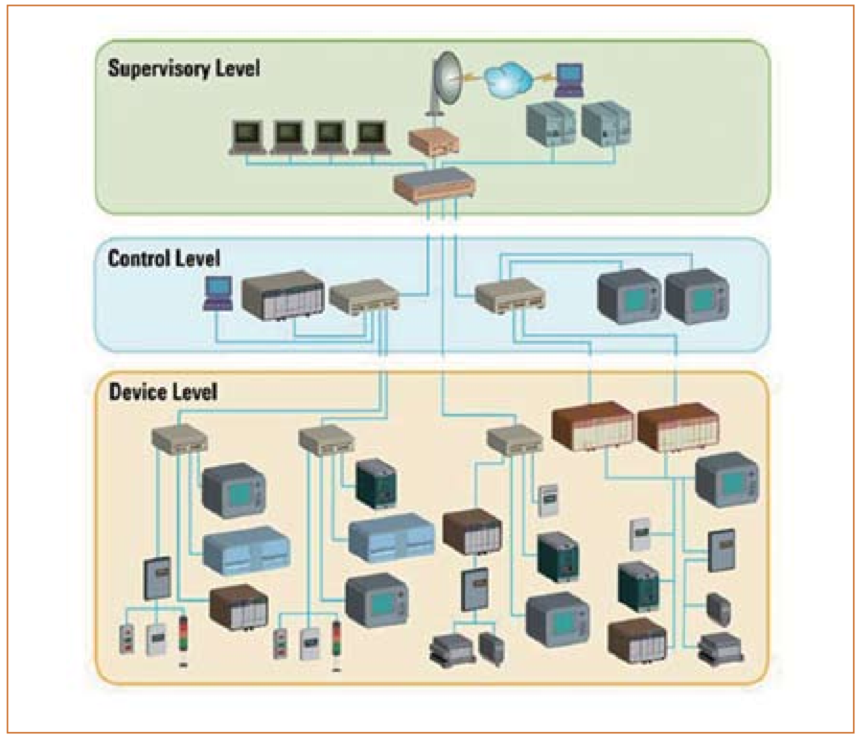
By Alexander Jaus, European Business Development Manager, Optical Communication Solutions Division Electronic Components Business Unit, Avago Technologies

"I think there is a world market for maybe five computers." (Thomas Watson, 1943) While Thomas Watson was not really right with this assumption, he still became one of the richest men of his time. Today we know that it has been computers, miniaturization and globalization that lead to a world of communication. While dynamic of change is obvious in mobile and wireless communication, it does not stop at classic areas such as industrial. Computers, robots, machines, sensors and humans are communicating in a growing industrial automation market and new trends require related components such as optocouplers to meet new challenges.

Industrial communication includes data monitoring and processing, diagnostic and sensing as well as visualizing. It also includes various aspects to maintain data integrity against group loop current or common mode noise where optocouplers are commonly used as they eliminate both problems. Requirements change over years and various technologies and communication buses allow the user to select according to their specific requirements such as speed, switching specifications or security. Sales of fieldbus systems in Europe are projected to rise from their 2001 level of \$170.2 million to \$420.0 million in 2008 (Frost & Sullivan) across all networking levels. The hierarchy of industrial networking includes:

- Enterprise Level (Ethernet PCs, Servers, Gateways)
- Control Level (High performance Ethernet (HSE), Ethernet, ProfiNet)
- Device Level (Profibus DP, DeviceNet)
- Sensor Level (CANbus, Remote I/O)

Smart sensors are nowadays used more and more within industrial systems causing change of communication on device level towards a more complex information exchange. Due to increased miniaturization a sensor becomes basically a small PC with memory and networking capability which allows sophisticated feedback and more



Industrial Networking Hierarchy (Source Omron) to compensate nonlinearity, offset or temperature related errors. These advantages and the new flexibility result in a success story of smart sensors today and boost industrial communication overall; more intelligences is also added in the form of programmable logic controllers (PLC's). They are used to control and handle the information flow on the lower network protocol layers (OSI), especially on sensor and device level.

Fieldbus is another area with expected growth rate as it also benefits from the smart sensors. Fieldbus is often used to connect these individual programmable logic controllers together. Among the most popular used today are Profibus, DeviceNet, Interbus, CAN bus with regional emphasis. In Europe, Profibus created in 1989 by a consortium of companies driven by Siemens, appears to be the market leader while in US DeviceNet supported by Allen-Bradley (Rockwell) is number one.

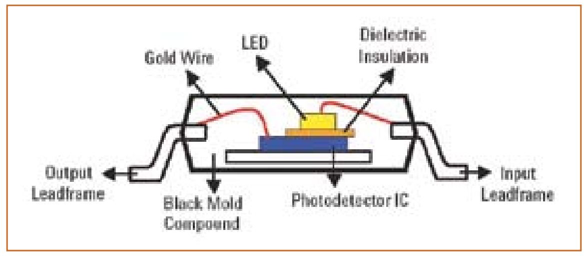
To achieve signal integrity, optocouplers are very often used on interface cards from slow RS232 or CAN bus to high speed RS485 interfaces. To optimize space consumption, multichannel packages are often preferred. Bi-directional communication channels are very helpful in further reducing board space.

Requirements for isolators are often expressed in "speed" or "MBd". More valuable for designers are the switching related specifications such as propagation delay and pulse width distortion. DeviceNet specifies relatively slow data rates 125 kBaud, 250 kBaud und 500 kBaud, but requires less then 40ns propagation delay. CANbus specifies 125kBit/s for low speed and 1Mbit/s for high speed but no sharp requirement on propagation delay. Profibus transmits in the 12MBd range and specifies a total PWD delay for both, isolator, transceiver and connection itself. To meet overall requirements, an isolator typically needs to be less than 8ns, 6ns or less preferred to have more safety margin for e.g. longer distances. Emerging technologies such as capacitive and magnetic isolators offer advertise faster speed up to 100MBd, but the limitation for communication speed comes from pulse width distortion (PWD). Established isolators in the market such as opto.-/magnetic or capacitive couplers do provide a PWD as low as 2ns which sets the maximum speed in asynchronous data communication. This can effectively be used without additional components to 50MBd, which is exactly what optocouplers provide today.

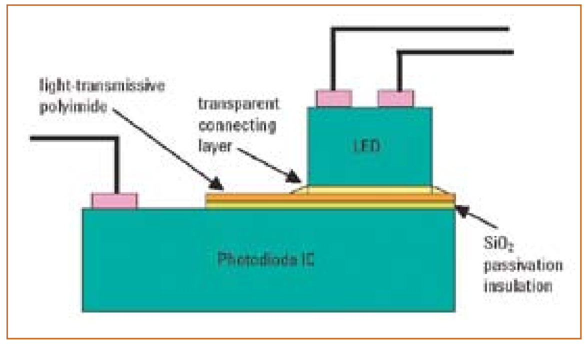
New transceiver generations are showing the trend towards lower supply voltages, especially in the control area where noise is not so much of a problem. Supply voltage in the range of 3V is becoming standard now. The availability of 3V isolators gives designers a chance to eliminate one supply and save costs.

New generations of optocouplers optimized for communication applications are therefore measured by their flexibility of supply voltage and overall board space consumption. Avago Technologies is the only optocoupler manufacturer world wide that offers multi-channel and bi-directional optocouplers as well as a series of digital optocouplers that operates at both, 3V and 5V, to serve these market trends. This technology leadership is based on a breakthrough in LED technology that allows so-called back-emitting LED's. These can be positioned directly on the isolation material, respectively the output IC, reducing the physical size of the LED-isolation-photodiode unit allowing up to 4 channels per package today. Depending on the package chosen, this results in effective board space saving for the customers of 75% and higher. Also, optocouplers pulse width distortion (PWD) as low as 2ns is still best in class.

In the future Ethernet based communication will become more important. ProfiNet is currently promoted in Europe by Siemens, EtherCat is another open standard supported by Beckhoff, and both allow data rates up to 100 Mbit/s. Isolation today is done with transformer technology inherited from computing Ethernet. Optocouplers have not yet found their place and are challenged by new speed requirements. In future, the usage of a new generation of high speed optocouplers is conceivable as well as optical fiber based solutions. Avago Technologies has just released a transceiver based on 650nm LED technology for 1mm polymer optical fiber (POF) and 200um plastic cladded fiber (PCF).



New optocoupler type ACSL-6xx0.



LED technology breakthrough.

Industrial Ethernet and established field buses will co-exist for at least the next 10-15 years, therefore optocouplers will continue to provide isolation, guarantee signal integrity and play a key role in industrial communication for the coming years.

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Trench MOS Barrier Schottky Rectifiers Address Weaknesses of Traditional Planar Schottky Devices

High-frequency applications require higher switching frequencies and greater power consumption resulting in higher voltage spikes

Here, Vishay Semiconductors discuss the limitations of traditional Schottky rectifiers and how they can be alleviated by using an innovative device built on a trench metal oxide (MOS) technology.

By Max Chen, R&D Sr. Director, Vishay Semiconductors
Henry Kuo, R&D Sr. Manager, Vishay Semiconductors
Sweetman Kim, Marketing Sr. Manager, Vishay Semiconductors

Until recently, silicon-based Schottky barrier rectifiers were limited to operating voltages below 100 V for most applications. However, the trend in high-frequency applications has been towards greater power consumption, requiring higher reverse bias voltages (100 V and above) for higher-output adapters. In consumer electronics, there has been a rapid increase in the power consumption of computers, game consoles, and LCD TVs. A similar development has occurred in the design of high-power, high-efficiency telecom base station power supplies. Higher voltage spikes and/or higher switching frequencies are the inevitable outcome of this trend.

Consequently, Schottky rectifiers are now being designed with higher operating voltage ranges. To meet the requirements of the consumer electronics and telecom applications, 100-V Schottky rectifiers have become more common, with new designs moving toward reverse bias voltage ratings of 120 V and 150 V or even 200 V. However, as higher operating voltages have become more common, the performance limitations of Schottky devices have become more obvious.

As shown in Figure 1, planar structures typically implement a carefully designed P-type guard-ring structure, a high-resistivity silicon epitaxial layer, and a high Schottky barrier height to achieve breakdown voltages of 100 V and above with an acceptable reverse leakage current. In this structure, the P-type guard-ring injects minority carriers into the semiconductor drift region; these carriers slow down the Schottky rectifiers under switching conditions.

As the operating voltage moves to 100 V and above, the high-resistivity silicon and high Schottky barrier height become factors in significantly increasing on-state voltage drop and slowing switching speeds. These limitations can be alleviated by using an innovative device built on a trench metal oxide (MOS) technology.

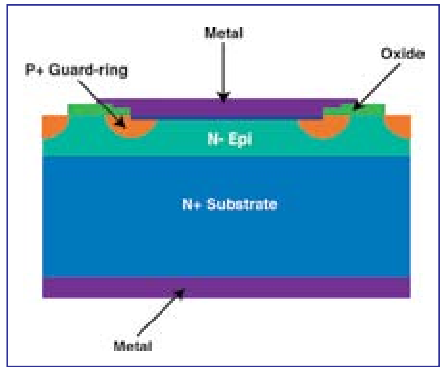

Figure 1. Planar structures achieve breakdown voltages of 100 V and above by utilizing a P-type guard-ring structure, a high-resistivity silicon epitaxial layer, and a high Schottky barrier height.

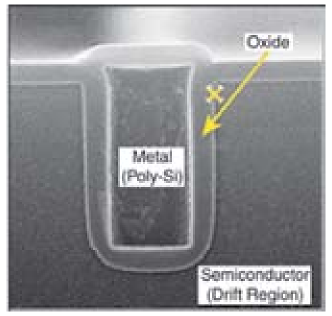

Figure 2. SEM photograph of a single TMBS sub-micron cell.

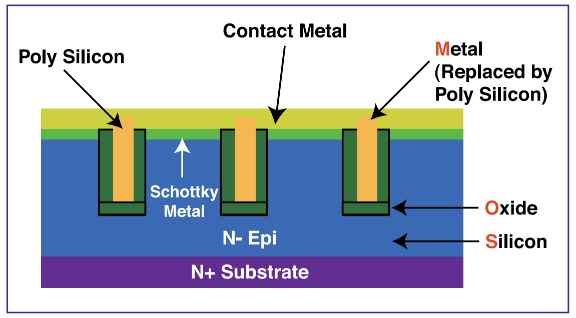

Figure 3. Multi-cell structure of a TMBS.

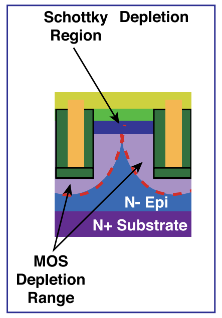

Figure 4. The depletion regions of two adjacent MOS structures will overlap as the reverse bias increases, resulting in an overlapped depletion region.

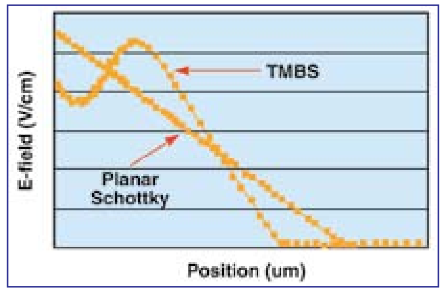

Figure 5. A comparison of the electric field curves of the TMBS and planar Schottky along the semiconductor drift region shows the surface electric field of the TMBS is much lower than the planar Schottky.

The increased on-state voltage drop and slower switching speeds of traditional planar Schottky rectifiers can be overcome by a new series of 100-V rectifiers that apply the Trench MOS Barrier Schottky (TMBS) structure. A single TMBS sub-micron cell is shown in the SEM photograph of Figure 2 and the multi-cell structure of the device is illustrated in Figure 3. The parameters that affect TMBS performance include the trench depth, mesa width, trench oxide thickness, doping of the epitaxial layer, and electric field termination. These parameters are related to stress, charge coupling, optimized forward voltage drop (V_F), and reverse current (I_R).

As shown in Figure 4, depletion regions occur when the TMBS device is in reverse bias, and the MOS couples the charge along its sidewall. The depletion regions of two adjacent MOS transistors will overlap as the reverse bias increases, resulting in "pinch-off" (an overlapped depletion region). The Schottky diode's interface leakage current (I_R) is reduced by this pinch-off electric field.

In the Trench MOS Barrier structure, stored charges are minimized under switching conditions as depletion regions diminish minority carrier injections to the drift region. The switching speed is much improved, especially under high working temperature and high conduction current conditions.

As depicted in Figure 5, the Trench MOS structure provides charge-coupling effects in the drift region that will change the shape of the electric field distribution from linear to non-linear, where same reverse breakdown voltages (which is the integration of electric field along the distance of drift region) will be obtained even with much lower resistivity silicon, as indicated by the sharp gradient of TMBS electric-field curve.

By altering the electric field distribution, the TMBS structure moves the stronger electric field away from the Schottky metal-silicon interface to the silicon bulk. As indicated in Figure 5, the surface electric field (E-field) of the TMBS device is much lower than the planar Schottky devices. The reduced surface field will suppress the barrier-lowering effect, which significantly reduces the leakage current for a given Schottky barrier height. This allows lower Schottky barrier heights to be used without sacrificing reverse leakage performance, which in turn results in a lower forward on-state voltage drop.

TMBS and Planar Schottky Performance and Electrical Comparison

When compared to conventional planar Schottky rectifiers with the same chip sizes and barrier heights, a 100-V TMBS device shows remarkable forward voltage drop performance (Figure 6). The switching performance of the TMBS is also better, as shown in Figure 7.

We performed a series of experiments in which TMBS rectifiers were tested against benchmark planar Schottky rectifiers to compare the two structures in an actual application. In the first test, we used a 350-W switch mode power supply (SMPS) as a test vehicle. TMBS devices rated at 40 A and 100 V were compared to industry-standard Schottky rectifiers rated at 20 A and 100 V (MXXXXH100CT) and two such devices with ratings of 60 A and 100 V (XXCTQ100 and STXXXX-H100CT). All devices in this evaluation are packaged in the standard TO-220.

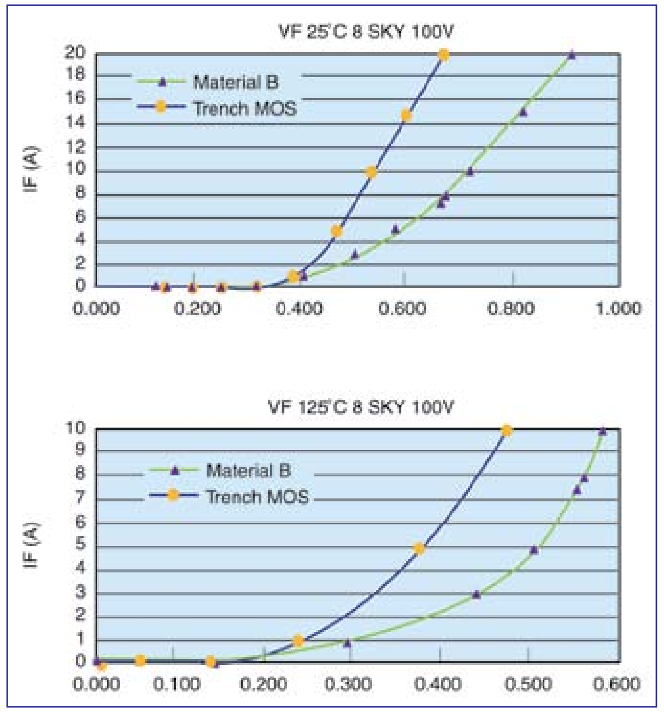

Figure 6. V_F comparison of TMBS and conventional planar Schottky rectifiers

P/N	Input Power (W)	Output Power (W)	Efficiency	Power saving
Industry 20A Planar Schottky (MXXXXH100CT)	299	234	78.3%	0 (Base)
Industry 60A Planar Schottky (XXCTQ100)	298	236	79.1%	2.35W
Industry 60A Planar Schottky (SXXXXXH100CT)	297	235	79.2%	2.77W
Vishay 40A TMBS (VTS40100CT)	297	236	79.6%	3.72W

Table 1. Efficiency evaluation on a 350-W SMPS (switch-mode power supply), comparing TMBS with industry-standard planar Schottky products. TMBS provides efficiency improvement of 1.3 %, for a power savings of 3.72 W.

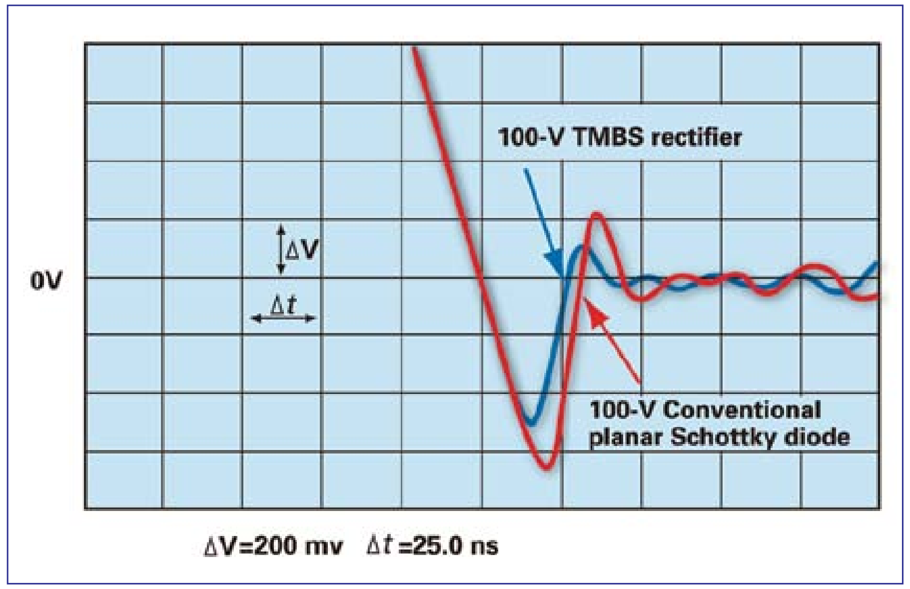

Figure 7. trr curves of TMBS and Planar Schottky rectifiers show TMBS has better switching performance.

The results show that at a 67 % output (about 235 W) to full rated power levels, the 20-A rated device has the lowest total power supply efficiency of 78.3 % (Table 1). When the 60-A rated devices were substituted for the 20-A devices in the same power supply slot, efficiency improvements of 0.8 % and 0.9 % were observed. These improvements translate into a savings of 2.35 W and 2.77 W, respectively, for the power supply. Even when the 40-A TMBS rectifier is used to replace a traditional planar device rated at 60 A, we see an improvement in efficiency of 0.4 %. Compared to a baseline 20-A planar Schottky rectifier, the efficiency improvement is 1.3 %, for a power savings of 3.72 W.

By evaluating TMBS rectifiers with ratings of 40 A and 100 V (VTS40100CT) in a 120-W adapter, we were able to further demonstrate the capabilities of the new TMBS devices. The typical solution for this application is a synchronous rectification approach implemented with two 40-A, 100-V MOSFETs and a matching driver IC. From test data as described

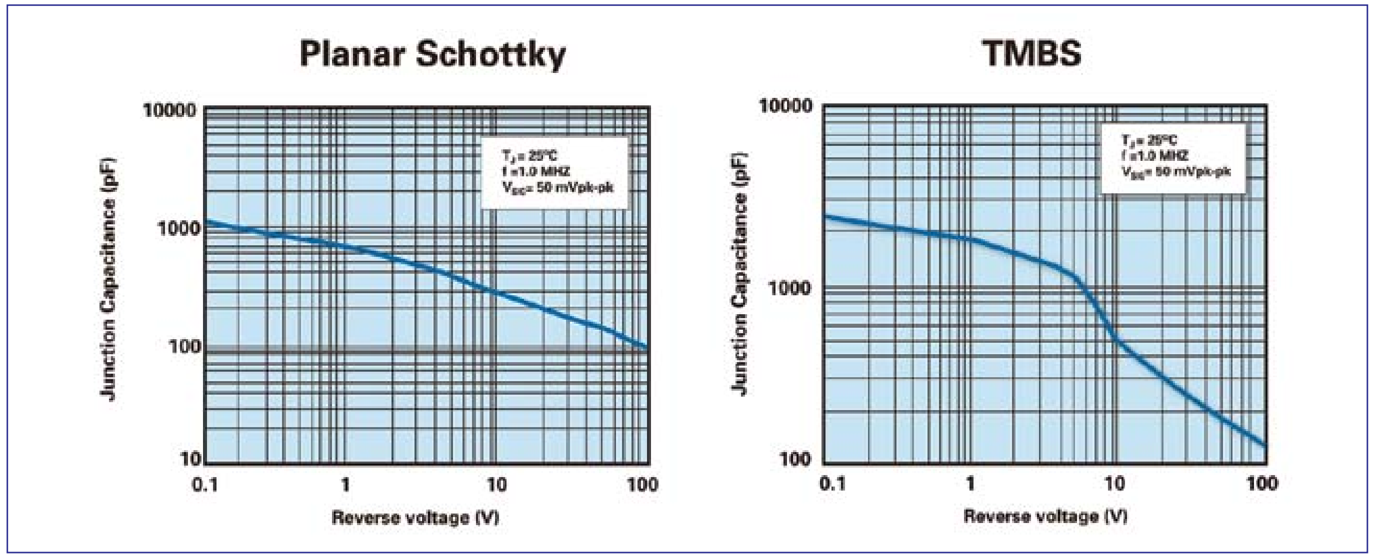

Figure 8. Capacitance comparison between TMBS and planar Schottky diodes shows that TMBS is close to that of the planar Schottky rectifier for reverse bias voltages over 30 V.

in Table 2, and under full-rated 120-W output conditions, the pair of TMBS rectifiers provide the same total adapter efficiency of 87 % as the more complicated, more costly, and less robust synchronous rectification solution.

The ability to withstand higher energy transients during reverse bias is another advantage of the TMBS structure. The strongest electric field of a conventional planar Schottky rectifier is at the surface of the device, which will limit heat dissipation and avalanche energy absorption. The strongest electrical field of a TMBS device, by contrast, distributes at the bottom of each trench well. The silicon bulk can thus absorb and dissipate more avalanche energy than at the surface.

For high ESD or rectification applications such as OR-ing diodes in hot-plug systems and diodes in SMPS, the ability to enable high reverse avalanche energy makes the TMBS rectifier the more suitable structure. The average of 8/20 µs reverse surge energy of the 40-A, 100-V VTS40100CT is about 170 mJ. This is about twice the conventional planar Schottky diode's reverse surge energy under the same test condition.

At a low reverse bias, TMBS devices have a much higher capacitance (C_J) than planar Schottky diodes. This high capacitance is caused by the trench sidewall and bottom capacitance being in parallel with the original Schottky barrier capacitance. When reverse bias increases, however, the TMBS capacitance falls significantly. Depletion regions will completely overlap when reverse biases are high enough.

TMBS and planar Schottky diodes have a similar electrical field distribution. Figure 8 shows the capacitance

Original 40A/100V SR Solution			Change to 40A/100V TMBS		
Input Voltage	90 Vac	100 Vac	Input Voltage	90 Vac	100 Vac
Iin (A)	1.56	1.39	Iin (A)	1.56	1.40
Pin (W)	140	139	Pin (W)	140	139
Vo (V)	20.2	20.2	Vo (V)	20.2	20.2
Io (A)	6.0	6.0	Io (A)	6.0	6.0
Po (W)	121	121	Po (W)	121	121
Efficiency %	86.4	87.1	Efficiency %	86.2	87.0

Table 2. Efficiency evaluation on 120-W adapter. The TMBS rectifier pair provides the same efficiency as the more complicated, more costly, and less robust synchronous rectification solution

Product Type		Industry 200V Planar Schottky (MBR20200CT)	Industry 200V Ultrafast Diode (STTH3002CG)	Vishay 200V TMBS (Experimental)
VR (V)	@ 1 mA/25'C	259	296	210
IR (mA)	@ 200V/125'C	0.10	0.01	6.70
VF (V)	@ 5A/125'C	0.57	0.64	0.53
VF (V)	@ 15A/125'C	0.69	0.80	0.65
IRR (A)	5A, -300A/us, 100V, 10%, 125'C	7.2	7.0	4.7
TRR (nS)		33	29	25
QRR (nC)		122	104	60

Table 3. Comparison of electrical characteristics for the experimental 200-V TMBS rectifier and 200-V planar schottky rectifier and ultra-fast diode.

of Vishay TMBS and a planar Schottky having the same chip size. We can see that the C_J of the 100-V TMBS is close to that of the planar Schottky rectifier for reverse bias voltages over 30 V. However, since TMBS has a higher current density, a smaller chip with lower capacitance may be used for a particular application.

So far, benchmark and application tests have focused on TMBS products with a 100-V reverse bias voltage. However, 120-V products have been developed and released for applications that see higher voltage spikes and where a 100-V rated product might provide inadequate headroom to ensure long-term reliability. These 120-V products offer current ratings from 15 A to 60 A and are offered in the ITO-220, TO-220, TO-262, TO-263, and TO-247 packages.

200-V devices are the next stage for TMBS rectifiers. The devices are currently under development, and the preliminary test results as described in Table 3 have been very encouraging,

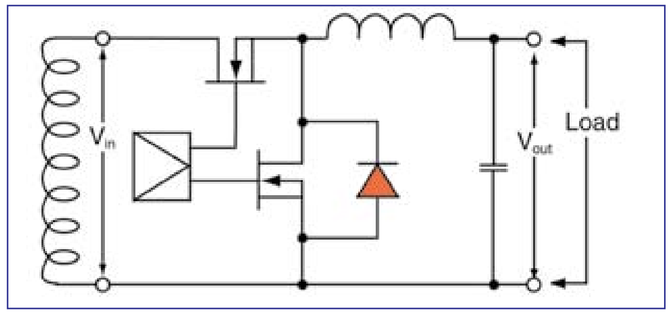

Figure 9. MOSFET implementation of synchronous rectification.

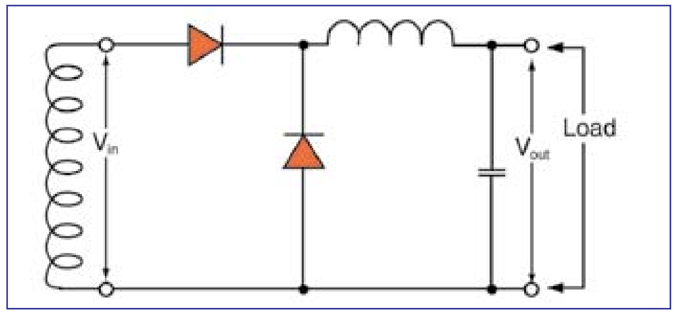

Figure 10. Alternate circuit using TMBS.

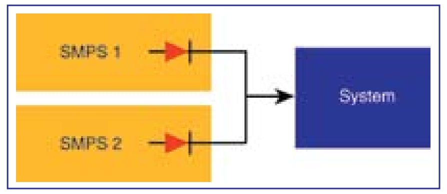

Figure 11. Redundant power supply used in a high-reliability power system with OR-ing diodes.

showing that the TMBS rectifier provides lowest on-state voltage drop compared to the industry-benchmark 200-V planar Schottky rectifiers and 200-V ultra-fast p-n junction diodes. The comparison underscores the switching performance advantages of the TMBS rectifier.

In addition to offering half the stored charge of industry-benchmark devices, the peak switching reverse recovery current (I_{RR}) of TMBS rectifiers is also 34% lower by comparison. This low I_{RR} will contribute to the lower switching losses of the transistor switches and improve the power conversion efficiency of the complete circuit, particularly in designs with switching frequencies above 300 kHz. The first 200-V rated TMBS rectifier has been released in Q4, 2006.

Advantages of TMBS Over Planar Schottky in Rectification Applications

As demonstrated in Table 1, the lower forward voltage drop and faster switching speed of the TMBS allow switch mode power supplies to achieve higher efficiency operation. The performance comparisons above (see Table 2) also show that TMBS achieves the same efficiency as a MOSFET synchronous rectifier in a 120-W adapter application, but at a lower cost. This application will be discussed further below, as well as other applications for the TMBS.

Due to the higher efficiency and better thermal performance of low on-resistance MOSFETs, synchronous rectification circuits have used them instead of planar Schottky rectifiers. However, as we have shown, TMBS is a cost-effective alternative to MOSFET synchronous rectifiers. Furthermore, TMBS offers the better performance in low output current devices such as adapters and open-frame power supplies. Synchronous MOSFET rectifiers may indeed provide good performance in high-current rectification applications, but the percent of MOSFET switching losses grows higher in the total power loss at output rectification in small current applications.

In addition, by requiring complex circuitry to control it, the MOSFET creates additional failure risks that can reduce the reliability of power supply systems. Therefore, low-V_F TMBS rectifiers are more suitable for lower-current adapters and open frame power supply designs. The performance of TMBS can compete with MOSFET in lower-current rectification applications and enjoys the advantages of shortened design cycles and lower production costs by requiring no additional control circuits. A block diagram showing a MOSFET implementation of synchronous rectification is shown in Figure 9, and an alternate circuit using TMBS is shown in Figure 10. As illustrated in these two figures, a single TMBS diode may replace the MOSFETs and drive circuit, thus simplifying the circuit significantly.

Diodes for redundant power supplies used in high-reliability power systems (Figure 11) are called OR-ing diodes, which are widely used in computer servers and telecommunication systems. The OR-ing diode at SMPS2 must have a reverse breakdown voltage greater than the output voltage of SMPS1 in order to protect SMPS1. It must also have a low reverse leakage current. However, if SMPS1 malfunctions and shuts down and SMPS2 turns on, it is important that the OR-ing diode have a low forward voltage drop to minimize power losses from SMPS2.

In high-reliability power systems, the system is protected from a shutdown resulting from malfunctions in one of the power supplies by having redundant power supplies share electrical loads. The design aims to isolate the failed SMPS from the common bus if an SMPS failure occurs, and thus requires a switch to isolate the failed SMPS. This switch must be highly sensitive and able to react with high interrupt speed when an SMPS fails; but it must also have low conductivity for big transient loads.

For OR-ing functions in isolated redundant power supplies, TMBS diodes offer significant improvements over conventional diodes. Low-$r_{(DS)on}$ MOSFETs (OR-ing FETs) are sometimes used in these applications. However, OR-ing FETs have a lower turn speed than OR-ing diodes, which may cause undesirable 0.8-V to 1.5-V voltage drops by the body diode of the OR-ing FET after it is tripped by high-transient voltage changes from high loading to low loading. The more reliable redundant-power-system design is to use one OR-ing FET in parallel with one low-V_F Schottky diode. The 100-V TMBS Schottky diode offers an outstanding design solution in telecom redundant power systems.

Another advantage of TMBS diodes is a higher reverse energy capability, allowing them to better withstand transients when power supplies switch on. The unique trench well structure and silicon bulk in the TMBS absorb and dissipate more avalanche energy than the plain interface structure of conventional planar Schottky rectifiers. This ability to enable higher reverse avalanche energy makes the TMBS more suitable for use in high-ESD or rectification applications than the OR-ing diodes in hot-plug systems and diodes in SMPS. The average 8-µs by 20-µs reverse surge energy of the VTS40100CT is about 170 mJ, which is about two times that of conventional planar Schottky diodes under the same testing conditions.

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Design Considerations for Compact and Highly Flexible Power Supplies

Can you afford to compromise?

XP Power explains the options and just what it takes to design a single-board, compact AC/DC power supply that can be easily adapted to suit multiple applications.

By Gary Bocock, Technical Director, XP Power, Pangbourne, United Kingdom

Many electronic systems require DC power rails outside the standard 3.3, 5, 12, 24 and 48V ratings, or require combinations of outputs not available from standard off-the-shelf products. Further, where multiple products or product variants are produced there are often differing requirements for each type. Commissioning custom designs can be an expensive, risky and lengthy process, especially in medium volume applications. In higher power applications modular, configurable power supplies are available from a number of vendors but these tend to become uneconomic below 300-350W. Many applications require 100-200W and these solutions are too expensive and typically too large.

One answer to the problem is to design a very flexible product range giving the user the opportunity to get the power they need with minimal compromise and minimal risk to their programme.

Flexible design, from a power supply perspective, means flexibility in mechanical options, electrical options, output ratings and configurations, and careful consideration to agency requirements and manufacturing.

Mechanical Flexibility

Some applications require open frame power supplies in this power range, others are better served by U-channel or chassis mount construction. Some will require a safety cover; some will have internal fan cooling while others will require a complete sub-assembly with integral cooling. Some systems will be required to be entirely convection cooled due to noise or maintenance concerns. These issues need to be considered from the outset of the design from the PCB through thermal management and mechanical parts, as this level of flexibility is difficult to add later. Figure 1 shows 3 of the 4 mechanical versions of the same standard power supply platform, XP Power's RCL175 AC/DC switcher.

Connection to the power supply can be a key consideration depending on the volume of products to be manufactured. For simplicity and cost, screw terminals will usually be the preferred method in low volume products. For medium & higher volume products push fit connectors – usually PCB headers – offer the benefit of faster system assembly and reduced risk of interconnection errors. Designing the power supply PCB to accommodate both options adds flexibility in this area.

Thermal considerations

Cooling arrangements and environmental requirements differ considerably from application to application so a flexible power supply design needs to maximise efficiency, minimise size to ease integration, minimise waste heat in the end application, and maximise lifetime. The aim is to maximise power density with a high convection-cooled rating and minimise forced cooling requirements to obtain higher power levels from one flexible product. Products requiring 20CFM and above can present a huge challenge for the system designer, especially as systems and equipment continue to shrink and audible noise levels come under pressure. 10 – 12 CFM is much more achievable without incurring high costs and the resulting moderate levels of audible noise can be easily managed. The combination of a substantial convection cooled rating and higher power force-cooled ratings also allows the use of variable speed or thermally controlled fans. These operate only at higher ambient temperatures or under high system load, enhancing reliability and further reducing the audible noise.

Figure 1: Mechanical flexibility means a range of packaging and interconnection options.

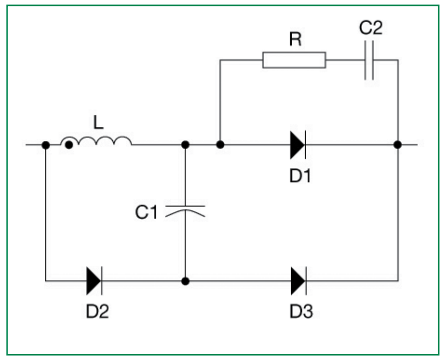

Figure 2: Traditional rectifier and snubber circuits like these can be replaced with a single SiC diode, saving board space and reducing design complexity.

Efficiency and topology issues

Maximising efficiency starts with the power factor correction (PFC) stage. Here, the availability of silicon carbide diodes for this application benefits efficiency and reduces component count at a similar cost to traditional diodes and their associated snubbing components (Figure 2).

The choice of power converter topology for a flexible product, designed to perform in a variety of applications, is important. The fly-back converter is often the topology of choice in the 100-200W range but does have some limitations. The power throughput is limited by the size of the transformer and hence the ability to provide peak power to complex loads such as motors, solenoids, lamps, downstream dc/dc converters and systems with large amounts of capacitance is also limited.

Other topologies, such as forward or half bridge converters have a transformer size limited only by temperature rise and are therefore capable of providing peak load requirements which occur on a momentary basis or during power up. The half bridge converter has further advantages over the forward converter. It brings a reduction in transformer size and allows the use of schottky barrier rectifiers in the higher output voltage rails further enhancing overall efficiency. The use of a coupled output inductor also enhances control of auxiliary output voltages over wide load variations.

Output considerations

Many applications require multiple outputs and combinations of positive and negative polarity. Keeping outputs isolated from one other allows flexibility in connection to provide such combinations, as well as allowing parallel or series connections to provide higher output voltages or increased output current. Isolated outputs also provide the facility for separate returns. These may be desirable for digital and analogue circuits.

To allow the power supply to be easily configured to a specific requirement, the full range of outputs must be considered at the outset; designing for both the highest voltage and the highest current is key and requires care to avoid compromising overall performance. Typical requirements fall into the range from 3.3V to 60Vdc, higher output voltage requirements being served by the ability to connect outputs in series. The challenge is to provide real flexibility in output voltages without unnecessary complexity or additional post-regulation stages that increase cost and reduce efficiency. Here a fractional turn transformer (FTT) can provide an effective solution.

Standard transformers are able to offer 1/2 turns by using E shaped cores, this not only severely restricts the choice of output voltages but can lead to problems with balancing and regulation. XP have used a different approach when designing the RCL175. This uses a separate transformer just for fractional turns, allowing the main transformer to deal only with integer turns where it is more efficient, smaller and provides better regulation.

The FTT provides significant advantages in multiple output supplies in terms of space saving, power transformer optimisation, cost cutting and efficiency.

Take a power supply requiring outputs of 5V and 12V. Ideally the 5V winding will be a single turn on the power transformer but the requirement for the 12V winding becomes 2.3 turns which cannot be readily achieved. The normal solution is to increase the 5V winding to 2T and then increase the 12V winding to 5T, by using diodes with differing forward volt drops an approximate 12V output can be realised. This means that the transformer size and losses are compromised, particularly as the lower voltage windings are typically copper foils and the diodes are not optimised for minimum losses.

Another common scenario in many applications is the need for 3.3V and 5V output combinations. The FTT largely eliminates cross regulation and, with suitable voltage sensing and control, there is no need for the post regulation usually employed to regulate the 3.3V output. This approach removes cost, enhances efficiency and reduces size. The principle is illustrated in Figure 3.

Safety and EMC

The power supply is critical when it comes to achieving the necessary safety agency approvals and compliance with electromagnetic compatibility requirements in any system.

The ideal scenario for a flexible power supply is to carry approvals for IT, industrial and medical applications, and allow for both class I (with a protective earth) and class II (without a protective earth) systems. The ability to deal with both class I and class II

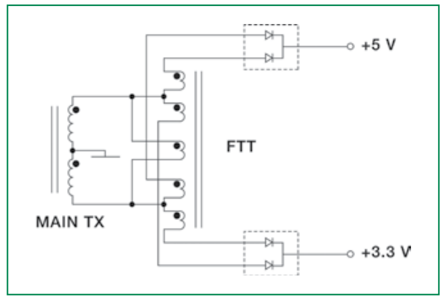

Figure 3: The FFT transformer removes cost, enhances efficiency and reduces size in multi-output power supplies.

applications is increasingly important in worldwide markets and as medical equipment in the home and residential clinics is becoming commonplace and ground connections are not always as good as they should be. This demands careful consideration of EMI filtering, PCB layout and topology to meet the requirements for increased creepage and clearance, reduced leakage current and non-earthed systems while maintaining compliance with international emissions and susceptibility standards. With appropriate design & component selection, it is possible to achieve compliance with level B conducted emissions, level A radiated emissions and level 3 susceptibility requirements.

Manufacturing

The key consideration for manufacturing is to design the power supply on a single PCB covering all requirements. This minimises both cost and delivery times and allows part built assemblies to be configured to the application in a short time frame without compromising agency approvals. The potential to configure modified standards in a short time, produce pre-production quantities on a short lead time and manufacture volume requirements in a low cost area is a key consideration in the initial design phase.

Agency approvals

One of the most significant delays in bringing new equipment or systems to market can be gaining the relevant agency approvals. With the right approach to design, safety testing & part numbering it is possible to gain approval for a wide range of potential output voltages and configurations without applying for re approval for each variation. This approach saves cost and, more crucially, saves significant time in removing the need for additional approval cycles of the power supply during equipment and system development.

Sidebar

All of the techniques described in this article have been combined in XP Power's RCL175 series shown in figure 1. The basic specification:

- 1-4 outputs
- Universal AC input with Active PFC
- Up to 120W convection cooled, 175W with 12CFM
- Common PCB's for any potential variation
- Compact 3.7 x 5.5 footprint
- Agency approved for output voltage to 60Vdc on individual outputs
- Industrial, IT & medical agency approvals
- Class I & class II safety approvals
- Level B conducted & level A radiated emissions
- Four optional mechanical/cooling formats
- Choice of PCB header or screw terminal connectors
- Options for conformal coating, overload characteristics & remote inhibit/enable

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Higher Efficiency Drives Incandescent Lamp Replacement

Compact fluorescent lamps last longer and are cheaper to run

As European and US legislation increasingly insists on better power efficiency, semiconductor designers are again called to the rescue. Initial cost is an issue. Fairchild use their power expertise to find the solution.

By Vajapeyam Sukumar, Applications Engineering, Fairchild Semiconductor, Austin TX

The European Union has a long tradition of being pioneers in energy conservation. A highly visible example of this is the replacement of incandescent lamps across the nations of the EU with the more efficient, longer lasting Compact Fluorescent Lamps (CFL). Over the last two decades, European engineers have helped make the CFL so popular due to a relentless drive to reduce the cost of Compact Fluorescent bulbs. Their significantly longer life and the dramatic power savings have helped the CFL compete with the standard incandescent bulb. However, the very low initial purchase cost of the incandescent meant that the pressure to reduce the cost of the CFL is the single most important factor in the development of this technology. The advent of higher quality, low-cost bipolar transistors in the late 1980s and early 1990s has made the CFL ubiquitous.

The typical Compact Fluorescent Lamp has a schematic that is similar to that shown in Figure 1. The major challenge here is the choice of the right bipolar transistors. The operation of the circuit is simple. The saturable cores in the base of the transistors help turn the transistors off alternatively. The challenge is to make sure that the transistors have turn-off times very close to each other to prevent heating up of the slower transistor, which, in turn, could lead to over temperature issues. Today, the majority of the Compact Fluorescent Lamps still use bipolar transistors. The fact that a 20W CFL produces about as much light as a 100W incandescent lamp, the high overall efficiency of the circuit and the relatively high rectified AC mains voltage means that the maximum current in these bipolar junction transistors is well below 0.5A.

Over the years, sorting techniques ranging from gain sorting to more sophisticated methods such as 'Vx' measurement have evolved. These sorting algorithms have attempted to use static measurement techniques to sort transistors with similar fall times. Static test methods are preferred by transistor manufacturers because of the testing speed and repeatability. Bipolar transistor processing techniques such as electron irradiation succeeded in reducing the spread of the fall and storage times by decreasing the turn-off times. The dramatic development in semiconductor process technologies has the potential to result in greatly improved bipolar transistors but it is the high cost of initial investment and the thin profit margins coupled with the replacement of bipolar transistors with other power semiconductors in other applications that have prevented any major radical improvement in the bipolar transistor. The introduction of bipolar transistors for CFL markets in the low cost signal transistor packages has, in recent years, helped decrease costs. A typical example is the FJN3303 where a 400Vceo/700Vcbo 0.5A transistor targeted at CFL applications is placed in the lowest cost package for the die size – the TO-92 through-hole package.

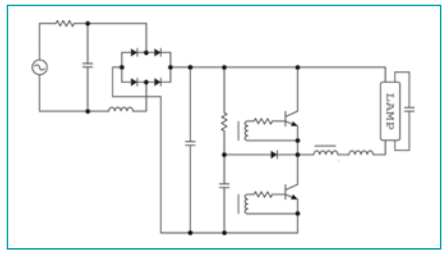

Figure 1: A simplified Compact Fluorescent Lamp ballast schematic.

Figure 2: The FAN7710 greatly simplifies the circuitry comprising the Compact Fluorescent Lamp.

Alternative power switches to the power bipolar transistor are the power MOSFET and the IGBT. The power MOSFET has been popular in CFL applications during the last decade. The range of options for the CFL designer has increased with the introduction of super-junction or charge balanced MOSFETs during this period. One challenge with the use of power MOSFETs has been the drive scheme. The last decade has also seen the development of high voltage (around 500V) P-channel MOSFETs specifically for use in CFL lamps. While the P-channel MOSFETs have a higher specific resistance than N-channel high voltage MOSFETs, the ease of drive has kept the P-channel MOSFETs as a viable alternative to the conventional N-channel MOSFETs in CFLs. The IGBT could be ideally suited for the application especially since the optimum switching frequency for CFLs today is in the range of around 35kHz. However, as noted above, it is commercial reasons rather than technological ones preventing the popularity of alternatives to the traditional bipolar transistor.

Due to its history as an incandescent bulb replacement, we tend to think of the CFL as a throw-away electronic assembly. But, cost and environmental factors can couple with better designs to boost the market for replaceable bulb CFLs. The very tight space constraints in the PCB found inside the CFL also favor solutions such as either a hybrid or a monolithic solution. One recently introduced monolithic integrated circuit, Fairchild's FAN7710, seeks to combine sophisticated protection and pre-conditioning functions as well as two power switches in a low cost DIP-8 package. Using a 600V Bipolar-CMOS-DMOS (BCD) process, the FAN7710 allows the user to set pre-heating and switching frequency.

The most impressive advantage of the FAN7710 is the ability to simplify design and minimize the Bill of Materials(BOM) while, at the same time, adding protection and reliability features that are very difficult to implement discretely (Figure 4). For example, the FAN7710 has an internal over-temperature shutdown function that monitors the junction temperature of the power switches and, within micro-seconds of detecting an over-temperature condition, shuts down the entire circuit. Implementing this feature discretely is expensive if at all possible.

Another advantage of the integrated approach is that it is possible to control the dead time during the operation to make sure that the MOSFETs switch at zero voltage every switching cycle. Eliminating the switching losses from MOSFETs helps to reduce the silicon area of the MOSFET and directly reduces the cost of the CFL solution. The same functional block that implements the dead time control and ensures ZVS (Zero Voltage Switch) also can detect an open lamp condition and, in turn, shut the ballast down. In fact, there are several abnormal conditions that can be detected by this sub-circuit – either the lamp is not inserted right, one lamp electrode may be broken or a deactivated lamp.

One of the most important needs for a CFL controller is the way the drive scheme for the high side MOSFET is implemented. High voltage bridge drivers for lamp ballasts as well as other power electronic applications such as power supplies and motor drives have become increasingly popular over the last decade. The major drawback of most of the earlier BCD processes was the parasitic high voltage transistor that could be turned on by high dv/dt which, in turn, limited the maximum switching frequency to less than 40kHz. Due to careful process and chip design, the switching frequency of the FAN7710 is able to exceed 100kHz. In fact, the minimum dead time control specification of 0.8µs is the gating item for the maximum switching frequency.

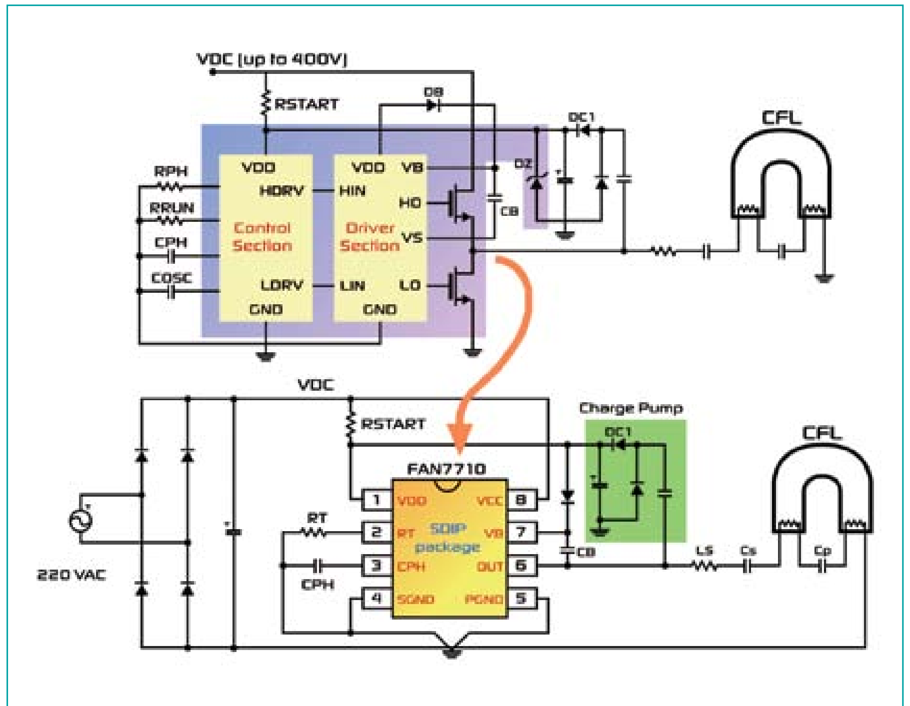

Figure 3: Showing the simplification of the CFL schematic as the FAN7710 replaces a discrete MOSFET solution.

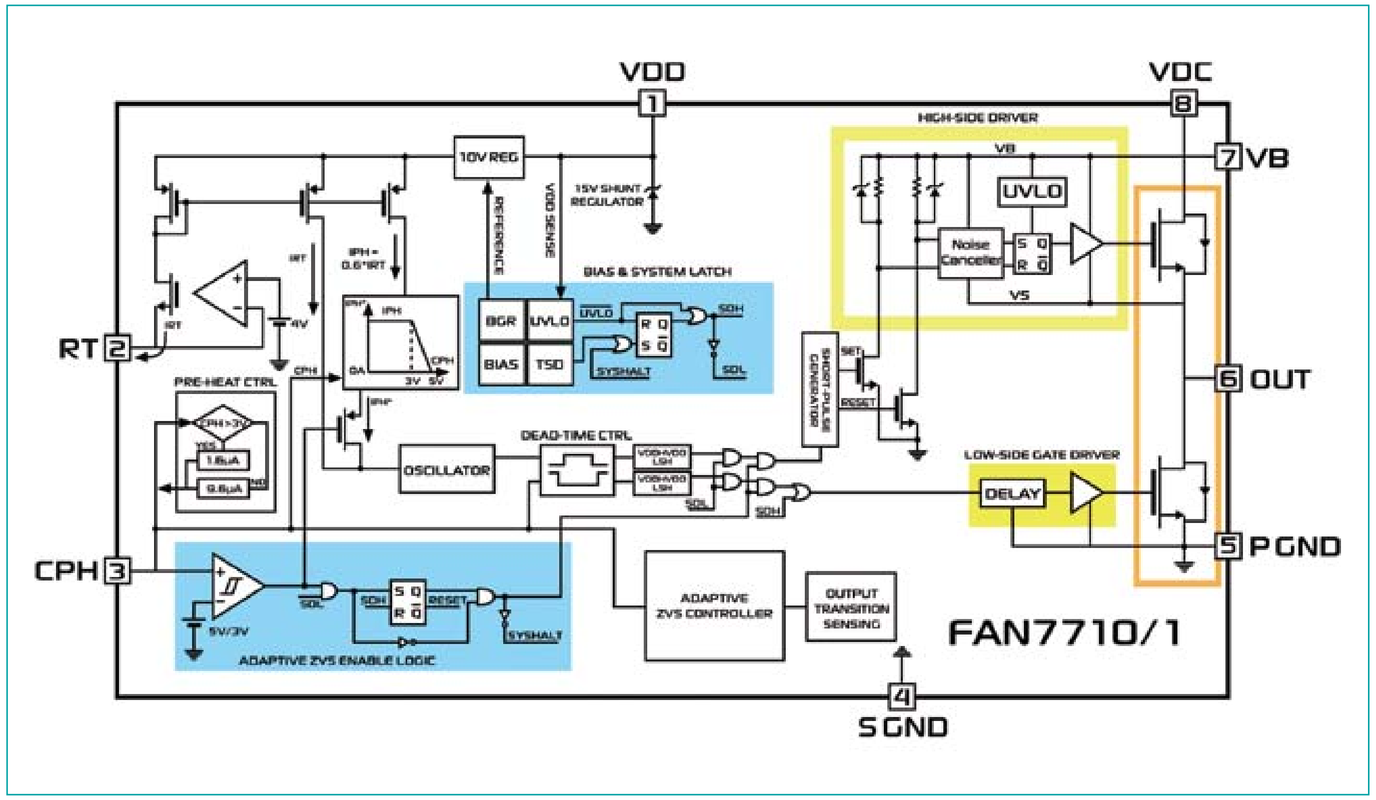

Figure 4: Block Diagram of the FAN7710.

The FAN7710 can be programmed by two external components, simplifying the design. The CFL switching frequency can be programmed by a single resistor. A switching frequency that is user programmable is necessary for optimizing efficiency and performance to match the characteristics of the lamp being switched.

Modern CFL lamps also require preheating before ignition. The FAN7710 circuit only needs a single capacitor to program the time in pre-heat and in doing so, meet the requirements of IEC929.

The micro-power start-up circuit that incorporates a shunt regulator helps eliminate the need for a separate IC start-up circuit for the FAN7710. The current draw is only 120µA off the rectified ac mains voltage at start up. The operating current is in the range of 2.7mA maximum.

Realizing the monolithic integrated solution in the BCD process has its limitations. While the overall schematic is greatly simplified by the monolithic design, one can make power MOSFETs more area efficient if a discrete power MOSFET process is used. While these integrated processes do an excellent job of realizing complex circuitry involving both high voltage and low voltage transistors, the $R_{DS(ON)}$ per unit area of the BCD MOSFETs are approximately twice that of an equivalent discrete transistor. Consequently the FAN7710 and similar designs are limited to around 20W applications for 240Vac input. If higher power CFLs are needed, it is recommended to use external discrete MOSFETs (especially charge balanced 600V MOSFETs such as Fairchild's SuperFET^{TM} MOSFETs) along with a controller IC. The FAN7711, for example, has the controller section of the FAN7710 but with MOSFET drivers replacing the integrated MOSFETs of the FAN7710. The fluorescent lamp ballast built using the FAN7711 is, therefore, capable of handling over 100W due to the external power MOSFETs. So, the FAN7711 can be used not only for Compact Fluorescent lamp designs but also in electronic ballasts for tubular fluorescent lamps.

The FAN7710 is representative of a new class of inexpensive, highly integrated circuits for Compact Fluorescent Lamp ballasts. Careful process and device design has the potential to increase efficiency and will result in higher wattage ballasts in the future.

As the global concern for energy conservation grows and stricter energy regulations are mandated, the market for CFLs will continue to increase. This will drive the need for more sophisticated ICs in small form factors.

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Threshold Voltage Thermal Coefficient (TVTC) in Power MOSFETs

Theoretical study, measures and simulation

TVTC is a very important parameter for a Power MOSFET to be safely used in linear zone operation modes. Find out how TVTC can be calculated and how certain thermal processes affect TVTC with a comparison between the simulated and the real data.

By Giuseppe Consentino, STMicroelectronics, Catania, Italy

In some applications, as audio amplifiers and fans, Power MOSFETs work in linear zone. A MOSFET works in linear zone when high voltage is applied on drain-source pins and high current passes through the device. When working in linear zone, Power MOSFETs could fail if a thermal run-away phenomenon occurs due to a drain current focalization (hot spots phenomenon). The failure depends on the Power MOSFET internal structure. In fact, the importance of physical device parameters such as channel length and width or the thickness of the gate oxide is well known. TVTC is one of the important elements that could cause the Power MOSFETs' failure. TVTC is the result of the derivative of Power MOSFETs threshold voltage against temperature. TVTC is a negative coefficient because an increase in temperature is followed by a decrease in threshold voltage. The MOSFET could become thermally instable and thus fail if the absolute value of TVTC increases. To understand if a Power MOSFET can safely be used in linear zone, it is necessary to consider a device with a very low TVTC absolute value. To address designers, it is necessary to establish a theoretical expression for TVTC.

MOS structure

It is well known that a MOS structure is composed by three layers: a top heavily doped polycrystalline silicon layer, a middle insulator (usually SiO_2) layer and a bottom semiconductor layer. Considering an ideal MOS system with a p-doped semiconductor, the energy band diagram can be depicted as in fig. 1.

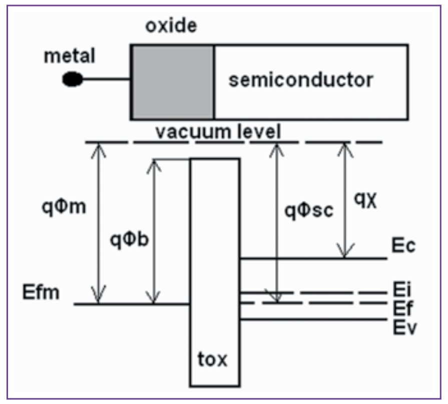


Fig. 1: Energy band diagram of an ideal MOS capacitor under thermal equilibrium.

$q\Phi_m$ is the work function, $q\Phi_B$ is metal-to-oxide barrier energy, $q\Phi_{sc}$ is the work function of the semiconductor, $q\chi$ is the energy difference between the vacuum level and the conduction band edge.

When a small positive bias is applied to the gate, holes are pushed away from the oxide interface and create a depletion layer in the semiconductor consisting of the negative charges due to the acceptor ions (Q_s):

$$Q_s = -qN_aW \quad (1.1)$$

N_a is the acceptor concentration and W is the width of the surface depletion layer.

Increasing the gate voltage causes the bands to bend downward until E_i (the intermediate level energy between the conduction and the valence bands) equals to E_F (the Fermi energy level) at the surface. In this condition, at the interface near the oxide, the semiconductor becomes intrinsic.

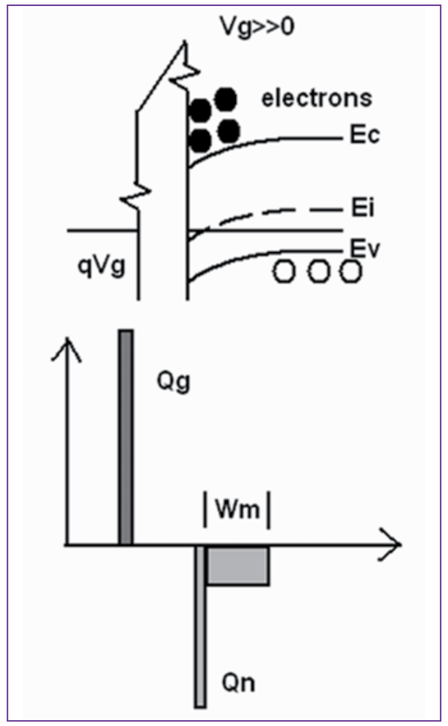


Fig. 2: Energy band diagram and charge distribution in an ideal MOS capacitor in inversion condition.

By increasing the gate voltage again, E_i crosses E_F, and thus the minority carriers, in this case the electrons, are attracted to the oxide-semiconductor interface. In this new condition, the surface layer contains more electrons than holes and it becomes of n-type (inversion layer) (see fig.2).

Now, Q_s can be written as:

$$Q_s = -Q_n - qN_aW \quad (1.2)$$

Q_n is the inversion layer charge.The electron and hole concentrations on the bulk semiconductor for non degenerate silicon can be written as:

$$n_0 = n_i e^{\left(\frac{E_F-E_i}{kT}\right)} = n_i e^{-\left(q\frac{\phi_F}{kT}\right)} \quad (1.3)$$

$$p_0 = n_i e^{-\left(\frac{E_F-E_i}{kT}\right)} = n_i e^{\left(q\frac{\phi_F}{kT}\right)} \quad (1.4)$$

n_i is the intrinsic electron concentration, E_i is the intrinsic Fermi level, E_F is the Fermi level, k is the Boltzmann constant equal to 1.38×10^{-23} J/K and Φ_F is the Fermi potential.

For n-channel devices with N_a acceptor (1.4) becomes:

$$N_a = n_i e^{-\left(\frac{E_F-E_i}{kT}\right)} = n_i e^{\left(q\frac{\phi_F}{kT}\right)} \quad (1.5)$$

Now, it is possible to achieve Φ_F as:

$$\Phi_F = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) \quad (1.6)$$

For an intrinsic silicon, n_i can be written as:

$$n_i = 3.88\times10^{16}T^{\frac{3}{2}}e^{-\left(\frac{E_{go}}{2kT}\right)}$$
$$= 3.88\times10^{16}T^{\frac{3}{2}}e^{-\left(\frac{7023}{T}\right)}[cm^{-3}] \quad (1.7)$$

The electron and hole concentrations near the surface semiconductor can be written as:

$$n_s = n_0 e^{-\left(\frac{E_{is}-E_i}{kT}\right)} = n_0 e^{\left(q\frac{\Phi_s}{kT}\right)} \quad (1.8)$$

$$p_s = p_0 e^{\left(\frac{E_{is}-E_i}{kT}\right)} = p_0 e^{-\left(q\frac{\Phi_s}{kT}\right)} \quad (1.9)$$

When Φ_s is equal to Φ_F the semiconductor surface becomes intrinsic. Instead, by increasing again Φ_s, the layer becomes of n-type. When n_s equals to p_0 a "strong inversion" occurs and the minority carriers at the surface equal the majority carriers at the bulk. The potential condition for the strong inversion occurs when:

$$\Phi_s = 2\Phi_F \quad (1.10)$$

V_G can be written as:

$$V_G = V_{OX} + \Phi_s \quad (1.11)$$

The MOS capacitance can be written as:

$$C_{OX} = \varepsilon_{OX}\frac{A}{t_{OX}} = -\frac{Q_s}{V_{OX}} \quad (1.12)$$

ε_{ox} is the oxide permittivity (34.5×10^{-12}F/m), t_{OX} is the oxide thickness and A the area. Considering (1.12), V_{OX} can be written as:

$$V_{OX} = -\frac{Q_s}{C_{OX}} \quad (1.13)$$

and the gate voltage as:

$$V_G = -\frac{Q_s}{C_{OX}} + \Phi_s \quad (1.14)$$

Thus, V_G can be rewritten as:

$$V_G = \frac{qN_aW}{C_{OX}} + \Phi_s \quad (1.15)$$

Considering the Poisson equation, it is possible to obtain:

$$rot\mathrm{E} = \frac{qN_a}{\varepsilon_s} = \nabla^2\Phi \quad (1.16)$$

ε_s is the silicon permittivity (105.4×10^{-12}F/m). Thus, it is possible to achieve:

$$\Phi_s = \frac{qN_aW^2}{2\varepsilon_s} \quad (1.17)$$

the depletion layer width can be written as:

$$W = \sqrt{\frac{2\varepsilon_s\Phi_s}{qN_a}} \quad (1.18)$$

V_G will become:

$$V_G = \frac{\sqrt{2\varepsilon_s qN_a\Phi_s}}{C_{OX}} + \Phi_s \quad (1.19)$$

The gate voltage at the strong inversion condition is called the V_{TH} threshold voltage of the MOSFET and it can be written as:

$$V_{TH} = \frac{\sqrt{4\varepsilon_s qN_a\Phi_F}}{C_{OX}} + 2\Phi_F \quad (1.20)$$

In the real MOS structure, when no voltage is applied on the gate, the existing difference between metal and semiconductor work functions, Φ_{ms}, cause opposite charges to accumulate along the oxide interfaces. In this article the charges inside the oxide will be neglected.

In order to consider the effect of Φ_{ms} on the threshold voltage it is necessary to take into account the follow formula (1.21):

$$V_{TH} = \Phi_{ms} + \frac{Q_{OX}}{C_{OX}} + t_{OX}\frac{\sqrt{4\varepsilon_s qN_a\Phi_F}}{\varepsilon_{OX}} + 2\Phi_F$$

Q_{OX} is the charge inside the oxide.

In modern devices the gates are in polysilicon material. For n-type gate and p-type semiconductor, ms can be written as:

$$\Phi_{ms} = -\frac{kT}{q}\ln\left(\frac{N_gN_a}{ni^2}\right) \quad (1.22)$$

N_g is the doping level of the polysilicon.

TVTC can be thus achieved deriving (1.21) versus the temperature:

$$\frac{\partial V_{TH}}{\partial T} = \frac{\partial\Phi_{ms}}{\partial T} + t_{OX}\frac{\sqrt{\varepsilon_s qN_a}}{\varepsilon_{OX}\sqrt{\Phi_F}}\frac{\partial\Phi_F}{\partial T} + 2\frac{\partial\Phi_F}{\partial T} \quad (1.23)$$

Φ_{ms} thermal coefficient can be written as:

$$\frac{\partial\Phi_{ms}}{\partial T} = -\frac{k}{q}\ln\left(\frac{N_gN_a}{ni^2}\right) + \frac{2kT}{qni}\frac{\partial ni}{\partial T} \quad (1.24)$$

and thus:

$$\frac{\partial\Phi_{ms}}{\partial T} = \frac{\Phi_{ms}}{T} + \frac{2kT}{qni}\frac{\partial ni}{\partial T} \quad (1.25)$$

Deriving (1.7) versus T, it is possible to achieve:

$$\frac{\partial n_i}{\partial T} = \frac{n_i}{2T}\left[3 + \frac{E_{go}}{KT}\right] \quad (1.26)$$

Replacing (1.26) in (1.25), it is possible to achieve:

$$\frac{\partial \Phi_{ms}}{\partial T} = \frac{\Phi_{ms}}{T} + 3\frac{K}{q} + \frac{E_{go}}{qT} \quad (1.27)$$

Now, taking into account (1.6), the Fermi voltage thermal coefficient can be written as:

$$\frac{\partial \Phi_F}{\partial T} = \frac{K}{q}\ln\left(\frac{N_a}{n_i}\right) - \frac{KT}{qn_i}\frac{\partial n_i}{\partial T} \quad (1.28)$$

and replacing (1.26) in (1.28), it is possible to achieve:

$$\frac{\partial \Phi_F}{\partial T} = \frac{\Phi_F}{T} - \frac{3}{2}\frac{K}{q} - \frac{E_{go}}{2qT} \quad (1.29)$$

TVTC, thus, can be rewritten as:

$$\frac{\partial V_{TH}}{\partial T} = \frac{\Phi_{ms}}{T} + 2\frac{\Phi_F}{T} + t_{OX}\frac{\sqrt{\varepsilon_s q N_a}}{\varepsilon_{OX}\sqrt{\Phi_F}}\frac{\partial \Phi_F}{\partial T} \quad (1.30)$$

Some considerations on V_{TH} and TVTC equations and real examples

Considering (1.21), it is possible to see that V_{TH} is the sum of three components: Φ_{ms} (negative for n-type polysilicon and p-type substrate - positive for p-type polysilicon), two times Φ_F (positive for p-type silicon) and the oxide voltage drop (positive for a p-type silicon). TVTC, as described in (1.30), also depends on three components: Φ_{ms} divided by T, two times the Fermi potential divided by T and a term function of Φ_F thermal coefficient and other key parameters as the oxide thickness and the impurity body concentration (it is a negative term). Φ_{ms} divided by T and the term of Φ_F thermal coefficient results in a negative TVTC considering an n-type gate and p-type silicon. Instead, Φ_F divided by T results in a positive TVTC. As in (1.22), Φ_{ms} depends on the gate and silicon doping concentration and the intrinsic carrier concentration. Such term increases in absolute value if the gate or silicon doping concentration rises, while it decreases in absolute value when the temperature rises because of the intrinsic carrier concentration increase. Thus, to minimize Φ_{ms}, the gate and silicon doping concentration should be lowered. ΦF depends on the silicon doping and the intrinsic carrier concentration. When the silicon doping is increased, Φ_F also raises its value. When T increases, Φ_F decreases due to the intrinsic carrier concentration raise. To maximize Φ_F, it is necessary to increase the silicon doping concentration. Φ_F thermal coefficient depends on Φ_F divided by T minus a constant and another term function of the inverse of T. Its value is negative because the components with the minus sign are greater than the positive terms. When T increases, Φ_F thermal coefficient also increases in absolute value because Φ_F decreases. Thus, to minimize Φ_F thermal coefficient it is necessary to increase Na.

However, the third component of (1.30) also depends on the inverse square root of N_a, thus, considering the modern technology, this term increases in absolute value when the silicon doping concentration also increases. In modern devices, it is possible to observe that TVTC increases in absolute value when the doping concentration also rises because the first and third terms are greater than the second term in (1.30).

Another important parameter to establish TVTC is t_{OX}. It affects only the third term of (1.30). When t_{OX} decreases, the third term in (1.30) also decreases, leading to a decrease of the TVTC absolute value.

A real example of V_{TH} and TVTC is shown below to compare the data measured with the theoretical model. The device under testing is called Device1, an N-channel Power MOSFET. This device has 55V of breakdown voltage and 5mOhm of R_{DSON}. Considering the values of N_g, N_a, t_{OX} and L in (1.21) and (1.30), it is possible to achieve the following graphs for V_{TH} and TVTC versus of T. These graphs compare the simulated and the real electrical data.

The simulated and measured data match.

The device has 3.2V of V_{TH} and TVTC is around 3mV/K at 300K. In fig.5, all components of TVTC are highlighted versus T.

Conclusions

This article has studied the effect of temperature on the V_{TH} of a MOSFET and, in particular, on TVTC. Mathematical models for both parameters were studied and a comparison with the real measurements was performed taking in consideration the N-channel MOSFET named Device1. In fact, the simulated and real data match. The model proposed highlights that in order to decrease the absolute value of TVTC it is necessary to decrease the thickness oxide, the silicon and the gate doping concentration of the device. However, to minimize TVTC it is not possible to decrease all the mentioned parameters together because V_{TH} must have an established value. Thus, it is necessary to rearrange all the physical parameters to reach a trade off between V_{TH} and TVTC values.

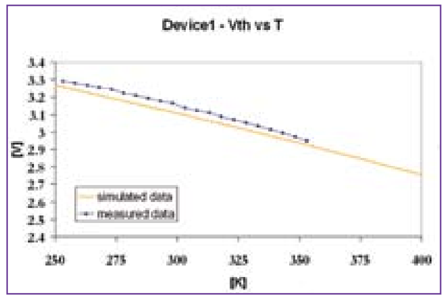


Fig. 3: VTH - Comparison between simulated and measured data for device1.

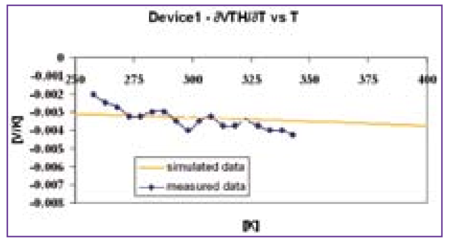


Fig. 4: TVTC - Comparison between simulated and measured data for device1.

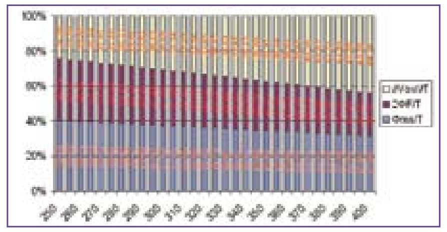
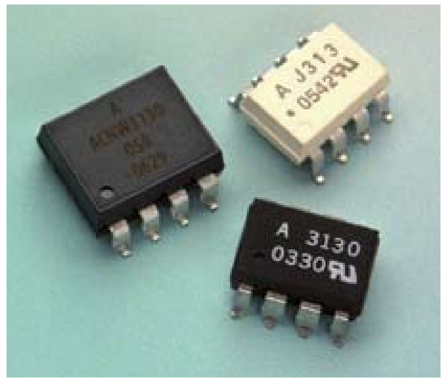


Fig. 5: TVTC components versus T.

www.stm.com

Gate Drive Optocouplers with highest Common Mode Rejection (CMR) Ratio



Avago has introduced three new gate drive optocouplers optimized for reliability and performance. As equipment manufacturers in industrial automation and data center power supply markets transition to developing more energy efficient products which require fast switching operation, Avago has engineered new optocouplers with the industry's highest common mode rejection (CMR) ratio (40 kV/µs @VCM=1500V).

CMR is the maximum slew rate of common mode voltage (VCM) which can be sustained, keeping the output in the correct logic state. CMR failure results in glitching on the output as either a positive or negative pulse. This key specification guarantees the reliable transfer of drive information at very high DC-link voltage and over fast switching operations.

Avago's new ACPL-3130, ACPL-J313 and ACNW-3130 gate drive optocouplers are ideal for applications such as isolated IGBT/ MOSFET-gate drives for industrial inverters, switching power supplies (SPS) and uninterruptible power supplies. The optocouplers deliver 2.5 A maximum peak output current. Additionally, the products support a wide operating voltage range (15 to 30 volts) required by gate-controlled devices.

As part of Avago's extensive range of high-performance, isolated, gate drive optocouplers, the ACPL-3130 contains a GaAs LED while the ACPL-J313 and ACNW-3130 contain an AlGaAs LED. The new optocouplers have received approval in accordance with the following safety standards: UL (pending), CSA (pending) and IEC/EN/DIN EN 60747-5-2.

www.avago.com

HVICs Save Space, Increase Reliability and Reduce Power Consumption

Fairchild Semiconductor has introduced industry-leading high-voltage gate driver ICs (HVIC) that feature an innovative common-mode dv/dt noise cancelling circuit for achieving excellent noise immunity. The FAN7383, FAN7384 and FAN73832 offer savings of at least 50 percent PCB area compared to optocoupler or pulse transformer-based solutions. Their high performance ensures superior system reliability and energy efficiency when compared to similar HVICs on the market. Fairchild's HVICs are the optimal solution for driving MOSFETs and IGBTs in a wide array of consumer and industrial applications up to 600V. These include inverter motor drives, switch-mode power supplies (SMPS) and electronic ballasts.

These HVICs feature advanced level-shift circuitry for industry-leading, high-side driver operation with negative VS swings of up to -9.8V (at VBS = 15V). This results in the devices' unique ability to eliminate an extra diode.

These devices feature lowest quiescent currents and temperature dependency and deliver full functionality in cold or hot ambient temperatures to guarantee stable performance in a wide range of applications.

Fairchild's HVICs feature a floating channel designed for bootstrap operation to +600V. They also increase reliability by providing under-voltage lockout (UVLO) on both channels, and an 11-20V supply range for VCC.

When combined with Fairchild's advanced MOSFETs, IGBTs and small-signal discretes, Fairchild's half-bridge gate drivers offer designers a complete half-bridge solution.

These lead (Pb)-free devices meet the requirements of the joint IPC/JEDEC standard J-STD-020C and are compliant with European Union regulations now in effect.

www.fairchildsemi.com/hvic

Product specifications:

Product	Output Current (milliamp)		Offset Voltage (V)	Quiescent Current (microamp)		Shut Down	Dead-Time Control	Short-Circuit Protection	Package
	Source	Sink		I_{QBS}	I_{QCC}				
FAN7383	350	650	600	35	650	Yes	Variable	No	14-SOP
FAN7384	250	500	600	50	600	Yes	Fixed	Yes	14-SOP
FAN73832	350	650	600	35	300	Yes	Variable	No	8-SOP/8-DIP

High-Performance Split-Core Current Transformers for Energy-Efficiency and Active Power Monitoring

LEM has introduced the TT series of compact split-core AC current transformers. These new devices feature an innovative core material to offer high performance at an attractive price.

The core material used in the transformers is a new type of ferrite with improved magnetic permeability, allowing accurate measurement of AC signals in a extended frequency range that includes 50/60Hz. The new transformers feature an absolute accuracy better than 1 percent at the nominal current and even better for lower primary currents. The ferrite material provides a linearity of better than 0.1 % even at very low levels, and the transformers have a very low phase shift between measured voltage and current of 1.5˚ ±1˚. The hard and dense core allows very small air gaps to be achieved and is virtually insensitive to ageing and temperature changes, in comparison with laminated FeSi or FeNi materials.

Two ranges of primary current measurement are available: 50A and 100A. The dimensions of the TT 50-SD are only 36.5 x 43 x 31.5 mm with an 8 mm diameter sensing aperture for non-contact measurement. The TT 100-SD measures 44.5 x 51 x 36.5 mm with a 16 mm diameter sensing aperture.

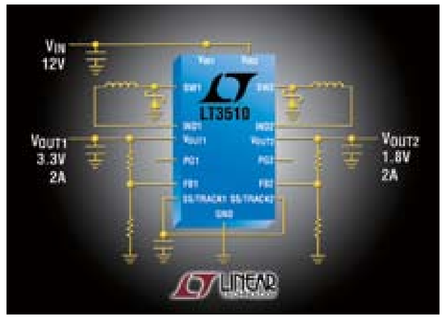
With a 3000:1 ratio, the TT 50-SD and TT 100-SD have low output currents (respectively below 16.66 mA or 33.33 mA). This, together with the internal output-protection circuit, guarantees safe and easy installation without the need to shut down operation since there is no risk of producing a high voltage surge when the transformers are opened, unlike 1A or 5A output products.

Being small, safe, self-powered and split-core, the TT current transformers are very easy to install andcommission. They are ideal for distributed measurement systems and can be retro-fitted into existing installations and non-interruptible equipment. Principal applications are in the field of energy sub-metering and cost allocation, dynamic consumption and peak analysis, energy waste or defective equipment detection and power quality control.

As with all LEM industrial products, the TT transformers benefit from high-quality standards and are backed by a five-year warranty.

www.lem.com

1.5MHz, 25V Dual 2A Step-Down DC/DC Converter



Linear Technology announces the LT3510, a dual current mode PWM step-down DC/DC converter with two internal 2.5A power switches packaged in a 20-lead TSSOP-20E package. Each channel is capable of delivering up to 2A of continuous output current at efficiencies up to 88%. Independent input voltage, feedback, soft-start and power good pins for each channel simplify complex power supply tracking and sequencing requirements. The LT3510's wide input range of 3.3V to 25V makes it ideal for regulating power from a wide variety of sources, including 5V and 12V rails, unregulated wall transformers, lead acid batteries and distributed power supplies. The LT3510's switching frequency is user programmable between 250kHz and 1.5MHz, allowing optimization between efficiency and external component size.

Both of the LT3510's converters are synchronized to either an external clock input or an internal oscillator and maintain a 180 degree phase offset between channels to reduce voltage ripple and input capacitor size. An internal 0.80V reference enables sub 1V output voltages, required to power the latest generation of low voltage DSPs and microcontrollers. Independent, sequential, ratiometric or absolute tracking is easily attained between the outputs. Low drop-out internal switches enable duty cycles to reach 95% while internal cycle-by-cycle current limit provides protection against shorted outputs. The low current (<10uA) shutdown offers extended run-time in battery-powered systems.

The LT3510EFE is available from stock in a thermally enhanced TSSOP-20 package. There is also an "I" Grade temperature version, the LT3510IFE.

www.linear.com

Tiny LDO Regulators Feature Excellent Transient Performance

National Semiconductor has introduced three low-dropout voltage regulators (LDOs) for digital and analog loads in portable, battery-powered systems such as medical equipment, navigation systems, handheld scanners, digital signal processing and microprocessor core supply applications.

The LP5951, LP3996 and LP5996 LDOs each feature typically less than 50 mV transient performance. The power supply rejection ratio (PSRR) of better than 60 dB reduces switching noise from the switching regulator to provide a clean output voltage.

The LP5951 is a 150 mA CMOS LDO voltage regulator which supports an input voltage below 2V and output voltage as low as 1.3V. It is well-suited for use in designs that require the post regulator to follow a switcher. When switched to shutdown mode via a logic signal at the enable pin, power consumption is reduced to virtually zero. The device is available in SOT-23 and SC-70 packaging and designed to be stable with small 0402 size ceramic capacitors with internal protection against short-circuit currents and over-temperature conditions.

Specified for -40 degrees C to 125 degrees C junction temperature, the device is available in fixed output voltages from 1.3V to 3.3V.

The LP3996 and LP5996 each pack two LDOs into a tiny 10-pin thermally enhanced LLP package measuring 3 mm x 3 mm. Using separate enable inputs, the dual outputs can be sequenced to ensure that the input/output (I/O) of a processor is powered before its core. In addition, the LP3996 features a power-on-reset (POR) output that can be used to keep a digital processor in a reset state until the power supply is within regulation.

The LP3996 supports a 300 mA load on one output and a 150 mA load on the other with less than 36 uA quiescent current for both channels enabled simultaneously during standby. The LM3996 has fast transient performance with small 0603 size 1 uF capacitors at both input and output. For analog loads, the noise and PSRR performance levels can be further improved with use of an external bypass capacitor.

The LP5996 has the same package and features as the LP3996, but does not include POR.

www.national.com

Industry's Smallest ESD Protection Diode Arrays

ON Semiconductor has introduced a new series of low-capacitance electrostatic discharge (ESD) protection arrays in an ultra-small SOT-953 package. Measuring 1.0 mm x 1.0 mm with a 0.5 mm profile, these devices are ideal for applications where board space is at a premium. Designed for a wide range of sensitive equipment, these devices are optimized for use in cell phones, PDAs, digital cameras and other protection applications.

These new SOT-953 packaged devices are 60 percent smaller than the SOT-553 ESD protection diode arrays also available from ON Semiconductor. The SOT-953 provides a 30 percent space savings compared to the 1.0 mm x 1.45 mm Micro-QFN - currently the next smallest package available in the market today.

The NUP45V6 series offer four independent lines of protection from ESD and other harmful transient voltage events. This new series includes devices with protection voltages of 5.6 volts (V), 6.8 V and 12 V and provide IEC61000 Level 4-2 ESD performance. Because of their miniature size, these diodes can be placed near input/output ports to suppress the transient voltage before it can be coupled into the rest of the board. Delivering low capacitance of less than 7 picofarads (pF) at 3 V, and low leakage current of less than 0.1 micro Amp (µA), these integrated devices are highly efficient and offer reliable protection.

www.onsemi.com

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