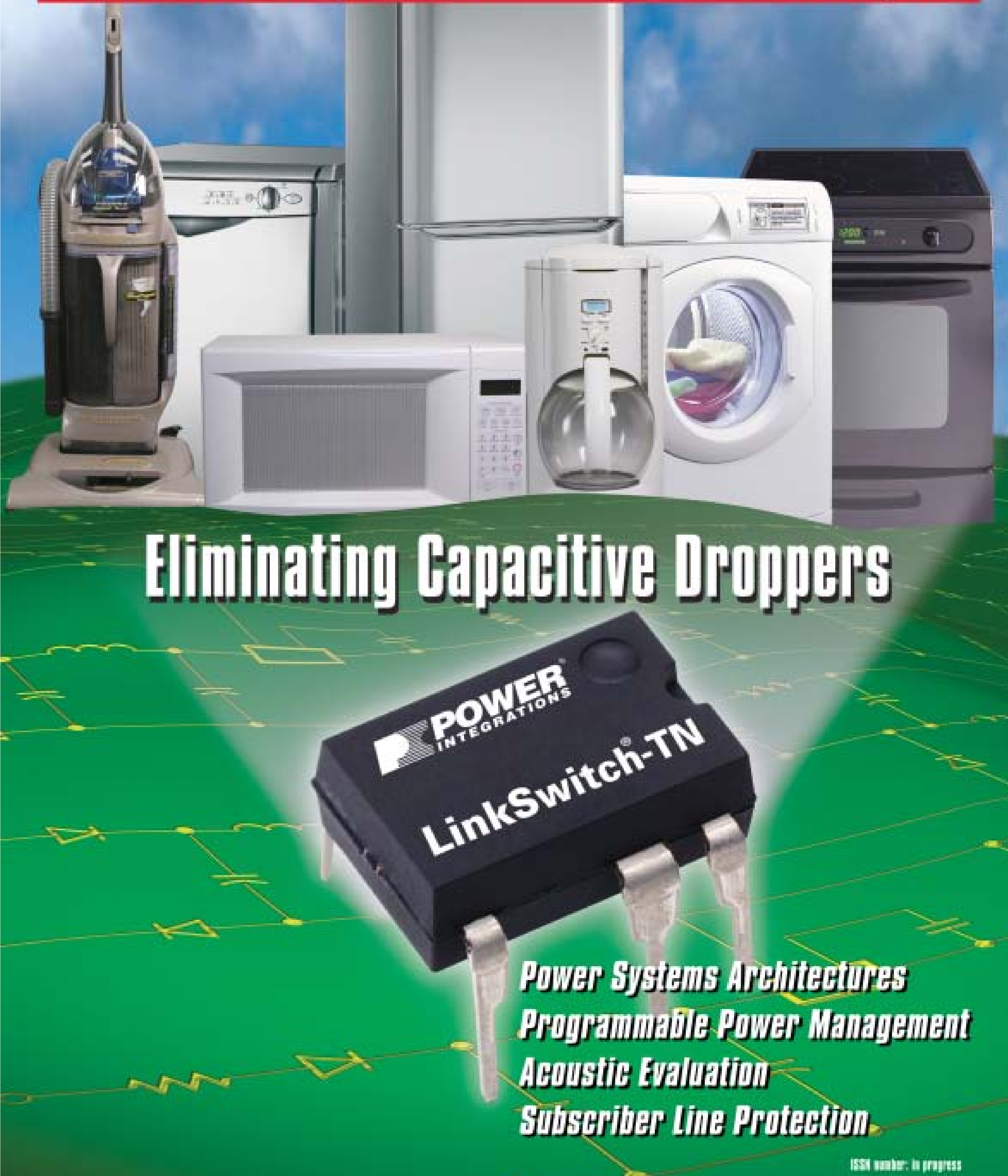
Power Systems Design EUROPE

Power Control Intelligent Motion
February 2004



Eliminating Capacitive Droppers

Power Systems Architectures
Programmable Power Management
Acoustic Evaluation
Subscriber Line Protection

ISSN number: in progress

Power Systems Design EUROPE

Power Systems Design Europe

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Volume 1, Issue 1

The Merry-Go-Round

Welcome and thank you to the industry for the overwhelming support and encouragement that you have given me the opportunity to continue to provide you with a focused technical power magazine in Europe.

Having the first issue of Power Systems Design Europe out in the engineer's hands makes us proud. Julia, Jim and I have turned around everything within a short time. We recognize that there remains a strong interest within the industry to provide a focused publication dedicated to the power sector. As before, I will keep focused on your needs as power systems designers.

Within the pages of Power Systems Design Europe you will find I have added a few extra features, one titled "Power Player". Each issue will introduce you to one of the members of our editorial steering committee who will provide a commentary on the industry. This issue's "Power Player" is a good friend of mine and well-respected colleague, Mr. Eric Lidow, Chairman and Founder of International Rectifier and one of the industry's foremost pioneers in power electronics. He provides you with his insight and analysis on the never ending quest for energy efficiency.

The March PCIM China Conference and Exhibition in Shanghai as well as the European highlight with the May PCIM Conference and Exhibition in Nuremberg will provide continued direction for our industry. Mark your calendar for the last week of May to attend the most important European event in power electronics, PCIM Europe—Nuremberg.

My continued association of more than one and a half decades as a board member of the Nuremberg PCIM conference provides additional fuel for the magazine and keeps the focus strongly set for power technology and their advanced applications.

I will be handling the podium discussions at PCIM 2004 in Nuremberg which is open to visitors and is conveniently located on the exhibition hall floor. Each day around lunch time we will have short presentations from experts followed by an open discussion. This year I chose semiconductors as the focal elements for power electronics. MOSFETs on Tuesday, IGBTs on Wednesday and Rectifiers on Thursday will be the topics.

I have spent more than a quarter of a century in power semiconductors and have seen new switch technologies emerge, being improved over time and now approaching ideal behavior in systems.

Power management in systems has now become a major consideration in product design. No matter the application, when management of power in design is a consideration, I will cover it.

My time as Editor-in-Chief of the former PCIM Europe magazine has inspired me to continue with an even stronger spirit. I am looking forward to continuing to provide you with the latest information on new power technology, applications and product offerings to stimulate your future system designs.

This is a new year with a new beginning and I feel good that my promises and commitments to you are coming true.

I still wear my old New York Yankees baseball cap, a little continuity is one thing we need.

If not before, I will see you at the PCIM show in Nuremberg!

Best regards

Bodo Arlt

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eupec increases its technological leadership

eupec in the future will have a separate department called Technology & Innovation (TI) for the strategic development of innovative technologies.

On 1st November, 2003 the company formed a special team headed by Dr. Reinhold Bayerer (50) for guaranteeing eupec's technological leadership.

"We intend to essentially strengthen our activities with regard to technological and product innovations over the next 5-10 years by this means", explains board member Erich Wallner.

eupec since its foundation by the companies of Siemens and AEG (1990) continuously has been improving its word market position in the high power semiconductor segment and meanwhile is the 2nd biggest player after Mitsubishi. This was possible only by a high innovation rate. While 1990 roughly 22% of all products were younger than 5 years, today 70% of the company's turn-over are achieved by new products.

www.eupec.com

TTI distributes WIMA capacitors

TTI Electronics has signed a franchise distribution agreement with European plastic film and metallised paper capacitor manufacturer, WIMA.

Comments Geoff Breed, TTI's European Marketing Manager: "Continual technical progress and expansion have placed WIMA amongst the top names in film capacitors worldwide. A high degree of automation ensures that WIMA can continue to manufacture in Europe while successfully meeting the challenges and competition of a global market."

WIMA has taken an environmentally-friendly attitude – priority is given to avoiding the use of material containing harmful substances, keeping an eye on the selection of recyclable substances and the reduction of packing materials.

Important new product lines include: polypropylene GTO MKP devices, designed to attenuate voltage spikes on GTO thyristors and IGBTs; and FKP and MKP snubber capacitors, developed to meet the demands of high-power converter technology and available in many switching configurations.

Concludes Breed: "WIMA is an important addition to our portfolio of leading passive names, and provides our customers with even more choice."

geoff.breed@uk.ttiinc.com

New Web-Site at Vicor

Vicor has launched its new Web-site. The site makes use of cutting-edge data-mining tools to ensure "minimum-click" navigation and easy search and selection. This content-rich, product-centric site will help design engineers to find the products and related information they need, quickly and efficiently. Easy access is also provided to Vicor's interactive design and configuration tools.

The site's new search engine searches comprehensively across web pages, documents and media, providing results that are easy to sort due to intelligent and detailed categorization.

The technical library, the product selector, and two innovative on-line design tools enable design engineers to learn about power conversion issues and to select or configure—in real time—products specifically suited to their applications. VCAD (Vicor Computer Assisted Design) facilitates on-line design of configurable VIPAC and VIPAC Array AC and DC power systems. Designs can be saved in the user's account for future reference and convenience.

VDAC (Vicor Design Assistance Computer) enables design engineers to design DC-DC converters to fit their specific requirements. They can specify on-line and verify in real time the attributes and performance of custom DC-DC converter modules.

The Web site features comprehensive information on Vicor's Factorized Power Architecture featuring the new V•I Chips, and an enhanced focus on product support and easy access to applications and technical support.

www.vicorpower.com or www.vicoreurope.com

Intersil To Join NASDAQ-100 Index

Intersil is being added to the NASDAQ-100 Index during the 2003 rebalancing that takes effect December 22, 2003 upon market open, according to a NASDAQ-issued press announcement on the annual re-ranking.

"We're very pleased to see Intersil Corporation join the ranks of the top 100 NASDAQ-listed companies, which include leading technology companies such as Cisco, Dell, Intel, and Microsoft," said Rich Beyer, president and CEO of Intersil. "This is a testament to the great team of dedicated men and women working at Intersil offices around the globe. This will certainly bring added awareness of Intersil's outstanding performance and strat-egy for growth to a larger number of investing institutions and individuals and will help us in achieving our goal of becoming a top-tier high performance analog semiconductor company."

Once a year, NASDAQ adjusts the index's makeup so it consists of the 100 largest non-fi-nancial companies listed. The Nasdaq-100 Index rebalance is based on market cap-italiza-tion, and is the basis for the Nasdaq-100 Tracking Stock—the most actively traded listed U.S. equity security.

www.intersil.com

Power Electronics Design Course

Since 1981, e/j BLOOM has organized and sponsored more educational courses in power conversion design subjects than any other company in the world! Now, as a part of its 23rd anniversary celebration activities, the Educational Division of the company will offer three presentations of a new two-segment Modern Power Conversion Design Techniques course in 2004 in the United States and the United Kingdom.

The first segment, 2 days in length, will deal with the practical design and development issues of state-of-the-art power converter circuits, including introductory sections on converter circuit models for stability control and on design approaches for high frequency transformers and power inductors. Planar and integrated power magnetics are also topics of this part of the course. This segment will be taught by Ed Bloom, President of e/j BLOOM associates Inc. He is a design specialist and a well-known consultant in the field of power converter & magnetics design, and has published many articles on his design methods. He is the co-author of the popular textbook, Modern DC-DC Switchmode Power Converter Circuits, now in its ninth printing. Ed is a Senior Member of the IEEE Power Electronics Society, and has 41 years of design experience in the fields of power electronics.

The second segment of the 2004 course, also 2 days in length, focuses on the proper design of switch-mode power converter circuits and systems for low Electro-Magnetic Interference (EMI) through the use of suitable topologies, component selection, power magnetics design and physical construction of the power conversion system, including printed-circuit board layout techniques. The instructor for this segment will be Bruce Carsten. Bruce is well known in industry circles for his significant contributions to the practical design of modern power conversion circuits and systems, and has over 34 years of design experience. Bruce is a Member of the IEEE Power Electronics Society and has presented more than 115 design-oriented seminars worldwide on modern power electronics circuit & system design issues.

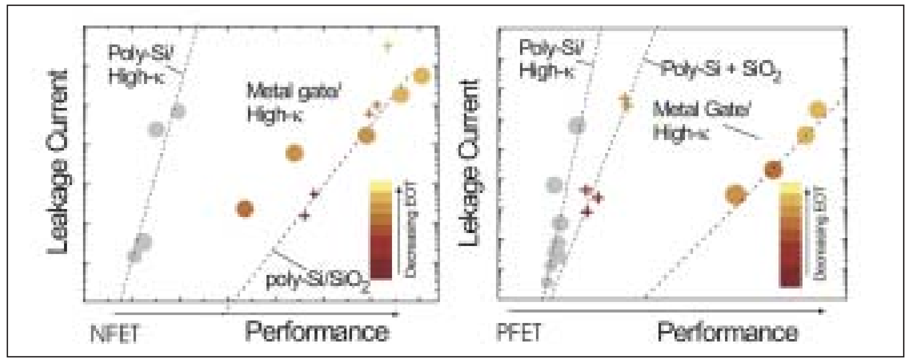
Dates, cities and country locations planned for the three 2004 course presentations are:

- *May 18-21 in Chicago, Illinois, USA. August*
- *17-20 in Las Vegas, Nevada, USA.*
- *October 12-15 in Portsmouth, England, United Kingdom.*

Persons interested in attending the course, or any segments thereof, can obtain a **FREE** brochure containing all registration, cost and course details by simply contacting:

http://www.ejbloom.com/downld.asp

Breakthrough in High-k/metal Gate Stacks



IMEC announces that they have successfully demonstrated the use of high-k dielectrics and metal gates to values below one nanometer. Achieving this level of electrical performance using materials other than the traditional polysilicon-based counterparts removes one of the industry's so-called 'red brick wall' barriers to advancing semiconductor technology.

As part of its industrial affiliation program, an IMEC research team utilized metal gates to overcome the problems imposed by the interaction between high-k materials with the com-monly used polysilicon electrode.

Using TiN or TaN gates and HfO2 as dielectric, aggressive scaling down to an 0.8nm equivalent-oxide thickness (EOT) was demonstrated in both nMOS (8.2 Angstroms EOT) and pMOS (7.5 Angstroms EOT) transistors. The metal-gated devices outperformed their polysilicon-based counterparts in terms of electrical performance parameters, including high conductance, low leakage and reduced threshold-voltage instabilities. Besides the elimination of gate depletion, the metal gates enhanced high-k scalability and significantly reduced gate-leakage by up to three orders of magnitude. Transistor drive current also improved signifi-cantly.

To realize sub-1nm EOT scaling, appropriate interfacial oxide control both prior to and during high-k deposition was applied. The lowest EOT values were typically obtained using a 'minimal interface approach' (i.e. minimal EOT contribution). In order to achieve this, scaled chemical oxide interfaces with controlled thickness and precisely controlled deposition and annealing conditions were used. HfO2 was deposited by atomic layer chemical vapor deposition (ALCVD).

Excellent nMOS performance was demonstrated with performance indicators slightly ex-ceeding those for poly/SiO2-based devices and significant improvement of the pMOS per-formance since the hole mobility remained constant down to the lowest EOT values. In addi-tion, not only the initial performance but also the threshold-voltage instabilities due to trap-ping were strongly reduced as compared to typical results on high-k films with polysilicon electrodes.

Part of this research has been done in collaboration with IMEC's high-k industrial affiliation program partners, namely International Sematech and its member companies, Renesas, Matsushita and Samsung.

Figure-of-merit for both nFET (left) and pFET performance (right) representing gate leakage as a function of performance– the symbols represent performance trend lines for poly/SiO2, poly/high-k and metal/high-k gate stacks.

www.imec.be

Power Events

- *PCIM China, March 17-19, Shangai, China*
- *Electronica USA, Power Electronics Conf. San Francisco March 29th to April 1s*
- *Hanover Industrial Fair, April 19-24, Hanover, Germany*
- *Semicon Europe, April 20-22, Münich, Germany*
- *PCIM 2004, May 25-27, Nüremberg, Germany*
- *Fisita 2004, May 23-27, Barcelona, Spain*

MOSFETs, IGBTs and Rectifiers

The Semiconductor Elements to Start the Design

Power Semiconductors chip performance continue to make improvements. Mounting and packaging technology create more efficient devices. The benefits are influencing all electronics, not only evident in the classical areas like power supply and drive application.

By Bodo Arlt, PSD Europe
Editor-in-Chief

MOSFETs and IGBTs have achieved improvement in silicon resulting in minimized switching and conduction losses. Low voltage MOSFET applications are benefiting from trench-gate technology, which has improved conduction characteristics. While the V MOSFET structure has been present for a long time, this technology has provided improved device performance by significantly increasing cell density per unit area. Other parameters must be considered in a MOSFET switch for a design to be successful. Avalanche capability in inductive switching is an important parameter for keeping the device within the safe operating area. Furthermore, active clamping is used to work successfully on automotive devices.

Trench design is replacing the traditional V MOSFETs designs by offering more active area for the current flow per device size.

DC/DC converters receive the main contribution from MOSFETs, which in combination with optimized passive components demonstrates an over 90 percent efficiency. Synchronous rectification with suitable MOSFETs and necessary control achieves the critical designs. Distributed power architecture uses DC/DC conversion for point of load supply.

Less than 200 volts, the MOSFET continues as the dominant switching element particularly in automobiles. The 42 volt supply and the sophisticated elements of future automobiles, like starter alternator and drive by wire applications, will inspire more tailored devices for this volume market. All manufacturers have a 75volt MOSFET product and future development will continue to support the automotive industry at the required voltage level. Packaging is important for this market segment, as this methodology is a way to compress functions requiring less weight and space in modules.

Above 100 volts IGBTs are the switch of choice. Improvement in IGBTs has been achieved by silicon thinning processes, which as a result lead to better thermal management, and reducing conduction losses. Actual IGBT technology with trench-gate components is bringing significant advantages thanks to the improved conduction characteristic at line voltages. Most IGBTs are at line voltages resulting in preferred breakdown voltages of 600 and 1200 volt. IGBT technology is even replacing historical GTO sockets by reaching voltages up to 6 kilovolt range.

All of these achievements will guide us to more advanced solutions in the power quality arena of power distribution. In the electric drive technology sector, the most important product category is variable speed drives. Modern inverter technology at line-voltage level is built on IGBTs. It is the preferred switch because of short circuit capability, speed and improved saturation voltage.

There are two IGBT concepts the Punch Through (PT) and the Non Punch Through (NPT) both have been improved over the years. Vertically by innovations of the buffer structure or lifetime killing process on the PT side. Reducing the wafer thickness in the NPT side, also the transistor cell structures are changed to minimized planar cells or trench cells. A really outstanding breakthrough in the IGBT development has been achieved with the Field Stop IGBT. This is step towards the next IGBT generation in terms of low static and dynamic losses. The resulting improved dice allow the packaging engineer to further improve his design. Most manufacturers develop a strategy based on end market. Modules of all sizes are readily available. In modules for power applications, the elimination of wire bonds is becoming a reality by using a solder process or pressure contact. All module manufactures are moving to more dense packages.

Perfect diodes with soft recovery characteristics compliment the IGBT performance. All major semiconductor manufacturers are working to optimize rectifiers.

AC to DC rectification is one of the most popular duties for diodes. At 50 or 60 Hertz, there are no really critical switching losses. Bridge rectifiers are available in a variety of packages and configurations in Voltage and Current ranges that serve all industry requirements.

Schottky diodes will still be used in many low voltage applications as a result of their extremely low forward conduction drop.

Inverters at line voltages are using IGBTs along with an ultra fast rectifier. As compared to the use of a MOSFET with an inherently slow intrinsic diode, the IGBT diode combination is a more efficient solution. As a result, in three phase designs at the required voltage, the independent IGBT diode is the favored approach as seen in the marketplace.

A rectifier manufacturer who wants to propose an optimized solution for each function, needs to develop several families with different trade-offs, mainly between forward voltage VF and reverse recovery charges Qrr (or reverse recovery time trr). Guidelines have been suggested to optimize the circuit's limited EMC behavior and the use of the power diodes, often incorporated in modules containing the complete power section of a frequency converter for electric drives. Application orientated testing generates the results that indicate that at a higher switching, the electromagnetic compatibility is confirmed as in some cases it is not correct to push switching speed up and thus suffer from electromagnetic interference (EMI). Therefore, the fast and ultrafast diodes have to have a soft recovery characteristic that minimizes the EMI.

The name of the game in producing an efficient diode is in the doping process and each supplier has a proprietary recipe. The resulting performance is what matters. Most have shown excellent results as evidenced by the data published.

Summarizing we can say that loss reduction and space minimization is a key goal achieved by MOSFETs offering extreme low on resistance thus replacing Schottky diodes while also being the main switch working at the high switching frequency to keep magnetics small in the converter design. While IGBTs dominate the motion arena with switching frequencies above the human ear for comfort. Ultrafast IGBT developments are targeting Switch mode power supply design in the AC to DC applications.

In conclusion all semiconductor manufactures are moving to more dense packages. Novel chip packs appear to provide an alternative in the packaging development. The rectifier and diode technology and design are not a designer's first choice of pursuit but are as needed as the salt in a good recipe.

The independent module and hybrid manufactures have the choice of using any optimized diode that best match their application from a wide variety of different performances of independent producers.

www.toshiba-europe.com/electronics
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www.irf.com
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Energy Efficiency: The Never-Ending Quest

by Eric Lidow, Chairman and Founder, International Rectifier Corp.

As the world's population grows and our use of electronics expands, never has the need to save electricity been as great as it is today. For the makers of the electric devices that have become part and parcel of modern-day life, power management technology has taken on an increasingly important role to achieve key energy efficiency milestones. For those of us who pioneered the power conversion industry, it's a very exciting time along a journey underpinned by a legacy of technology breakthroughs spanning half a century.

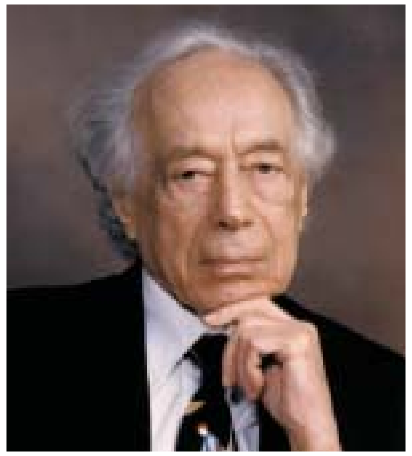
The quest for power efficiency has been the mission of International Rectifier since 1947. In the early years, our quest focused on process materials and energy sources. Soon after opening its doors, International Rectifier became the dominant supplier for selenium rectifiers then moving to germanium and finally silicon.

The early years also brought the study of alternate energy sources that still hold promise today. One was photoelectric power. In the late 50's, International Rectifier demonstrated its potential by converting a 1913 Baker electric car that ran purely on solar energy, the first fully solar-powered automobile in the world. Today, that car is on display at our Temecula California facility, a testament to the futuristic thinking still common in our industry today. International Rectifier went on to commercialize the use of photoelectric cells in space, using it to power the first RCA weather satellite.

The late 70's heralded one of the industry's most fundamental technology shifts, the birth of the first field effect power transistor (FET) and IR developments that spawned a $4 billion dollar industry. The new FETs, manufactured using vertical DMOS process, delivered very high gain and could switch full load at much greater speeds than the prominent bipolar transistor technology found in most power supplies of the time. Shortly thereafter, IR unveiled the HEXFET power MOSFET whose compact six-sided cell structure brought significant advancements in size and performance. These devices now represent more than twice the number of bipolar transistors sold each year.

By the '90's, it was apparent that integrated high-voltage technology was needed to drive MOSFETs in many applications. International Rectifier led with the introduction of a driver capable of operating at 1200V, an IC still unique in the industry.

As it was in the early years, our developments to drive down power consumption have revolved around applications where we can make the largest impact. One of our greatest opportunities today lies in motion control where we can influence the adoption of variable speed motion to dramatically improve the energy efficiency of household appliances and manufacturing equipment. Similarly, we can apply the same electronic motion control technology to automotive systems for electronic braking, electric steering and integrated starter alternators to vastly improve the mileage, safety



and environmental impact of future cars. IR's pioneering efforts in the development of electronic light ballasts also offers meaningful ways to conserve electricity on a global scale.

Looking ahead, we will concentrate on technological barriers still hindering power management advancement in critical, high-impact applications. To lessen the interconnect losses that have now surpassed the silicon losses, we are co-developing and co-packaging an array of power management functions into integrated building blocks using state-of-the-art packaging technologies. More importantly, we're tailoring these building blocks toward specific applications where power management technology can enable the next big leaps in our collective step into the future. As a pioneer in the industry, International Rectifier remains committed to the never-ending quest towards greater energy efficiency and leading the way to technology developments that will make it happen.

COVER STORY

Buck Converter Eliminates Capacitive Droppers

Switching Power Conversion IC Displaces Non-Isolated Passive Power Supplies

For the first time, a new power conversion IC family offers the superior performance of switching power solutions plus extreme energy efficiency for a growing number of very low power applications, at a system cost equal to traditional passive solutions.

Stefan Bäurle and Kent Wong, Power Integrations

Many applications such as appliance controls, LED drivers, electricity meters and residential heating controllers usually require power supplies without galvanic isolation and with low output currents in the range of 20 mA to 100 mA. Passive solutions such as capacitive dropper or line cycle transformer power supplies have traditionally served those needs because of their simplicity and low cost. Lately, however, added features to appliances such as electronic displays require increased power capabilities that cannot be fulfilled cost effectively with capacitive dropper power supplies. Additionally, consumers today demand energy efficiency in their products. Passive power supplies are therefore no longer an option.

The new highly integrated off-line switcher IC series, LinkSwitch TN, is specifically designed to address the increased load current demands and energy efficiency requirement for non-isolated power supplies. This flexible new family supports a variety of different topologies such as buck, boost, buck-boost, SEPIC and flyback. Unlike passive solutions, it enables universal input voltage range power supplies and provides system level protection in case of faults such as thermal overload, output short-circuit and open control loop. Power supplies based on this device typically consume less than 0.2 W during no-load at 265 VAC input voltage. Additionally, they can be produced entirely using surface mount components.

The LinkSwitch TN family consists of three family members. The maximum deliverable output current for each device in a non-isolated buck converter is outlined in Table 1. For example, the smallest family member, LNK304, is able to deliver up to 120 mA running in mostly discontinuous conduction mode (MDCM). In continuous conduction mode (CCM) the LNK304 can deliver output currents up to 170 mA. All devices in the family are available either in a DIP 8 or SMD 8 package that offers a minimum creepage of 1.98 mm between the high voltage pin and adjacent low voltage pins.

OUTPUT CURRENT TABLE				
PRODUCT	230 VAC ±15%		85-265 VAC	
	MDCM	CCM	MDCM	CCM
LNK304P or G	120 mA	170 mA	120 mA	170 mA
LNK305P or G	175 mA	280 mA	175 mA	280 mA
LNK306P or G	225 mA	360 mA	225 mA	360 mA

Table 1. LinkSwitch-TN Output Currents

IC Description

LinkSwitch-TN devices integrate a 700 V power MOSFET with a low voltage controller that includes simple ON/OFF control, an oscillator, frequency jittering, a fully-integrated auto-restart circuit, a high voltage switched current source, cycle-by-cycle current limit, and thermal shutdown circuitry. Figure 1 illustrates the internal block diagram of the LinkSwitch-TN. The simple ON/OFF control scheme enables the power MOSFET to switch when a current of less than 49 A is delivered into the FEEDBACK (FB) pin, representing a voltage of less than 1.65 V. The typical oscillator frequency is set to 66 kHz with a frequency jitter of 4 kHz peak-to-peak to minimize EMI emissions. In order to optimize EMI reduction for both average and quasi-peak emissions, the modulation rate of the frequency jitter is set to 1 kHz. In the event of a fault condition such as output overload or into auto-restart mode, which disables the power MOSFET for 800 ms if no feedback from the output is received for 50 ms. Becausef the extremely low power consumption of the internal control circuitry of LinkSwitch TN, the chip can be powered through the integrated high voltage MOSFET. The high voltage switched mode current source charges a capacitor connected to the BYPASS (BP) pin to 5.8 V directly from the drain whenever the drain is off. A bypass capacitor of 0.1 F is sufficient for energy storage and for high frequency decoupling. The BYPASS pin under-voltage circuitry enables (turns on) the power MOSFET after the BYPASS pin reaches 5.8 V at start-up. If the BYPASS pin voltage is lowered below 4.85 V, the power MOSFET will be disabled; it must then be raised back to 5.8 V to re-enable the power MOSFET. A 6.3 V shunt regulator clamps the BYPASS pin when current is provided through an external resistor, to further decrease no-load consumption.

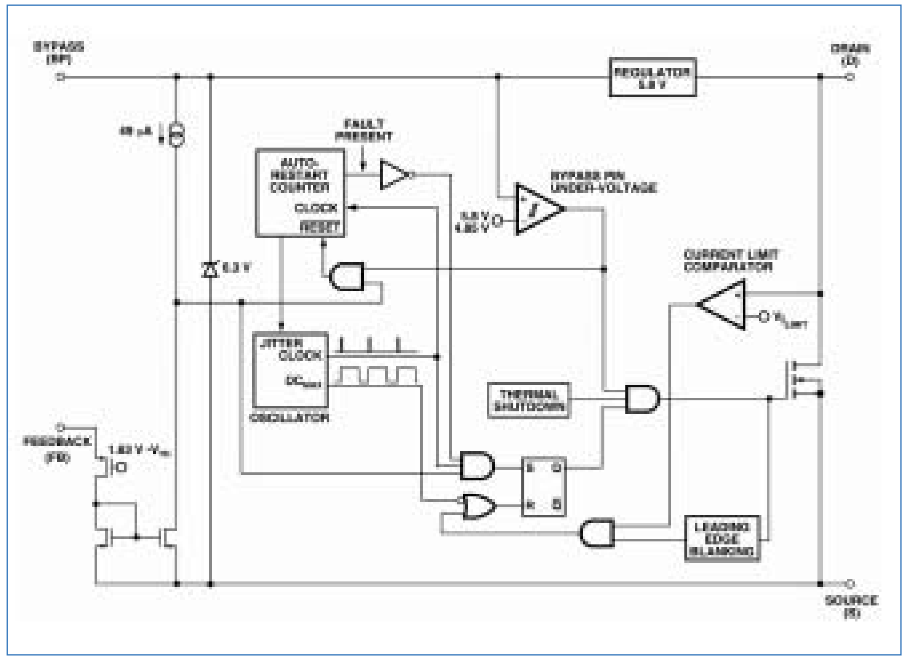


Figure 1. Functional Block Diagram

The current limit circuitry senses the drain current of the power MOSFET and terminates the switching cycle when the drain current exceeds an internal threshold. The current limit circuitry also incorporates a leading edge blanking time circuit, which inhibits the current limit comparator for a short time after the power MOSFET is turned on so that current spikes caused by rectifier reverse recovery time and primary-side capacitance will not prematurely terminate the cycle. The over-temperature protection circuit senses the die temperature and is triggered when the temperature exceeds 142 C. his disables all switching until the die temperature drops by 75 C, whereupon it is re-enabled.

Application Example

The circuit in Figure 2 depicts a typical implementation of a 12 V, 120 mA non-isolated buck converter employing LNK304 that operates from a worldwide mains input. The input stage comprises fusible resistor RF1, rectifiers D3 and D4, DC rail electrolytic capacitors C4 and C5, and inductor L2. Thanks to the IC's integrated frequency jitter, the simple pi-filter consisting of C4, L2, and C5 provides enough attenuation to meet the requirements for conducted emissions according to EN 55022, class B. Resistor RF1 is a flameproof, fusible, wire wound resistor that accomplishes three functions. First, it limits the inrush

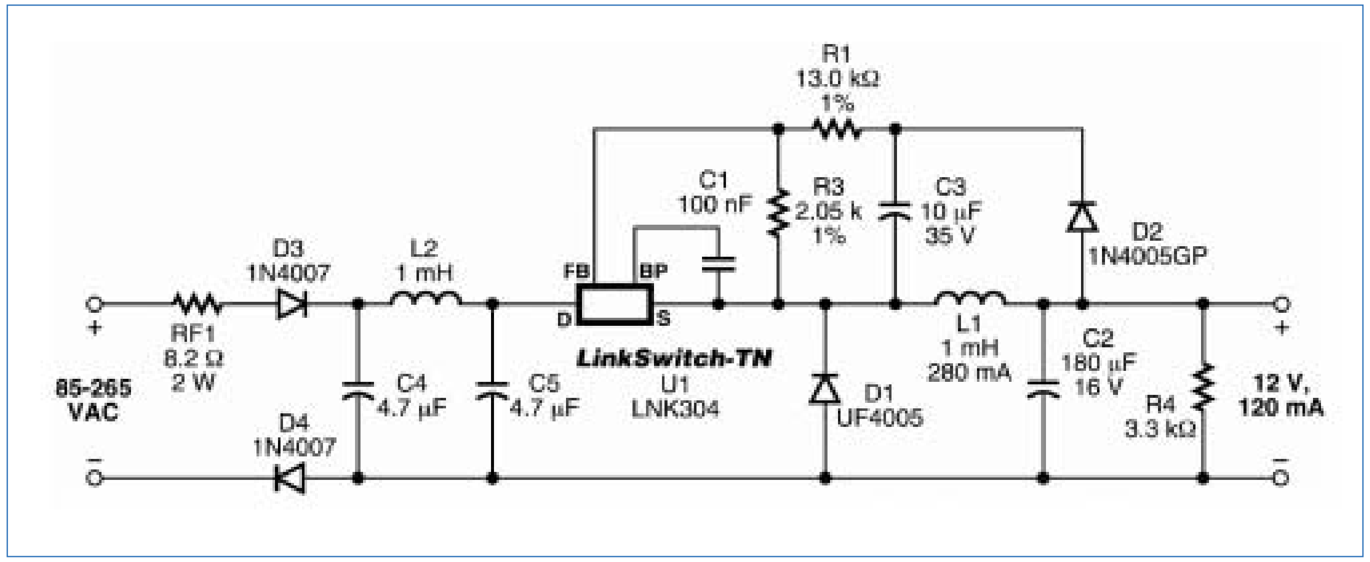


Figure 2. Universal input 12 V, 120 mA off-line buck converter with LinkSwitch-TN

current limit to a safe level for the input rectifiers. Secondly, it attenuates differential mode emissions. Finally, it acts as an input fuse in case any other component fails short-circuit.

The power stage is formed by LNK304, the freewheeling diode D1, output choke L1, and the output capacitor C2. In this particular case the IC and L1 have been selected to set a mostly discontinuous mode of operation. Choke L1 is a standard off-the-shelf inductor with an appropriate RMS current rating. The minimum required inductance to deliver the desired output power can be calculated as follows (MDCM operation):

$$L_{1(MIN)} = \frac{2 \cdot V_O \cdot I_O \cdot (V_{MIN} - V_{DS} - V_O)}{I^2_{LIMIT(MIN)} \cdot f_{OSC(MIN)} \cdot (V_{MIN} - V_{DS}) \cdot \frac{1+2\cdot\eta}{3}}$$

where VMIN is the minimum DC bus voltage, VDS is the LinkSwitch TN Drain-to-Source voltage (typically 10 V), ILIMIT(MIN) is the specified minimum internal current limit of the respective device (0.24 A for the LNK304), fOSC(MIN) is the specified minimum oscillator frequency (62 kHz), and ? is the estimated efficiency (e.g. 0.7). The factor (1+2?)/3 takes into account that approximately 66% of the losses in the converter are dissipated in L1 and D1. Those losses are processed by the buck choke as well. For a proper selection of the inductor, the inductance tolerance (typically ±10%) and the drop of inductance at elevated component currents (typically 10%) need to be factored in. Therefore, L1(MIN) is multiplied by a factor of 1.1 to 1.2 (using 1.15 as a typical value) to find the data sheet value of inductor L1.

Electrolytic capacitor C2 is the output filter capacitor. It is primarily selected to determine the desired maximum output voltage noise, which is generally a stronger function of the ESR than the capacitance value of the capacitor. The output regulation is performed with a bootstrap circuit formed by the feedback diode D2, tracking capacitor C3, and the resistor divider R1 and R3 connected to LNK304's FB pin. To a first order, the forward voltage drops of D1 and D2 are identical. Thus, the voltage across C3 tracks the output voltage. Resistor R3 effectively increases the ON/OFF current threshold compared to the internal FB pin threshold (typically 49 µA) by establishing a bias current for the feedback resistor divider. A bias current value of 0.75 mA is recommended. The feedback resistor network can therefore be calculated as follows:

$$R3 = \frac{V_{FB}}{I_{FB} + 750\,\mu A} = \frac{1.65\,V}{49\,\mu A + 750\,\mu A} = 2065\,\Omega$$

$$R1 = \frac{R3 \cdot (V_o - V_{FB})}{V_{FB}}$$

This simple feedback approach requires a constant current flow through inductor L1, allowing capacitor C3 to accurately sample the output. Resistor R4 therefore establishes a pre-load of approximately 3.6 mA, keeping the output in regulation even at very light loads.

Figure 4 shows that the load regulation of LinkSwitch-TN at 240 VAC input is much better than the load regulation of the capacitive dropper example depicted in Figure 3.

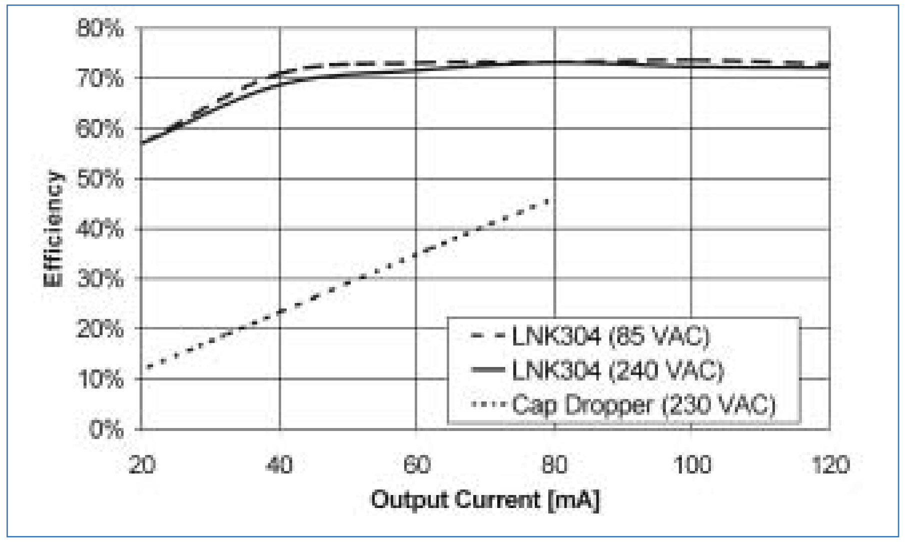


Figure 5. Efficiency LNK304 Buck Converter vs. Capacitive Dropper Example

The increasing output voltage with smaller load currents can be controlled with the pre-load resistor R4 as described above. For a minimum system load of 10 mA, the pre-load resistor can be eliminated and the feedback capacitor C3 can have a smaller value (1 µF, for instance).

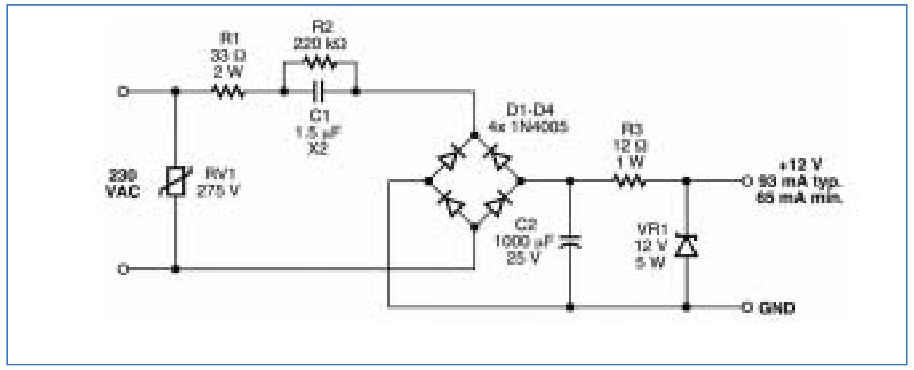


Figure 3. Capacitive dropper example delivering 12 V, 65 mA (230 VAC input only)

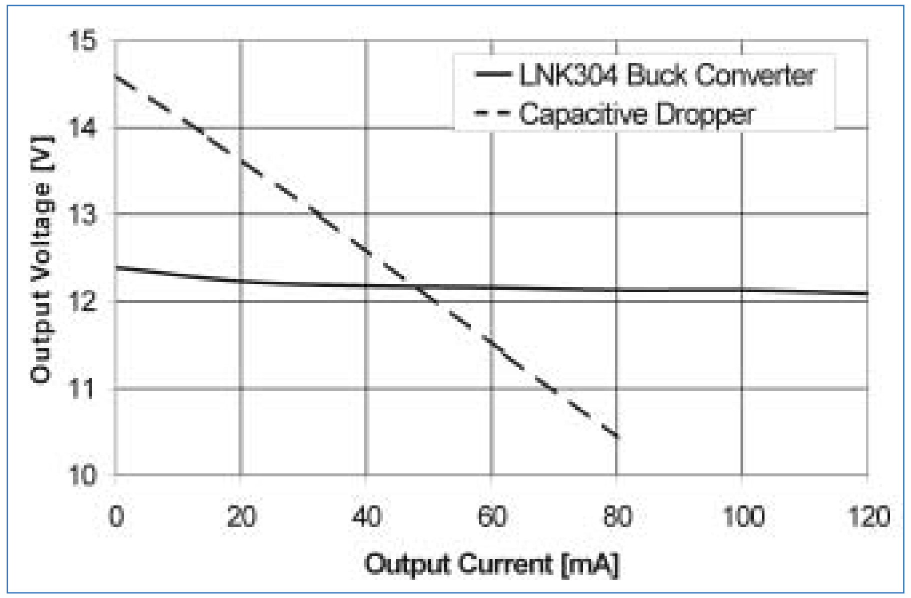


Figure 4. Load Regulation LNK304 Buck Converter vs. Capacitive Dropper Example

Figure 5 shows that the full load efficiency of the buck converter example is typically 72% compared to 45% for the capacitive dropper at its maximum current capability of 80 mA. It is interesting to note, that even at light load currents such as 20 mA, the LinkSwitch-TN buck converter still offers an efficiency of 57%, whereas the efficiency of the capacitive dropper decreased sharply to 11%.

The no-load input power of the LNK304 based buck converter is typically below 180 mW at 265 VAC input voltage. This compares to 2.6 W for the capacitive dropper at 230 VAC input voltage.

Conclusion

The LinkSwitch TN IC family is a universal, cost effective and extremely energy efficient switching alternative to the traditional highly inefficient passive type non-isolated power supply currently being used. The highly integrated device is optimized for a simple low-cost buck or buck-boost converter topology that is well suited to handling the electronic control requirements for major appliances and any other non-isolated low output current power supplies. Please visit *www.powerint.com* for more information.

Ever Seen a Unicorn?

Heat Pipes do exist

Heat pipes are efficient, two-phase heat transfer devices with effective thermal conductivities several thousand times that of solid copper. They are in effect heat movers or spreaders.

By John Broadbent, Thermacore

No one has ever seen a Unicorn, nor are likely to, it's an imaginary creature. Everyone however will be able to describe a white horse with single long spiralled horn. Unlike the Unicorn, Heat Pipes do exist, and although commercially available since the mid 1960's they are little known and little understood.

In the past decade, the electronics industry seems to have defied the laws of economics by providing increasing performance at less cost. However the industry has been unable to suspend the laws of physics, higher performance has been accompanied by higher heat generation.

As a result thermal management is critical and finding thermal solutions will become important for the cost reduction and time-to-market pressures governing success in electronics sales.

Heat Pipe cooling of electronics is increasingly popular due to thermal advantages, reliability and cost.

Heat Pipe operation

Heat pipes are efficient, two-phase heat transfer devices with effective thermal conductivities several thousand times that of solid copper. They are in effect heat movers or spreaders; they acquire heat, and move or spread it to where it can be more readily rejected.

Construction usually begins as a tube, typically copper Figure 1. The inside of the tube is lined with a wick structure, which provides surface area for the

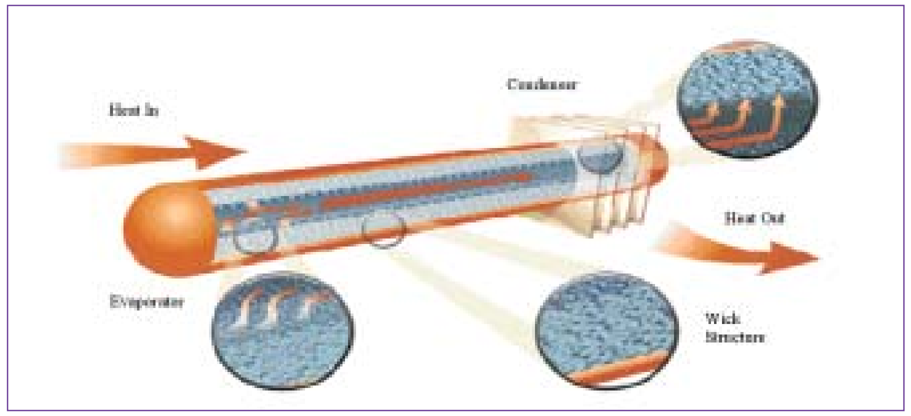


Figure 1. Heat Pipe Operation

evaporation/condensation cycle and capillary capability. The core of the tube is open for vapour flow. Before being sealed the tube is evacuated and a small quantity of working fluid just enough to saturate the wick is added.

The fluid, typically water, is the only dynamic component in the heat pipe; the pressure inside the pipe is equal to the saturation pressure associated with ist temperature. As heat enters the equilibrium is upset generating vapour at a higher pressure and temperature. The higher pressure causes vapour to travel to the condenser where the lower temperature causes the vapour to condense onto the wick structure giving up its latent heat of vaporisation. The condensed fluid is returned back to the evaporator by gravity and/or the capillary forces in the wick structure. This cycle can transfer large quantities of heat with very low thermal gradients.

Applications:
Embedded Heat Pipes

As heat fluxes increase solid metal extrusions exhibit inherent limitations. The geometry and material result in high spreading resistance and in order to offer enough surface area these sinks tend to be large and heavy.

Figure 2. Embedded Heat Pipe Heat Sink

When embedded into extrusions Figure 2. The high thermal conductivity of heat pipes spread the heat throughout the base of the sink minimising spreading resistance making the sink far more efficient.

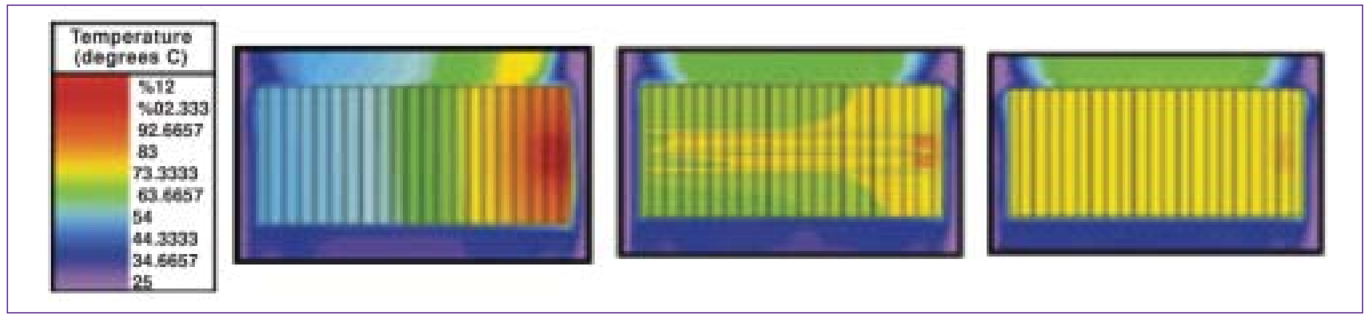


Figure 3. Comparison of Three Heat Sinks.

This reduction of spreading resistance is particularly beneficial in applications where the heat source or heat sources are concentrated. Even higher performance in reducing base spreading resistance would be to fabricate the entire base from a vapour chamber (Therma-Base). The vapour chamber utilizes the effective thermal conductivity of two-phase heat transfer to virtually eliminate spreading resistance in the heat sink base, increasing the effectiveness of fins located at the perimeter of the heat sink, offering the possibility to reduce its size and weight.

Figure 3 compares the relative performance of three heat sinks. All had the same geometry and a 75 watt heat source placed 1.3cm from the right hand edge. The sink on the left is an aluminum extrusion. The middle profile is the same with three embedded heat pipes showing a 36% improvement. The profile on the right is a sink with a vapour chamber base showing a 44% improvement.

Remote fin stack (Therma-Sink)

Many custom situations are improved by heat pipe assemblies. Constraints such as height restrictions, which limit heat sink profile options and component distances from available air source, are common problems that are solved.

Therma-Sink designs typically consist of an evaporator block (heat input) the heat pipe(s) (heat transport) and fins (heat dissipation). The heat pipe technology moves the heat from the heat source to a location where enough air volume exists for adequate heat removal. Fins are stacked onto the heat pipes to provide the surface area required for heat dissipation.

The relatively small size (a 6mm heat pipe can transfer 30-40 watts with little or no ?T) ensure maximum flexibility in where to site the remote fin stack Figure 4.

Figure 4. Therma-Sink™

Wick structures

The main distinction of heat pipes, besides working fluid, is wick structures. Several types of wick structure are used in copper/water heat pipes including, screen, grooves and sintered metal powder. Wicks are primarily used to provide capillary pumping to return condensed liquid to the evaporator. The selection depends on the power handling requirements and working orientation. Groove and screen mesh wicks have limited capillary force capability, they can not overcome significant gravitational forces, and dry out can occur and are therefore limited to gravity aided and horizontal orientations.

Sintered powder wicks are capable of returning working fluid to the evaporator against gravity by using capillary pumping action and are effective in against gravity applications.

The finer the pore radius of the wick structure, the higher against gravity the heat pipe can operate.

Sintered powder wicks provide a large surface area available for evaporation and provide a mechanism to accommodate vapour and liquid simultaneously. Typical sinter powder wicks handle 50W/cm≈, and have been tested to 250W/cm≈. In comparison a groove wick will nominally handle 5W/cm≈ and a screen wick 10W/cm≈ Figure 5.

Orientation & Pipe Geometry

The efficiency of the heat pipe will decrease as the angle of operation against gravity increases, therefore the orientation of heat pipe designs are critical. When possible the heat source should be below or at the same elevation as the cooling section. This allows gravity to aid the capillary action and results in greater heat carrying capability. If this orientation is unacceptable, a sintered powder wick will be required. Custom geometry is possible by the bending and flattening of the heat pipes.

Limitations

Heat pipes can be manufactured in many shapes and sizes and designed to carry a few watts or several kilowatts. For a given temperature gradient, heat pipes can transfer significantly more heat than even the best metal conductors. There are two primary limitations that must be considered:

Thermal Conductivity

When driven beyond its rating the thermal conductivity of the heat pipe will be reduced. It is important to design a heat pipe to safely transport the required heat load.

Figure 5. Three kinds of wicks.

The maximum heat transport capability of the heat pipe is governed by several limits. Viscous, sonic, capillary pumping, entrainment and boiling Table 1.

Thermal Resistance

Another primary heat pipe design consideration is the effective heat pipe thermal resistance or overall ?T at a given design power. As the heat pipe is a two-phase heat transfer device, a constant effective thermal resistance value cannot be assigned. The effective thermal resistance is a function of a number of variables, such as heat pipe geometry, evaporator length, condenser length, wick structure and working fluid. The total thermal resistance is the sum of the resistances due to conduction through the wall, conduction through the wick, evaporation or boiling, axial vapour flow, condensation and conduction losses back through the condenser section wick and wall.

Detailed thermal analysis of heat pipes is complex. There are however a few guidelines that can be used for first pass design considerations.

A rough guide for a copper/water heat pipe with a powder metal wick structure is to use 0.2°C/W/cm≈ for thermal resistance at the evaporator and condenser and 0.02°C/W/cm≈for axial resistance. The evaporator and condenser resistances are based on the outer surface area of the heat pipe. The axial resistance is based on the cross-sectional area of the vapour space. This design guide is only useful for powers at or below the design power for the given heat pipe.

Manufacturing

Every heat pipe should be subjected high temperature and high internal pressure to be aged. After this aging every pipe must pass a thermal response test to check its leakage and ensure its normal function. If the heat pipe is to be bent into some custom geometry the minimum bending radius is 3 x the pipe diameter. Tighter bends increase the risk of the pipe damage. Bending 2.5 x the diameter may be possible depending upon pipe hardness, wall thickness and the process used. Heat pipes can also be flattened, calculating the minimum flattened thickness for sintered pipes can be straightforward if the production mandrel diameter is known. Thermacore can change the pipe specification by adjusting the mandrel diameter and reducing the pipe wall thickness in order to achieve the flattening requirements.

Conclusions

With increasing power levels in smaller packages heat pipes provide effective solutions.

These passive, efficient and versatile heat transfer devices can be applied directly to a heat source(s) and attached to a heat sink such as a fin stack, extrusion, thermoelectric devise, cold plate or enclosure wall. Heat pipes can also be used to enhance other thermal solutions such as extrusions.

Thermacore are investing a large portion of earnings in continues R & D to develop advanced wick structures and in the introduction of new and advanced materials into the production environment. Flexible, laminated and pulsating heat pipes are just a few of the new technologies on the Thermacore roadmap.

www.thermacore-europe.com

Heat Transport Limit	Description	Cause	Potential Solution
Viscous	Viscous forces prevent vapor flow in the heat pipe	Heat pipe operating below recommended operating temperature	Increase heat pipe operating temperature or find alternative working fluid
Sonic	Vapor flow reaches sonic velocity when exiting heat pipe evaporator resulting in a constant heat pipe transport power and large temperature gradients	Power/temperature combination, too much power at low operating temperature	This is typically only a problem at start-up. The heat pipe will carry a set power and the large ^T will self correct as the heat pipe warms up
Entrainment Flooding	High velocity vapor flow prevents condensate from returning to evaporator	Heat pipe operating above designed power input or at too low an operating temperature	Increase vapor space diameter or operating temperature
Capillary	Sum of gravitational, liquid and vapor flow pressure drops exceed the capillary pumping head of the heat pipe wick structure	Heat pipe input power exceeds the design heat transport capacity of the heat pipe	Modify heat pipe wick structure design or reduce power input
Boiling	Film boiling in heat pipe evaporator typically initiates at 5-10 W/cm2 for screen wicks and 20-30 W/cm2 for powder metal wicks	High radial heat flux causes film boiling resulting in heat pipe dry out and large thermal resistances	Use a wick with a higher heat flux capacity or spread out the heat load

Table 1.

POWER SEMICONDUCTORS

FRFET increases reliability of Phase-Shifted ZVS Full Bridge PWM Converter

ZVS topology operating at high frequency can improve the efficiency

If the body diode is not properly designed the power switch may lose gate control. The new FRFET overcomes the reliability issue for this topology by incorporating a robust, low Trr, soft recovery diode.

Sampat Shekhawat, Praveen Shenoy and Bob Brockway, Fairchild Semiconductor

Abstract

High reliability is very important for today's Switched Mode Power Supply (SMPS) market. High switching frequency allows reduction of power supply size. The zero-voltage-switching (ZVS) or zero-current-switching (ZCS) topologies which allow for high frequency switching while minimizing the switching loss are of interest. ZVS topology operating at high frequency can improve the efficiency as well as reduce the size of the power supply. ZVS also reduces the stress on the semiconductor switch, improving the reliability. These advantages have made the high voltage high power Phase-Shifted Full Bridge ZVS PWM converter a very popular topology. The conventional power MOSFET body diode can cause device failure during switching due to un-recovered minority carriers. The new fast body diode MOSFET (FRFET MOSFET) is designed to address the diode reverse recovery problem.

Introduction

The SMPS industry is experiencing revolutionary developments in increased efficiency, and reliability due to improved power devices for the circuit topologies. The Phase-Shifted, Pulse Width Modulated, Full-Bridge Zero-Voltage-Switched (PS-PWM-FB-ZVS) topology utilizing the FRFET as power switches can achieve the above goals. The poor reverse recovery (Trr) characteristics of the inherent body diode of high voltage MOSFET can reduce the reliability under certain conditions. These conditions can occur even during light loads where switch with high output capacitance can enter a hard-switching condition and increase switching losses. If the body diode is not properly designed the power switch may lose gate control. The new FRFET overcomes the reliability issue for this topology by incorporating a robust, low Trr, soft recovery diode.

Topology description

The PS-PWM-FB-ZVS converter as shown in Figure 1 usually operates at switching frequencies (fs) in excess of 100 kHz. In the conventional H-bridge topology the switches are turned on and off under hard switching conditions. A conventional H-bridge topology can be modified to obtain the PS-PWM-FB-ZVS topology. First, modulation is achieved by phase shifting two overlapping constant frequency square waves by using leading-leg and lagging-leg. Second, it

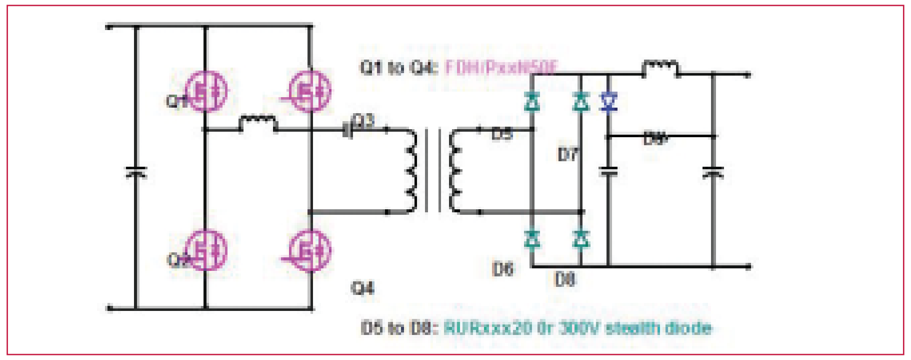


Figure 1: PS-PWM-FB-ZVS topology

is important to achieve resonant ZVS to minimize the switching losses that result from hard switching. The primary difference between this topology and the more traditional H-bridge topology is the switching method to achieve ZVS.

Instead of turning on the diagonally opposite switches of the bridge simultaneously (i.e. Q2 & Q3, Q1 & Q4), a phase shift is introduced between the switches in the left leg (leading-leg Q1 & Q2) and those in the right leg (lagging-leg Q3 & Q4) as shown in Figure 2. This phase shift determines the operating duty cycle of the converter. Zero-voltage turn-on is achieved by using the energy stored in the leakage and series inductance of the transformer to discharge the output capacitance of the switches through resonant action. The resonance forces the body diode into forward conduction prior to gating on the switch.

ZVS process

Two different mechanisms exist which provide ZVS [3] for the lagging-leg and leading-leg.

From Figure 1 and Figure 2, at $t=t_1$, Q1 is turned-on just after Q2 has turned–off. The current starts to free wheel through D1 and Q3. At $t=t_2$, the stored energy in the inductor may not be adequate to turn-off Q3 under a ZVS condition. The energy stored in L1 is used to charge the output capacitance of Q3 and discharge the output capacitance of Q4. The energy stored in the output filter inductor was freewheeling through the output rectifier diodes and does not affect the lagging-leg switches. When the output capacitance of Q4 discharges, D4 turns-on and then Q4 can be turned-on at ZVS. Once D4 conducts, positive bus voltage is applied to the primary winding of the transformer. Using a switch with low effective output capacitance eliminates hard turn-off and turn-on improving the efficiency at light loads. To achieve soft turn-on and turn-off of the lagging leg, the following equation should be satisfied.

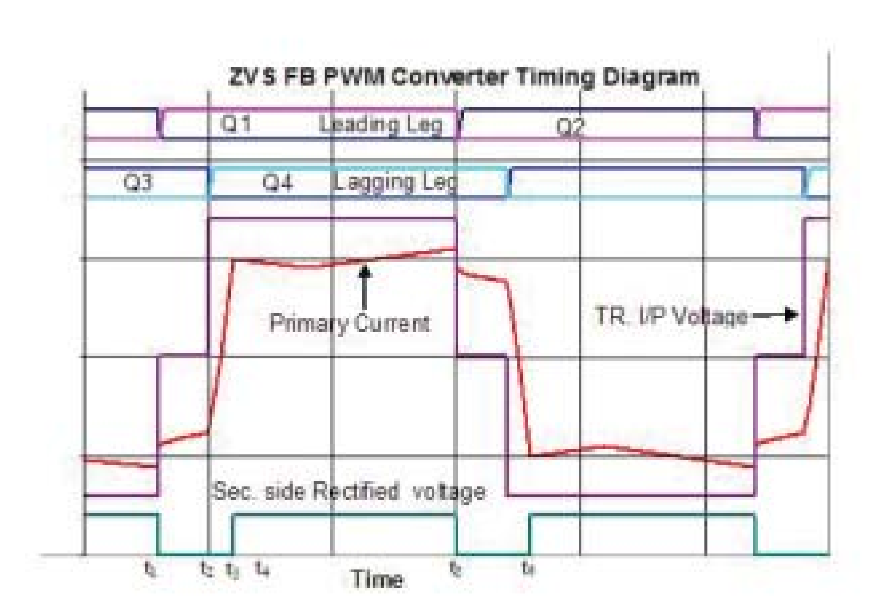


Figure 2: ZVS Waveforms

$$0.5L1(I_{p1})^2 > 0.5(C_{oe3}+C_{oe4}) \times (V_{in})^2 + 0.5C_{TRW} \times (V_{in})^2$$

Where C_{oe3} & C_{oe4} = Effective output capacitance of the power switches Q3 & Q4, I_{p1} = Primary transformer current at turn-on and turn-off for Q3 and Q4 and C_{TRW} = Transformer winding capacitance.

For the leading-leg switches (Q1& Q2), the ZVS occurs as explained below.

At t=t_5, when Q1 is turned-off, the energy stored in the output filter inductor L2 and primary side inductor L1 is available to charge Q1 output capacitance and discharge Q2 output capacitance. The output filter inductor value is high. So, even at light load, the energy stored in L2 is high enough to turn-off Q1 and turn-on Q2 and vice versa under a ZVS condition. Once the output capacitance of Q1 is charged and the output capacitance of Q2 is discharged, there is still enough energy available to forward bias the diode D2. Once D2 is on, the leading-leg switch can be gated-on. If the switch Q2 is now commanded to turn-on, the diode D2 continues to carry current for a long period of time due to the energy stored in L1 and output inductance L2. The stored energy in the filter inductor is large compared to that required to charge and discharge the capacitances in the primary. So the switch capacitance is charged at a linear rate. Accordingly, for soft turn-on and turn-off of the leading leg the following equation should satisfy.

$$0.5\,(L2_p+L1) \times (I_p)^2 > 0.5(C_{oe1}+C_{oe2}) \times (V_{in})^2 + 0.5C_{TRW} \times (V_{in})^2$$

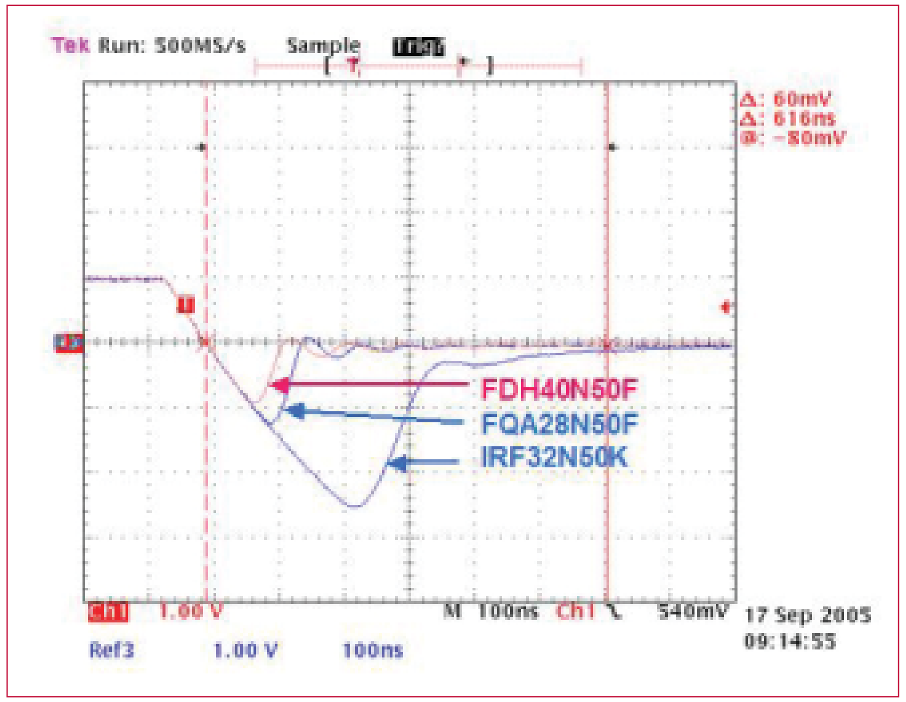


Figure 3: Diode reverse recovery comparison @ Vrm = 20V, I_F=10A, di/dt = 150A/us.

Where: C_{oe1} & C_{oe2} = Effective output capacitance of the power switches Q1 & Q2. $L2_p$ is the output filter inductance referred to primary.

Importance of free wheeling diode for this topology

The MOSFET body diode must not be taken lightly in the ZVS topology. Even with the reduced switching stress on the MOSFET, failure may occur because of a poor diode recovery. The failures have been reported [1, 2] at no-load or light-load conditions. These failures result from the lagging-leg losing ZVS at turn-on and turn-off forcing a hard switching condition. One potential failure mechanism is due to the CGD x dVDS/dt current. The resulting current can cause VGS to charge above VTH. A shoot through condition will exist where both of the MOSFETs in the lagging-leg can turn-on and cause the leg to fail.

To achieve ZVS at turn-on, the body diode of the on coming MOSFET is allowed to conduct current. For example, body diode (D2) of Q2 will conduct current when Q1 is turned-off. When the Q2 MOSFET is gated-on, channel will start carrying current in the third quadrant (same direction as diode). Current will free-wheel through D2 and Q4.

POWER SEMICONDUCTORS

When Q4 is turned-off, diode D2 and diode D3 will carry current. When Q3 is turned-on at t6, the current in diode D2 decays to zero. The MOSFET Q2 will start to conduct in forward direction. The body diode D2 starts to recover with a very low reverse voltage. The body diode Trr increases significantly due to low reverse voltage. Figures 3 & 4 illustrate the influence of Vrm on diode recovery. Figure 3 shows that when diode recovers with di/dt= 150A/mA and 20V reverse voltage, the body diode Trr is 616ns. The Trr increases further when Vrm is reduced to 10V as shown in figure 4. The di/dt is less in this case which should have reduced Trr but it increased instead due to reduced Vrm. It is clear that the Trr increases as the reverse voltage is reduced.

If the MOSFET Q2 is turned-off and its body diode has not fully recovered before the complementary switch Q1 turns on, the body diode of Q2 can create shoot-through. The dVDS/dt can cause a current, made up of the un-recovered charge in the diode and the charge in CDB, to flow through the parasitic NPN Rb base resistance. This current can bias on the parasitic NPN BJT causing loss of Q2 MOSFET gate control and failure. The diode should have a low Qrr, Trr and Irrm to overcome the problem discussed above. The Qrr and Trr of the body diode should be low enough to provide complete minority carrier removal before the device turns-off. If this does not occur, the turn-off dVDS/dt of this device could turn-on the parasitic NPN transistor and forcing the transistor into secondary breakdown. The possibility of this failure occurring increases as the frequency is increased. The life time of the parasitic body diode has been killed by Platinum diffusion and that has reduced the Qrr, Trr and Irrm.

Conclusion

The reliability problems of the PS-PWM-FB-ZVS topology have been documented. These problems can be over-come by using the FRFET series

MOSFET. The CGD x dVDS/dt immunity of these MOSFETs has been increased by reducing QGD, the QGD/QGS ratio, and the internal gate resistance (ESR) and increasing VGS(TH). The intrinsic body diode of the FRFET MOSFET has been improved by reducing the Qrr and Trr as shown in Figure 3. The Qrr of the FCS fast body diode MOSFET has been reduced by 10X compared to standard MOSFET and Trr has been reduced by 5X. This take care of the reliability issues. The Trr and of FDxxxN50F series Qrr has been reduced compared to our previous generation FRFET (FQxxxN50F series). For more information, go to:

www.fairchildsemi.com/power/

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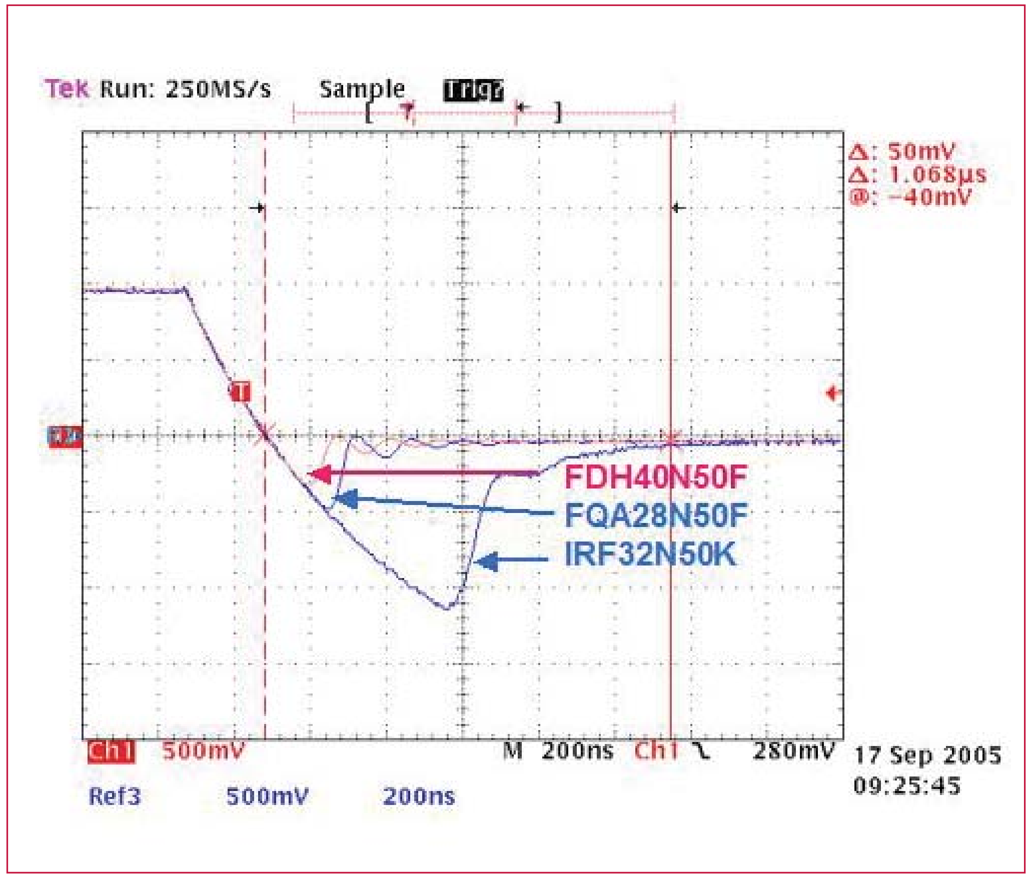

Figure 4. Diode reverse recovery comparison @ Vrm = 10V, I_F=9A, di/dt = 50A/us.

The ACPI advantage and system design challenge

The Late and future-generation of computers will benefit

Today's computers represent a quantum leap in performance and complexity compared to the available technology of only a few years ago. Nevertheless, a paramount goal of these late and future designs is to make this complexity transparent to the user.

By George Lakkas and Bogdan Duduman, Intersil

With minimal setup and intervention, these computers will be able to wake up to perform routine maintenance, download software updates, send and receive fax transmissions, answer the telephone, download audio and video streams and, when the tasks are complete, go back to a low power sleep state where they consume less than a night light. This is the world of Instantly Available PCs (IAPC).

Picture the following scenario in an office setting: a computer system will be powered up in the morning, and the CPU and all other system component voltages will receive regulated power from the on-board dc/dc regulators operating off the AC/DC supply (also known as the "silver box"). During the day the user may leave the computer unattended for coffee break or meetings. Upon a pre-determined lack of user input, the computer transitions into a stand-by (sleep) mode during which it consumes minimal power, while still monitoring all input ports for incoming data. Depending on the stand-by mode, the PC responds to inputs such as an incoming fax through the PCI slot, a keystroke on the keyboard, a mouse click, or an incoming photo of a USB-connected digital camera, by resuming normal operation in a timely manner. IAPC systems may be able to modify their performance by clock throttling and changing the CPU core voltage on the fly, to match user and application demands. These, and other advanced modes of operation, enable the computer systems to consume energy in the most efficient manner, while providing an enhanced user experience.

Hardware and software features

The restriction of power management algorithms by the information available to the BIOS that implements them, the lack of a well-specified power management and configuration mechanism to address advanced system architectures, such as Universal Plug and Play, and the existence of legacy hardware such as the ISA slots, serial and parallel ports, limit the functionality and flexibility of many of the computer systems still available today and ultimately deprive them of becoming truly intelligent machines.

The Advanced Configuration and Power Interface (ACPI) Specification provides a platform independent, industry standard approach for operating system based power management. The ACPI specification is the key constituent in Operating System-Directed Power Management (OSPM). OSPM and ACPI apply to all classes of computers including handheld, notebook, desktop, and server machines. In ACPI enabled systems, the BIOS, hardware, and power architecture must utilize a standard approach that enables the operating system to manage the entire system in all operational situations. The ACPI OS takes over the power management and Plug and Play functions from the legacy BIOS interfaces (such as the APM BIOS and PNPBIOS) and allows inexpensive power management hardware to support very elaborate power state transitions, maximizing the computer's power consumption and resource utilization efficiencies.

The ACPI OS can put the whole computer or parts of it, such as the the processor and motherboard devices, in

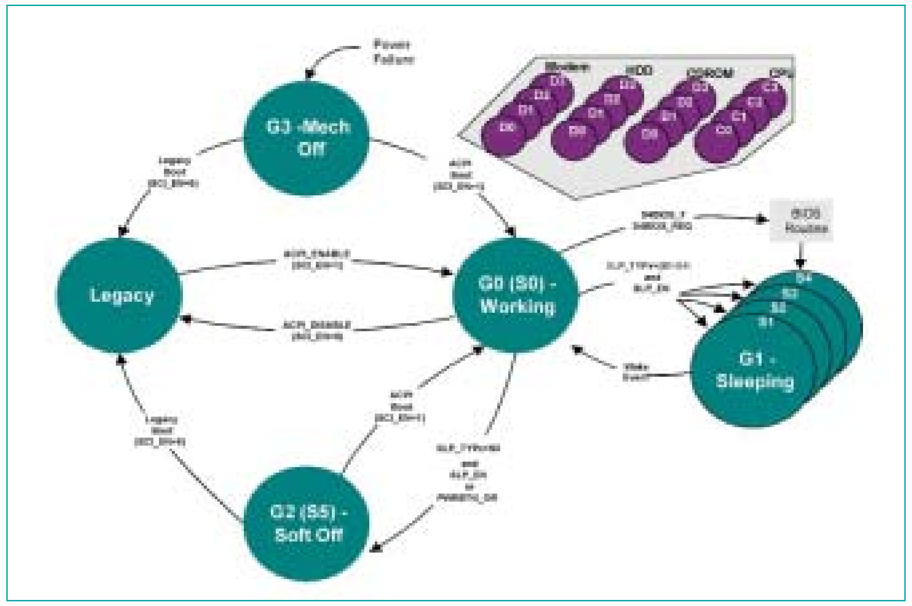

Figure 1. There are six discrete systems operating states possible.

and out of various sleep states, based on user settings and application requests. It has knowledge of which devices will be affected prior to docking or undocking, device insertion and removal, or thermal events. The OS calculates the battery remaining capacity and battery remaining life, and determines the various battery warning levels in mobile PCs. It allows other drivers within the system to communicate and use the resources of system embedded controllers.

Hardware implementation challenges

What does ACPI power management mean from a computer power system designer's viewpoint? A multitude of voltages on the motherboard and riser cards that enable the processing of audio, video, and data streams have to be generated and managed with no user intervention. ACPI-compliant computers require the generation of these multiple voltages at various current ratings as the system transitions between different sleep states. There are six discrete system operating states possible as defined in the ACPI Specification. These states are referred to S0 to S5 in order of highest to lower power consumption (Fig. 1). All states correspond to some level of power management. In the S0 state, the CPU may toggle between C0 and C1 or C2 states, and the power system must be able to respond quickly to resultant current transients. Other system components have their own corresponding power states (D0 to D3) that best match their usage profile based on user and application needs. As the system transitions into lower power states (S1 and S2), the power consumption decreases.

Lowest power consumption comes in the sleep states of S3 through S4, where the computer system slips into a virtual shutdown. A typical system will supply standby power to system memory, USB and PS/2 ports, and LAN card or modem circuitry in an S3 state. The same system will typically remove standby power to the system memory and modem when entering an S4 state, and all components except the power button when entering an S5 state.

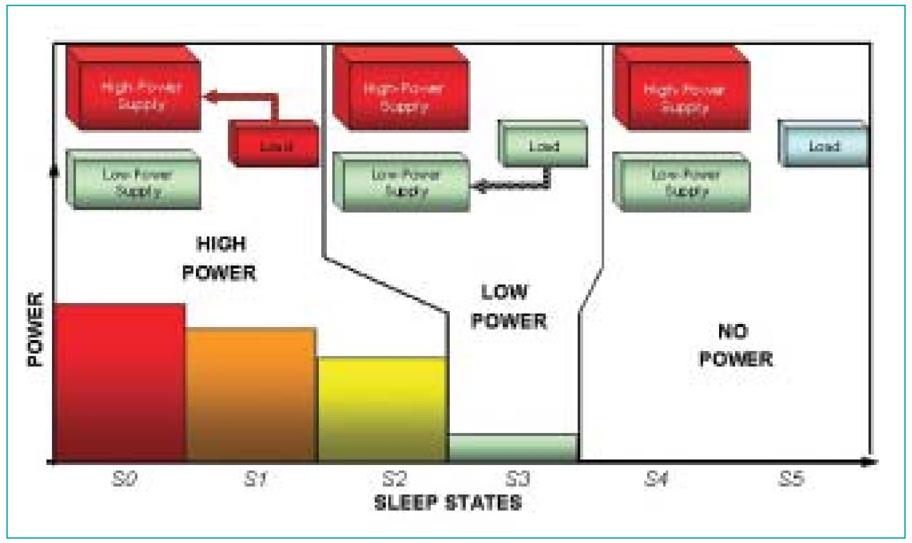

Figure 2. This concept leads to a high-power supply and low-power supply.

The deep, power saving, sleep states do not come without drawbacks. The more circuitry that is shut down to conserve energy, the longer the time that is required to restore the system to an operational status. A multitude of power management challenges arise when these systems transition between these various states. A system in an S3 state that wants to go into an S4 state must first go to an S0 state, perform the required tasks, then enter the lower power S4 state. The on-board power conversion and power management circuitry must generate and enable the appropriate voltage and current levels as the system transitions into the various states completely glitch free. Here, hardware design and implementation quality are important, as a power anomaly at any transition point could cause severe problems, including loss of user data.

The computer "dual" power supply concept

The concept of "dual supply" was introduced by Intel in the "Power Supply 98" initiative. The initiative is targeted at dealing with the different power supply demands of the computer subsystems during their operation in various states. A supply powering a computer sub-system in an ACPI environment must be able to supply the full active current, yet drop into a low-power mode when the sub-system itself slips into a low-power sleep state. To maximize power delivery efficiency, it makes sense to have a dedicated power supply for each group of active and sleep states. Thus, this concept leads to a high-power supply and a low-power supply, and matching the power needs of the subsystem with the appropriate power supply (Fig. 2)

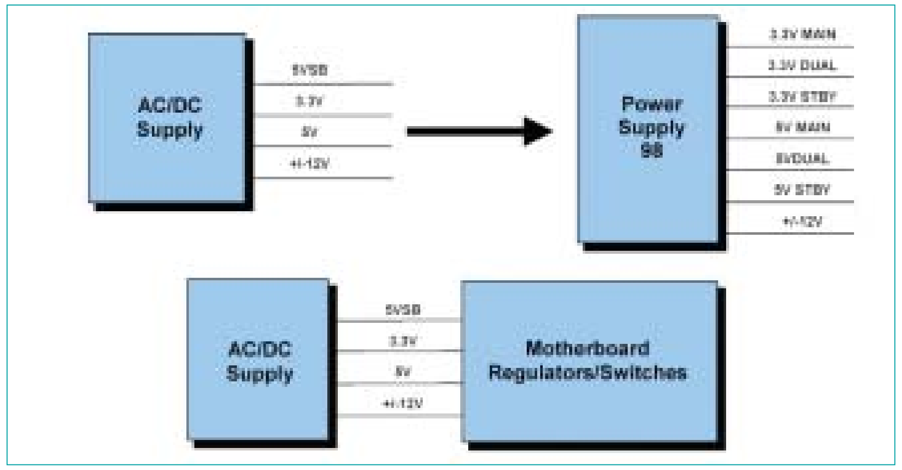

Figure 3. If the project calls for supporting only a limited set of ACPI features.

Dual supplies can be realized either within the AC/DC power supply itself or directly on the computer motherboard. However, traditional AC/DC supplies are not user-configurable. Thus, if computer manufacturers want to use a dual-mode silver box, they must pay for the cost of full ACPI support in every power supply purchased, regardless of whether the computer or the motherboard is capable of full ACPI support.

Implementing the dual supplies on the motherboard allows for application flexibility and custom configurations, as well as cost advantages if the project calls for supporting only a limited set of ACPI features (Fig. 3). In this implementation model, a series of on-board regulators and switches are required to generate these various voltages and to switch between supply rails as the various sub-systems change operating modes.

On-board ACPI power management: discrete vs. integrated approach

A fully discrete implementation may initially seem as the most simple and cost-effective method of regulating the various ACPI power states and the transitions between them. The various on-board regulators for system memory, PCI slots, Universal Serial Bus, keyboard, and mouse can be realized with voltage references, resistors, capacitors, op amps, diodes, bipolar and MOS transistors. Such discrete implementations have many drawbacks, the most important of which were the subject of many technical articles. Noise coupled into the circuits leads to "illegal" ACPI state transitions and power perturbations that can lead to loss of critical data. Switching between supplies while they have not fully stabilized, or switching several loads into the same supply line leads to power overloads, responsible for momentary brownouts, leading to output regulation falling outside design limits. Interfacing the various discrete regulators to the South Bridge additional glue logic that is not immune to system noise. Glitches may trick the regulators to enter a fault state or latch off. The typical result of data loss is a system crash, followed by a much needed reboot.

Good, discrete implementations can be realized, but, typically, a discrete ACPI power management circuit takes up precious board area, and lacks system monitoring and protection functions that could significantly reduce the Total Cost of Ownership (TCO) and prolong the life of an ACPI-compliant computer. The surface mount placement cost associated with these discrete components also contributes to a higher implementation cost. Additionally, the reliability of the computer is potentially reduced, as compared to an integrated solution, as there are many more components on the board that could fail over time (Table 1).

ACPI power circuit comparison - HIP6503 vs. all-discrete implementation

Block	Component	HIP6503	Discrete Solution	Discrete component cost (based on volume price estimation)	SMT insertion cost
Reference Block	one resistor	Internal	External	$0.01	$0.01
	voltage reference	Internal	External	$0.06	$0.01
P_OK Inverter Block	two resistors	Internal	External	$0.02	$0.02
	low power FET	Internal	External	$0.03	$0.01
2.5V memory block	four resistors	Internal	External	[illegible]	$0.04
	three low power FETs	Internal	External	$0.09	$0.03
	one switching diode	Internal	External	$0.03	$0.01
	two rail-to-rail op amps	Internal	External	$0.10	$0.02
	one 200mA NPN	Internal	External	$0.04	$0.01
3.3V dual/stby block	four resistors	Internal	External	[illegible]	$0.01
	three low power FETs	Internal	External	$0.09	$0.03
	one med power FET	Internal	External	$0.10	$0.01
	two rail-to-rail op amps	Internal	External	[illegible]	$0.02
	one 200mA NPN	Internal	External	$0.04	$0.01
5V Dual block	two resistors	Internal	External	[illegible]	$0.02
	two low power FETs	Internal	External	$0.06	$0.02
1.8V Always block	three resistors	Internal	External	[illegible]	$0.01
	one op amp	Internal	External	[illegible]	$0.01
	one 200mA NPN	Internal	External	[illegible]	$0.01
2.5V Clock Block	one resistor	Internal	External	$0.01	$0.01
	one op amp	Internal	External	$0.04	$0.01
	one 1A FET	Internal	External	[illegible]	$0.01
RC filter for 200Ps delay to S3#	resistor and capacitor	Internal	External	$0.02	$0.02
Overall component count (not including common components)		1	39		
Total discrete component cost (not including common components)				$1.80	$0.36
Common components	2.5V memory power NPN or	External	External	Benefits of HIP6503 implementation not quantified (selected)	reduced PCB area
	3.3V standby med power MOSFET	External	External		over-current protection
	1.8V always med power MOSFET	External	External		thermal protection
	5V dual low power MOSFET	External	External		fault reporting
	5V dual med power MOSFET	External	External		no illegal state switching
	Output capacitors for all outputs	External	External		noise immunity

Table 1. Comparison integrated to discrete solution.

An integrated circuit that combines all the ACPI regulators and system monitoring and protection functions needed to properly manage the operating state transitions and the power demanded, is the most economical, simple, and reliable method of ACPI-compliant motherboard power management.

The ACPI Power Controllers

Intersil's HIP6501A was the industry's first integrated device targeted at the ACPI power management initiative. The HIP6501A regulates/controls 3 voltage planes. The output voltages are fixed eliminating the need for external resistors.

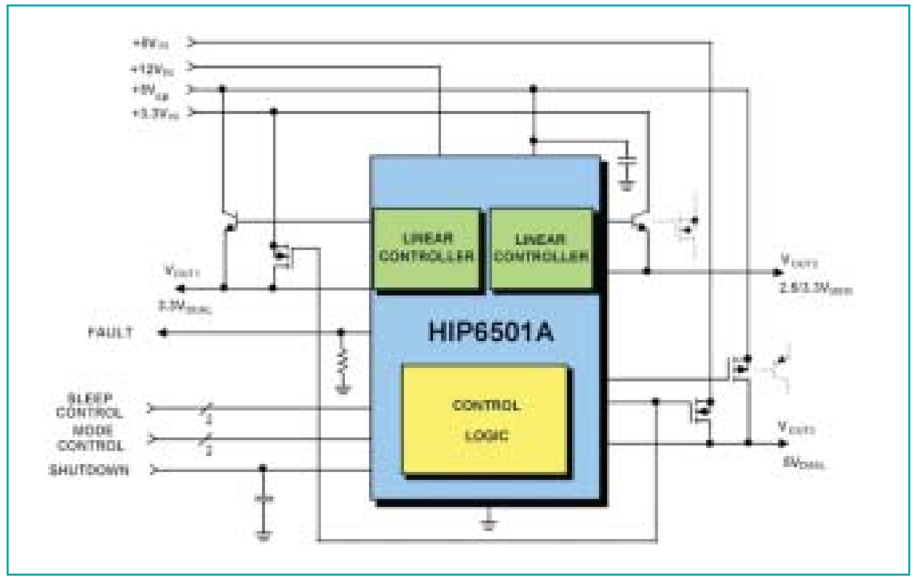

Figure 5. The HIP6501A has build-in filters for noise immunity.

The HIP6501A interfaces with the computer system through four digital lines, which allow it to be configured in four support configurations, as well as be controlled directly by the Southbridge chip. Up-integration and intelligent design allows the HIP6501A to employ only eight (8) external components while operating from within a small 16-pin narrow-body SOIC package.The HIP6501A integrates three linear controllers: a $5V_{DUAL}$ for USB/Keyboard/Mouse, a $3.3V_{DUAL}$ for PCI/Auxiliary/LAN, and a selectable $2.5V/3.3V_{MEM}$ for systems with either RDRAM, SDRAM, or DDR SDRAM memory. The HIP6501A also provides adjustable soft start, internal compensation, over-temperature and under-voltage protection with centralized FAULT reporting. The HIP6501A has built-in filters for noise immunity and requires no glue logic (Fig. 5).

The small pin count package and the small number of external components do not impede on the chip's functionality or ease of use. Wherever possible, the chip was designed to be compatible with bipolar transistors, reducing system cost when compared to implementations using entirely MOSFETs. Thus, a bipolar PNP transistor can replace the PMOS switch employed on the 5VDUAL output. For systems employing RDRAM or DDR SDRAM memory, the HIP6501A uses a bipolar NPN as a pass element of the corresponding output. For SDRAM-based systems, the NPN pass element is to be replaced by an NMOS transistor. A HIP6501A-based ACPI circuit eliminates, typically, a minimum of twenty-nine (29) external components, as used in a fully discrete ACPI power management implementation.

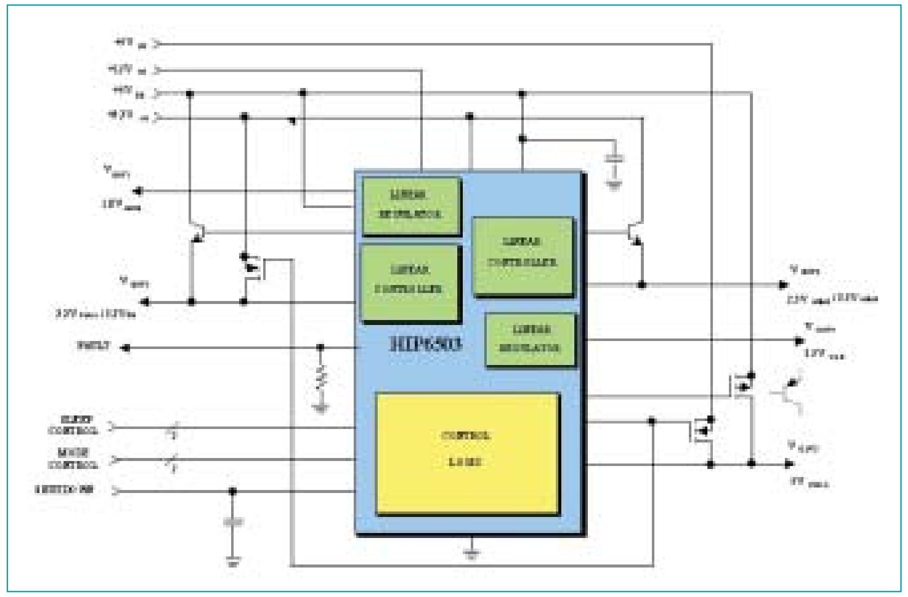

Figure 6. The HIP6503 addresses Intel ICH2-based chipset architecture.

Intersil's HIP6500B, HIP6502B, and HIP6503, each regulate and control five (5) voltage planes. In addition to the $5V_{DUAL}$, $3.3V_{DUAL}$, and $2.5V/3.3V_{MEM}$, the HIP6500B also regulates the $3.3V_{SB}$ (3.3V standby), and $2.5V_{CLK}$ (2.5V clock). The 3.3VSB output is used to power the chipset. The $2.5V_{CLK}$ output powers the motherboard clock generator in the active states only.

The HIP6502B differs from the HIP6500B in that it combines the $3.3V_{DUAL}/3.3V_{SB}$ voltage planes in one and provides two individual memory outputs ($2.5V_{MEM}$ and $3.3V_{MEM}$) for motherboards that utilize both RDRAM and SDRAM (separate video and system) memories. The HIP6500B and HIP6502B eliminate, typically, a minimum of thirty-five (35) external components, as used in a fully discrete ACPI power management implementation.

The HIP6503 addresses Intel ICH2-based chipset architectures and in addition to the $5V_{DUAL}$, $3.3V_{DUAL}/3.3V_{SB}$, $2.5V/3.3V_{MEM}$, and $2.5V_{CLK}$ voltages, it provides a fixed $1.8V_{MCH}$ output for the chipset (Fig. 6). The HIP6503 eliminates, typically, a minimum of thirty-five (35) external components, as used in a fully discrete ACPI power management implementation.

Intersil's two-power IC solution for complete PC motherboard voltage regulation

The HIP6500B, HIP6501A, HIP6502B, and HIP6503 utilize an ATX AC/DC supply ("silver box") and work in conjunction with the HIP6020/21 and ISL6523/24 four-in-one PWM (Pulse-Width-Modulated) controllers to simplify the power supply design on ACPI-compliant motherboards.

An Intersil two-regulator chipset consisting of the HIP6020/21 and HIP6501A target VRM8.4-compliant Intel Pentium (R) III motherboards employing the Intel i810, i810e, i815, Via Apollo ProMedia 133, and SiS SiS620/5595 and SiS630 chipsets (Fig. 7).

By substituting the HIP6501A with the HIP6500B, Intersil's dc/dc regulator combination addresses VRM8.4 Intel Pentium (R) III motherboards with the Intel i820, Via Apollo Pro 133A, Apollo Pro 133, and Apollo KX133 K7 chipsets.

The HIP6502B ACPI linear power controller is intended for VRM8.4 Intel Pentium (R) III-based workstation and server motherboards utilizing Intel's i840 and Serverworks' LE/HE chipsets.

An ISL6523/24 and HIP6503 chipset regulates all active and sleep-state voltages on VRM8.5-compliant motherboards featuring Intel's new Tualatin microprocessor, i815e/i815ep Memory Controller Hub (MCH) and I/O Controller Hub (ICH2/ICH3) (Fig. 8).

Conclusion

Pragmatically, IAPC power management using integrated approaches, such as Intersil's dual dc/dc regulator solutions, provide the computer and motherboard manufacturers with the lowest bill of materials cost and highest reliability, leading to a longer motherboard and computer system life.

ACPI-compliant computers provide a rich experience for the consumer and corporate user, as once set up properly, these systems require far less maintenance, and are one step closer to truly becoming the intelligent appliances we have come to expect.

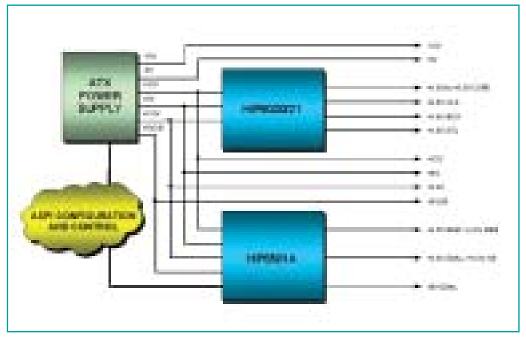

Figure 7: An Intersil two-regulator chipset.

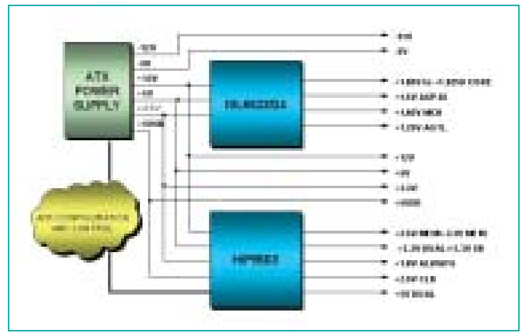

Figure 8: An ISL6523/24 and HIP6503 chipset. regulates all active and sleepstate voltage.

POWER PROTECTION

Protection of subscriber line interface cards

Withstand the surge current

A large number of hook switches are now semiconductor devices such as FETs. Semiconductor switches have a maximum operating voltage which, to avoid their damage, should not be exceeded.

Chris Likely, Cooper Electronic Technologies

There are two main over-voltage threats to subscriber line interface cards (SLICs): lightning and short circuit to the AC utility supply. The protection mechanism for these two types of over-voltage event need to be different, after a lightning strike the protection circuit needs to reset and the SLIC must continue to operate. However, mains crossing events are less common than lightning strikes and potentially more destructive, under these circumstances the protection circuit is allowed to fail in order to prevent damage to the SLIC. In order to meet these requirements the protection circuit components need to be carefully selected.

Subscriber lines can be divided into two main types, analogue and digital. Analogue lines work from a nominal –48V supply but also have ringing voltages of up to 150Vrms. Digital lines on the other hand tend to operate with a much lower supply voltage, as low as 3.3V, and use digital signals to produce ring tones in the terminal equipment. Both types of subscriber lines use SLICs and both require over-voltage protection, the main difference being in the selection of the transient voltage suppresser (TVS).

In analogue systems during ringing a voltage of 150Vrms is superimposed on top of the -48V supply giving a peak voltage of up to 270V. When the telephone is answered the loop current increases and as a result the ringing is stopped and the call is connected. Call connection normally occurs when the loop current exceeds 3mA. This mode of operation sets the minimum requirements for the TVS: it must not operate at less than 270V and at this voltage level the leakage current must be less than 3mA.

When the telephone is 'on-hook' the hook switch will be open, as shown in figure 1, any transient voltage that occurs in this state will appear directly across the hook switch.

For adequately rated electromechanical devices this is not a problem but a large number of hook switches are now semiconductor devices such as FETs. Semiconductor switches have a maximum operating voltage which, to avoid damaging the device, should not be exceeded. Hence the TVS must operate at a voltage below the hook switch voltage rating. When the hook switch is closed it must be able to withstand the surge current associated with an over-voltage event, this is often achieved by using series resistors to limit the current.

Protection from lightning strikes is normally achieved by using two or three stages of protection, as shown in figure 2.

The first protection stage is known as the 'primary protection', this generally consists of a gas discharge tube or a spark gap with current limiting series resistors and slow acting high current fusing. This stage of protection is designed to take the initial lightning voltage of >20kV down to between 1-4kV and reduce the transient period from something over 50ms to less than 1ms.

The second stage is refereed to as 'secondary protection' or 'line side' protection. This level includes protection against short circuit to the utility supply and generally consists of a fuse or positive temperature coefficient resistor (PTC) a TVS and possibly a resistor in each line. The effect of this stage is to reduce the 1-4kV transient down to less than 50V. The final stage is normally only require in digital applications in order to protect the low voltage CMOS circuitry, it reduces the 50V transient to less than 10V.

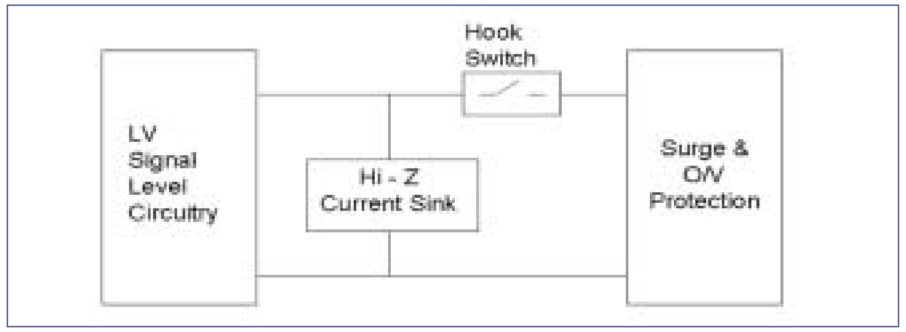

Figure 1: Hook Switch Circuit

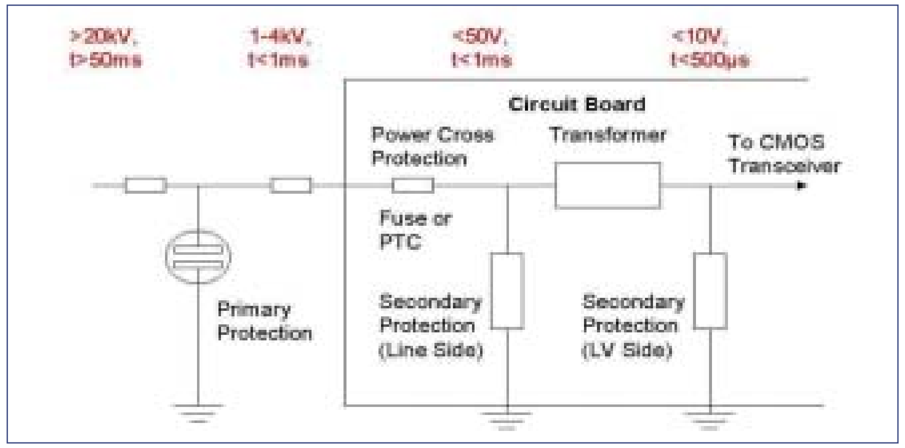

Figure 2: Stage of Lightning Protection

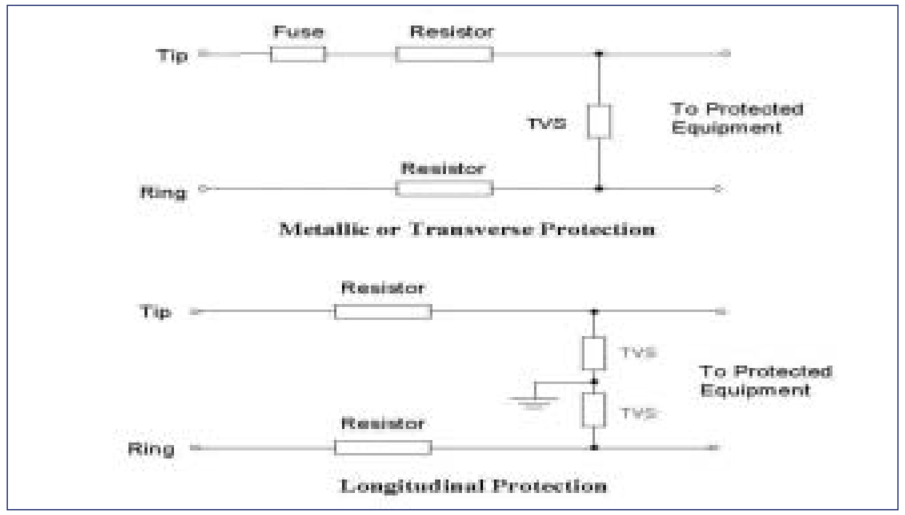

Figure 3: Types of Lightning Protection

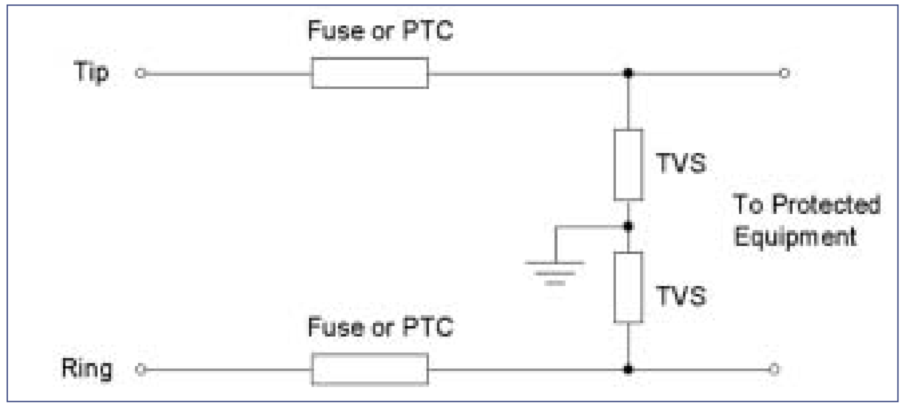

Figure 4: Typical Line Side Protection Circuit

The line side protection is designed to protect against the two main types of lightening induced over-voltage event. These are metallic or transverse protection that is required to protect against direct strikes on the overhead lines and longitudinal that protects against induced over-voltages due to ground strikes effecting under ground cables. Figure 3 shows the protection circuits required for these types of over-voltage transient and figure 4 shows a typical line side protection circuit.

The use of series resistors in each line is common practice when using a fuse for protection from short circuit to the utility supply. The resistors limit the peak current during over-voltage events allowing the use of a lower current rated TVS and less robust fuse. As mentioned previously this technique can also be used to protect the hook switch. In order to save space and reduce cost it is common practice to replace the fuse and resistors with PTCs which provide a current limiting impedance and act as a re-settable fuse.

Although PTCs are suitable for many subscriber line applications they do have some problems, both the specified trip current and holding current values vary significantly with temperature. The trip current is the current level at which the PTC becomes high impedance and the holding current is the current level below which the PTC resets after an over-current event. Both these values can vary by as much as ±50% over the device operating temperature range. PTCs also tend to be slower to operate than fuses thus allowing more, potentially damaging, energy through to the interface card.

More significantly, for subscriber line applications, the PTC will tend to reset from an over-current to a slightly different resistance each time, hence any initial line balancing will be upset after a PTC has tripped and reset. Also in digital circuits, such as E1 & T1, where the operating impedance is only 100 Ohms, introducing the additional resistance of a PTC in to the line can significantly lower output levels. In this type of application robust 'telecom circuit protection' fuses (TCP's) are the ideal solution. For more information:

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The cooling of high-power LEDs

Effective solution for rapidly dissipating heat

Osram chooses Bergquist insulated metal substrate (IMS) technology for traffic signal cooling The use of high-power LEDs in applications that have conventionally used incandescent lamps is fuelling demand for high-efficiency cooling solutions.

Mark de Vos, Bergquist

Here, we look at how The Bergquist Company's Thermal Clad Insulated Metal Substrate (IMS) material has helped lighting specialist Osram in developing its latest family of LED-based traffic light solutions.

Thanks to the potential for both energy savings and reduced levels of maintenance, highways authorities around the world are rushing to adopt traffic lights based on LED arrays rather than conventional incandescent lamps. Around 10% of all traffic lights in the US, for example, were converted to LED-based solutions in both 2001 and 2002, and the same rate of change is taking place in Europe. In China, Beijing is upgrading its traffic lights to LED-based units in time for the 2008 Olympics. Osram Opto Semiconductors is at the forefront of the development of LEDs for traffic light applications.

Benefits of LED replacement

In the USA, where a conventional traffic light can consume up to 150W, energy savings offered by LED array replacements are particularly significant. Assuming an average of eight lights per junction, for example, a large US city having several thousand intersections could expect to save over $1 million per year in energy costs alone by fitting LED arrays that consume between 15W and 20W. Conventional European traffic lights only consume around 40-60W, making the potential energy savings less dramatic, but the longer life expectancy of LEDs delivers additional benefits. At 50,000 hours typical lifetime, a coloured LED used in a traffic signal should last more than five years, compared to approximately nine months for a conventional incandescent bulb. This not only reduces purchasing costs but more significantly, saves the expense of maintenance crews, who frequently have to close a lane simply to change one bulb.

Osram traffic signals

The latest additions to the Osram Opto Semiconductor family of modular TRAFFICsignal units are designed to completely replace the incandescent lamp, reflector, lamp socket and front disk of conventional 210mm and 300mm traffic lights. To allow easy retrofitting, these LED lamps will fit into all standard signal housings and are compatible with nearly all symbol masks, such as arrows, X indicators for lane closures, and STOP or WALK/DON'T WALK legends. They are also resistant to moisture and particle ingress to IP65. Lights are available in red, green and yellow, and each achieves high luminous efficiency. Each unit comprises three modules: the LED light source array, an advanced optical system that minimises phantom effects and presents a uniformly illuminated front lens to the viewer, and an electrical driving unit.

The LED arrays used in the Osram TRAFFICsignal products are based on the company's Power TOPLED family of surface mount power LEDs. These high-intensity red, yellow and green InGaAlP and InGaN devices are housed in compact P-LCC-4 packages, have forward current ratings (IF) of 70mA, and power dissipation ratings of up to 180mW. Optical efficiencies ranging from 15 lumen/W to 30 lumens/W, and the need to comply with light intensity regulations such as those covered by the European EN12368 standard (see Figure 1), dictate that the number of LEDs used in each light is between 60 and 120 depending on the colour (fewer are required in the case of higher brightness red LEDs, while more are required for in the case of lower brightness green). And it is this combination of power dissipation and mounting density—plus the need to operate in some very high ambient temperatures - that meant Osram had to

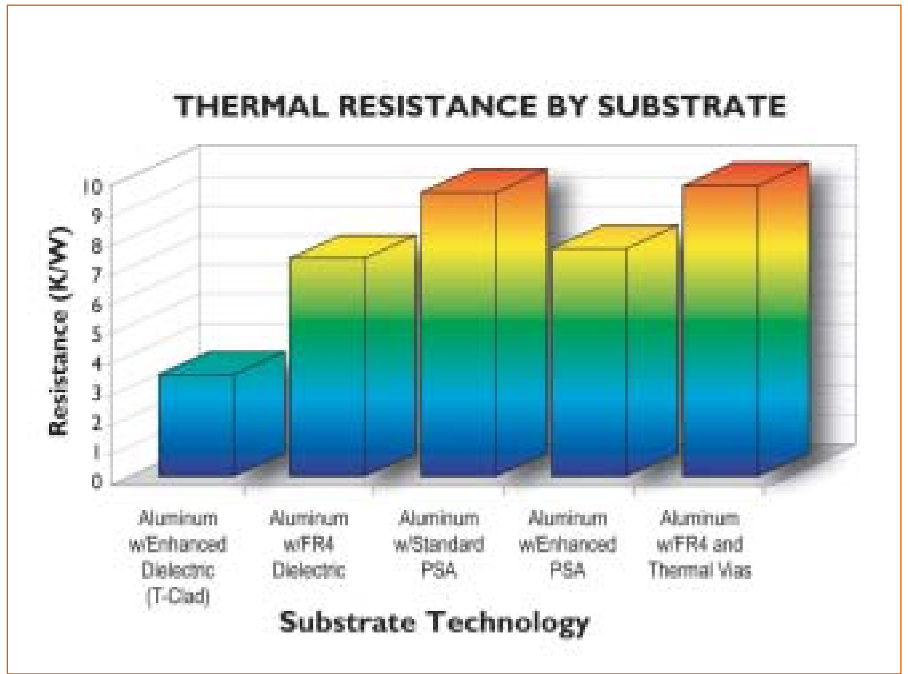

Figure 1: Thermal resistance by substrate.

find an effective solution for rapidly dissipating heat away from the LED arrays.

Heat dissipation

The cooling of LEDs has rarely, until now, been a key design criteria. Indeed, to date in consumer electronics, office equipment and most other applications employing LEDs, product life cycles are such that there is a significantly higher chance that the product will fail or reach the end of its useful life before the LEDs suffer any degradation. However, when it comes to the high-density mounting of surface mount power LEDs such as the TOPLED devices used by Osram uses in its OS-TR family of traffic signal units, cooling becomes a critical factor.

The main issue is that, while LEDs have typically been seen as 'cool running' devices, the fact is that they actually create a significant amount of heat in relation to their size. Not only can this heat build-up damage the electrical integrity of the LED (eventually leading to lamp failure), it can also affect the light intensity over time. In applications such as traffic lights where there are clear rules and regulations governing light intensity (see side panel) and where long-term reliability is essential for both cost and safety reasons, it therefore becomes important to choose materials that provide the most efficient method of heat dissipation.

As surface mount devices, the majority of heat generated by the TOPLED LED lamp is transferred to the printed circuit board through the base metal to the dielectric layer (see Figure 2).

However, during the traffic signal development, Osram found that conventional FR4 substrates did not deliver the appropriate level of heat dissipation because the dielectric layer that FR4 employs did not offer a high enough level of thermal conductivity. The company also experimented with aluminium substrate materials which, again, could not deliver the requisite levels of thermal conductivity. Eventually the search for alternative substrate materials led the Osram team to The Bergquist Company's Thermal Clad Insulated Metal Substrate (IMS) technology.

Thermal Clad Insulated Metal Substrate (IMS)

Designed originally to provide thermal management solutions for higher Watt-density surface mount applications where die size is reduced and heat issues are a concern, Thermal Clad is perfectly suited to long-life, high-power LED applications. Thermal Clad minimises thermal impedance and conducts heat more effectively and efficiently than traditional PCB materials, ensuring the lower operating temperatures needed for long-life, consistent LED operation.

Thermal Clad IMS comprises a circuit layer, a thermally enhanced dielectric layer and a metal substrate (see Figure 2).

The dielectric layer offers electrical isolation with high thermal conductivity and bonds the base metal and circuit foil together. By adjusting the composition and thickness of the dielectric, as well as the type of base material, a range of Thermal Clad solutions is available to meet a variety of power dissipation requirements. When developing its high-intensity LEDs, Osram selected a very thin dielectric material offering a high thermal performance. In comparison to common dielectrics such as reinforced fibreglass or pressure sensitive adhesive (PSA), the Thermal Clad enhanced dielectric minimises thermal resistance, resulting in more effective and efficient heat conduction. A comparison of the thermal resistance of the Osram Thermal Clad material and alternative technologies is shown in Figure 3. This lower resistance is key to delivering the high thermal conductivity necessary to meet Osram's traffic signal requirements.

Summary

LED technology in traffic signals and other types of high intensity signage offers persuasive energy and maintenance savings. The enormous number of such signals in use globally presents a valuable opportunity for manufacturers who can meet emerging national specifications. The key is to effectively dissipate the significant heat generated by such large arrays of densely clustered LEDs. Practical experience has shown that LEDs mounted very densely on standard FR4 or aluminium substrates will not meet minimum standards throughout the lifetime of the signal. Failure to dissipate this heat also compromises safety and reduces the lifetime of the lamp itself. Osram's experience has shown that the enhanced dielectric of an IMS such as Bergquist's Thermal

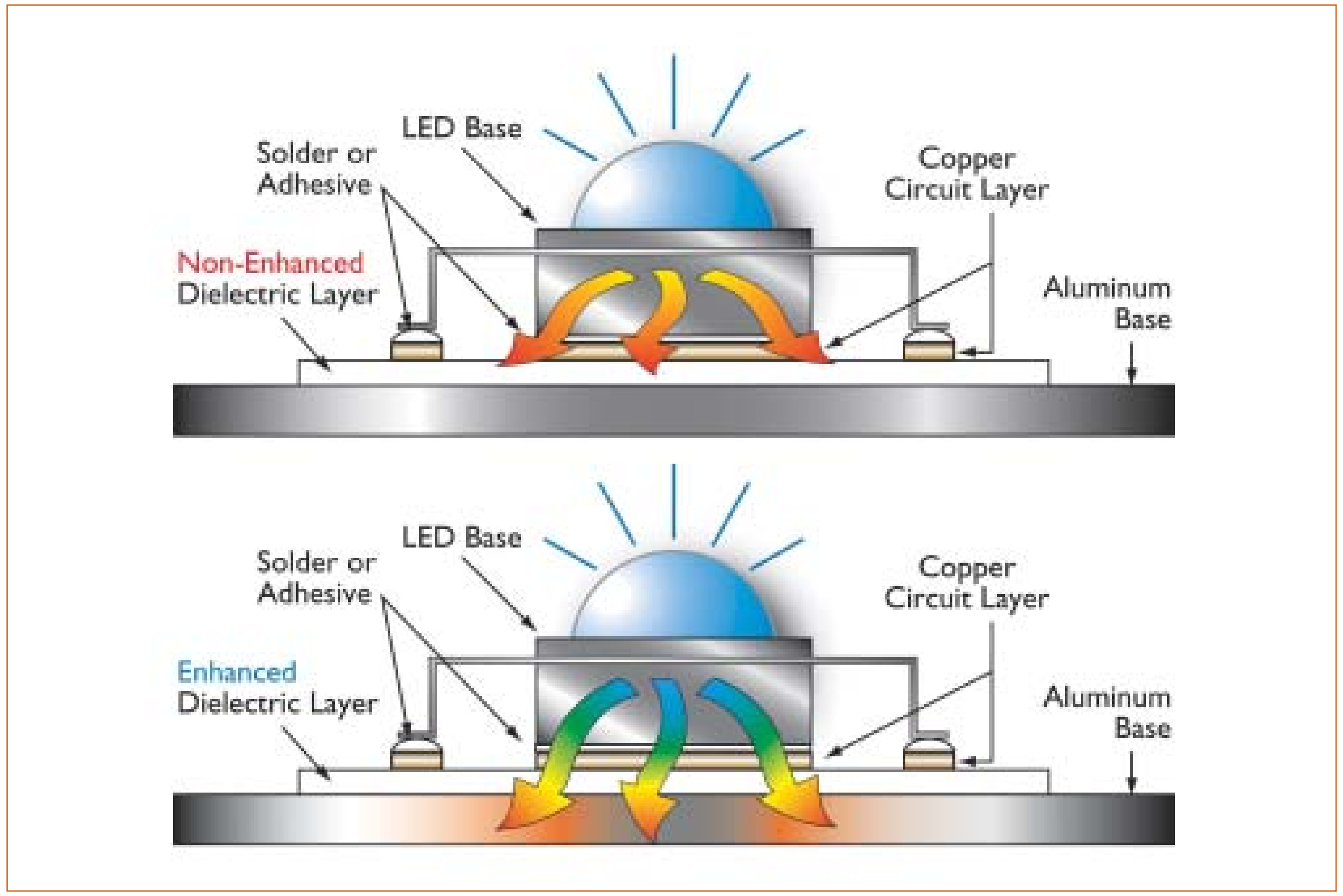

Figure 2: The majority of heat generated by the TOPLED LED lamp is transferred to the printed circuit board through the base metal to the dielectric layer.

Clad delivers a cost-effective solution to the thermal management challenge presented by high intensity LED traffic signals.

Finally, it should be noted that, in addition to traffic signals, there are a number of other applications that use LEDs where good heat dissipation is required. The 'Golden Dragon' LED from Osram, for example, can be driven with currents in excess of 300mA and is used in applications where high brightness is required from a very small area. Dissipating the heat away from this LED is a key design consideration and, again, the Bergquist Thermal Clad IMS offers a high-efficiency solution.

For more company information visit the Bergquist web site at: *www.bergquistcompany.com*

For more information on OSRAM Opto Semiconductors please visit: *www.osram-os.com*

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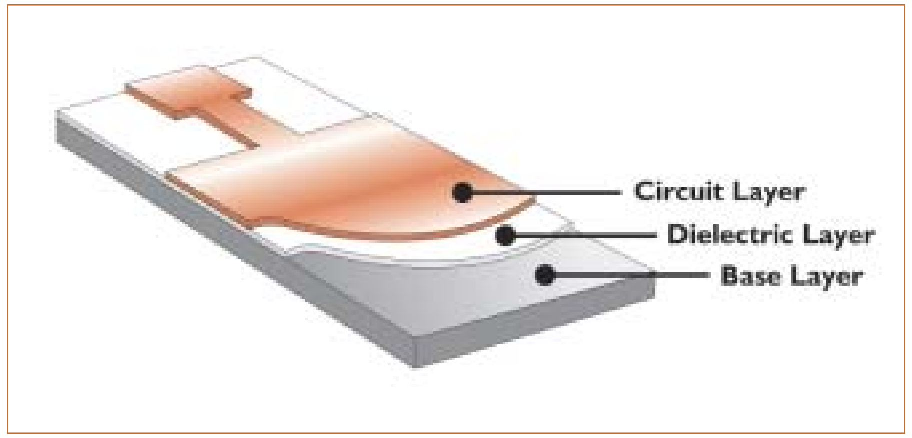

Figure 3: Thermal Clad IMS comprises a circuit layer, a thermally enhanced dielectric layer and a metal substrate.

Power management is now programmable

Programmability reduces prototype-debugging time

The power manager family provides the complete collection of functions needed for sequencing and monitoring power supplies in all 5 phases of power supply cycle; it is a highly integrated single-chip solution with all sequencing and monitoring functions in one central place.

Johannes Fottner, Lattice Semiconductor

Advanced integrated ciruits such as communication processors achieve increased performance, added functionality, and reduced power consumption in part by being fabricated using the latest sub-micron technologies. The reduction in process geometries also results in reduced operating core voltages. Inter-device communication standards, however, often dictate the use of specific I/O supply voltages, which results in devices that require multiple power supplies. Many of these devices also require that their power supplies be turned-on or sequenced in a particular order and additionally, some require that the I/O voltage be within a given voltage range of the core voltage during turn on.

While the individual functions may be easy to implement in isolation, satisfying the complete set of power supply requirements for all the devices on the circuit board present a significant challenge for today's board designers. The Power Manager series from Lattice Semiconductor is capable of performing all these power supply management functions in a single chip.

Power Manager Architecture

Being the first mixed signal PLD in the world the Power1208 and Power604, packaged in 44-pin TQFP packages, provide the following programmable modules to implement sequencing and monitoring functions (figure 1):

- On-board ispMACH sequence controller CPLD
- Delay timers (for sequence delays and watchdog timers)
- Internal oscillator for precision timing and clocking the CPLD
- Multiple analog inputs with programmable precision analog threshold
- Buffered comparator outputs
- Programmable N-channel MOSFET drivers (Power1208 only)
- General-purpose open-drain digital logic outputs
- General-purpose logic inputs

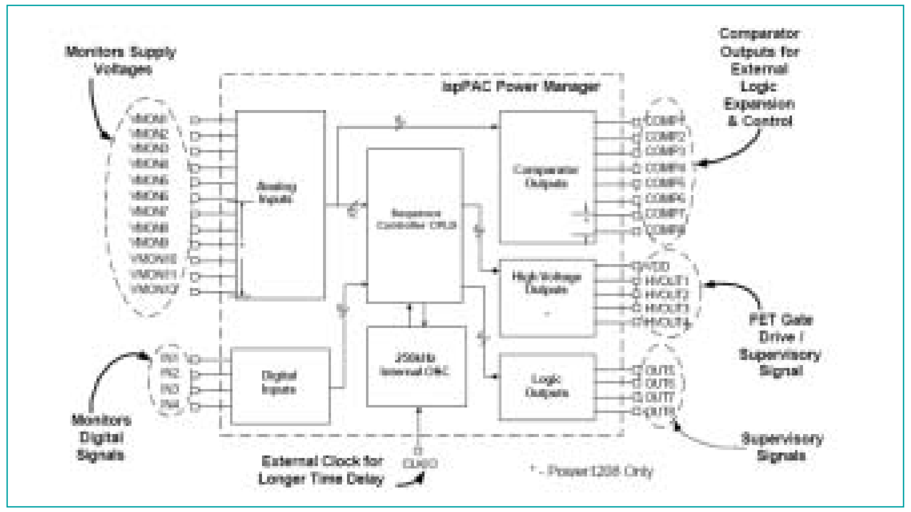

Figure1. Power1208 and Power604 block diagram.

Feature	Power1208	Power604
Power Supply Sence Inputs	12	6
Supervisory Control Outputs	4	4
High Voltage FET Drivers Digital Outputs	4	—
Reprogramable Timers	4	2
Embedded CPLD Macrocoils	16	8
Operating Voltage	2.25V to 5.5V	2.25V to 5.5V
Package	44-Pin TQFP	44-Pin TQFP
Odering Part Number	ispPAC-POWER1208-01T441	ispPAC-POWER504-01T441

Table 1: Comparison of Power1208 and Power604 functions.

The Power Managers' embedded CPLD is derived from that of the ispMACH4000 CPLD.

Inputs for the CPLD block are derived from the comparator outputs, the logic inputs, the internal clock generator and the delay timers, which enable the Power Manager to realize any combination of voltage sequencing and monitoring. Programmability of both analog and digital functions makes it easy to adapt to changes during the design phase.

For clarity the differences of Power1208 and Power604 are shown in table 1.

Each of the 12 analog inputs provides a precision programmable threshold comparator for logic supply voltages ranging from 1.03 V (1.2 V- 14 %) to 5.7 V (5 V + 14 %) with a typical step width of 1 %. Using external resistive dividers can extend this input range and all twelve voltages can be monitored simultaneously. The comparator outputs as such are fed to the CPLD block. In the Power1208, 8 out of the 12 comparator outputs are also fed to an open drain output, in the Power604, 6 out of 6 comparator outputs also feed open drain pins generating supervisory signals, and controlling the delay timer blocks.

Timing for the device is provided by an internal clock generator, which oscillates at 250 kHz, or by an external clock signal. In both cases the signal passes through a prescaler block with division ratios of 20 to 28. Synchronizing multiple power managers is easy by making one of them the master which then provides the clock signal which is then in turn fed to the slave devices. Depending on the use of an internal or an external clock the related pin is either an open drain output pin or an input pin.

Sequencing functions often require multiple long-duration delays. There are 4 programmable timers onboard the Power1208 and 2 on Power604. They can be individually configured to generate timing delays of up to 500 ms using the internal 250 kHz clock oscillator.

Timing delays can be extended to any desired duration through the use of an external clock.

Complete Power-Supply Management Using Power1208

The block diagram fig. 2 is an example of a power supply distribution system in a circuit board with multi-voltage devices. The Power1208 implements all power sequencing and monitoring functions. Each one of the Power1208's analog inputs is connected to a dedicated threshold comparator. These comparators offer precise, independently programmable thresholds that allow them to monitor the supply voltages for over voltage or under voltage conditions. Power up sequencing entails progressing through a series of phases, which are detailed below.

Phase 1: Input Voltage monitoring ensures that all external power supplies

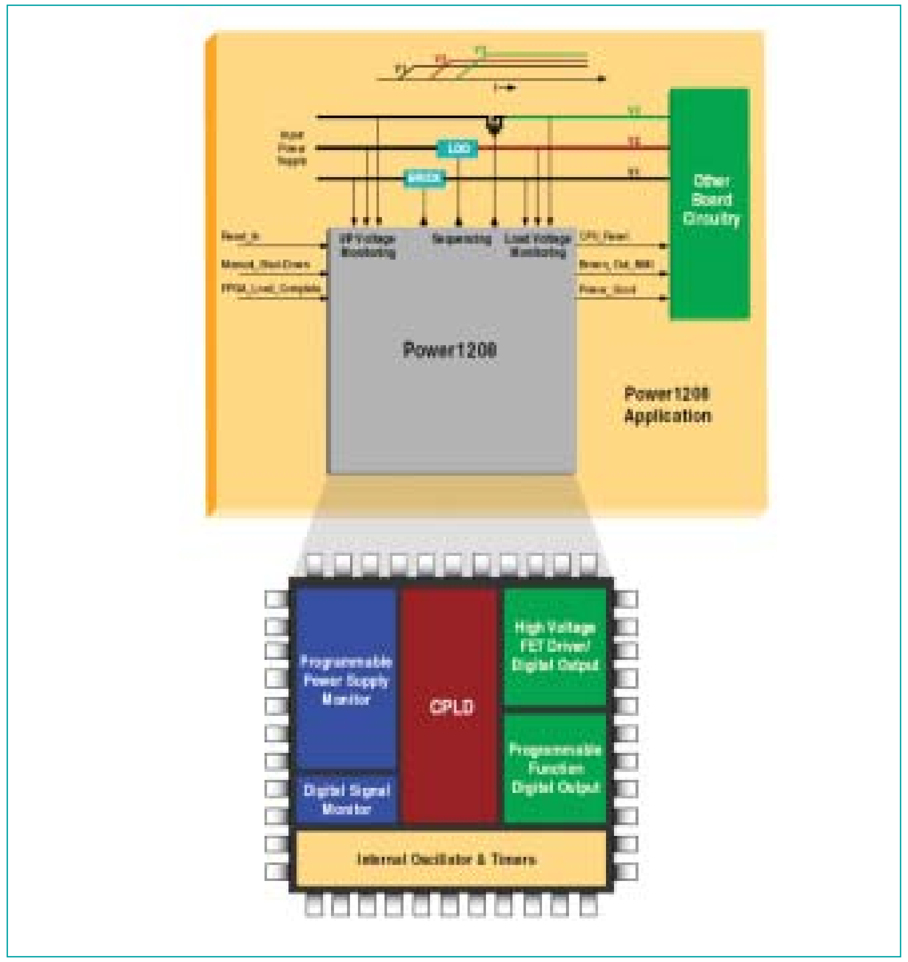

Figure 2: Block diagram of a typical Power1208 Application

are stable before the onboard power supplies (Brick, LDO, and FET) are turned on. This makes sure that the system start-up phase won't start while supply voltages are out of the specified range.

Phase 2: The voltages on the device side (V1, V2, V3) are monitored to ensure reliable power is applied to the devices. In multi-voltage systems sequencing specifications can be quite complex, e.g. core voltage first, then core voltage and then auxiliary voltages.

Phase 3. All power supply nodes (input and device side) and digital input signals (Reset_In& FPGA_Load_Complete) are monitored to generate logic control signals (CPU_Reset and Power_Good) for the system to start up. The power manager's precise delay capabilities allow the control of delays ranging from a few microseconds to seconds!

Phase 4. All power supply nodes (input and device side) are monitored for power supply faults and to facilitate generation of supervisory signals: Brown_Out_NMI, CPU_Reset, and Power_Good. Also, the Manual_Shut_Down signal is monitored to facilitate the control logic to jump to phase 5.

Phase 5. Monitor supplies to ensure controlled shut down. Integration and Programmability Benefits with Power Manager

The power manager family of Lattice Semiconductor greatly simplifies implementation of complex power-supply sequencing and monitoring systems and reduces design time.

Programmability reduces prototype-debugging time, and by programming the threshold voltages, power supply margining tests can be performed even on the production line.

The power manager family provides the complete collection of functions needed for sequencing and monitoring power supplies in all 5 phases of power supply cycle; it is a highly integrated single-chip solution with all sequencing and monitoring functions in one central place. Its robustness ensures reliable start up of the board; even under noisy power supply start up conditions and the change in supply sequencing and monitoring requirements due to component substitutions on the circuit board can be easily addressed through re-programmability.

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Power systems architectures

What's in? What's out? What is state of the art?

The Factorized Power Architecture (FPA), in concert with IC-style chip devices, provides power system designers with high performance at low cost. FPA is enabled by the power conversion chips, which efficiently process over 200 Watts of power in a power Ball Grid Array with power densities over 800 Watt/ cubic inch.

Robert Marchetti, Vicor

Distributed power has been a viable design approach for decades, albeit almost exclusively in the telecommunications domain. Board-mounted DC-DC converters, for example, were constructed with discrete components and used to convert power from a centralized supply to more usable power, typically at a backplane. Subsequently, the advent of high-density DC-DC converter modules paved the way to more widespread use of the idea in EDP, industrial, military, and medical applications. Since that time, the chorus of articles in the trade press extolling the virtues of Distributed Power Architecture has been increasingly loud and clear: centralized architecture is going or gone and DPA is king. The structure and operation of each of these power architectures is summarized in Figure 1, and they are discussed in subsequent paragraphs.

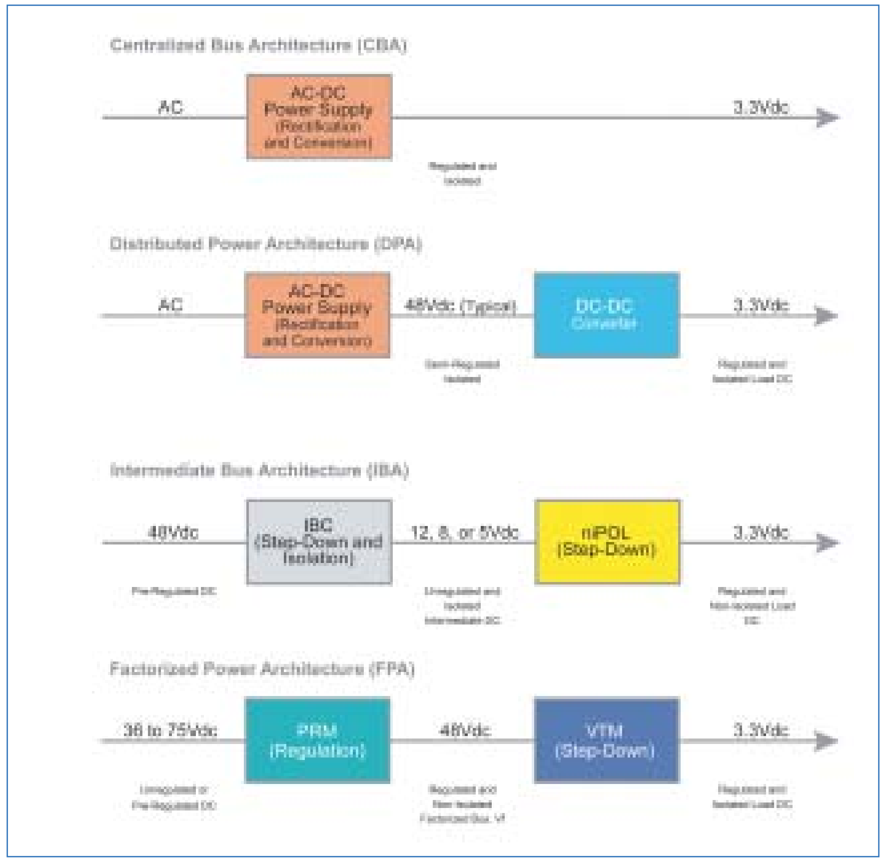

Figure 1: A comparison of the structure and operation of major power architectures.

Centralized architectures

The evolution of power architectures began with the centralized architecture. A centralized power supply contains the entire power supply in one housing æ from the front end through the DC-DC conversion stages. It converts the line voltage to the number of DC voltages needed in the system and buses each voltage to the appropriate load. It's very cost effective. It doesn't consume precious board real estate at the point of load with the power conversion function. It's relatively simple to manage thermals and EMI. It is fairly efficient because it avoids serial power transformations. In the past, the centralized system, usually a custom design constructed of discrete components, was often chosen because it was less expensive. These systems, in general, work well when the power requirements, once defined, are not likely to change and space is not an issue.

The central supply should be located near the load to minimize I2R losses, and it should also be located as close as possible to the AC entry point to reduce noise radiated from the unshielded AC lines. This is often a difficult trade-off with the input cables requiring shielding to minimize common and differential mode currents that produce noise.

Centralized power works well in many respects, but the most obvious problem is how to distribute hundreds of amps common with low output voltages. Centralized power also lacks scalability. Many systems can be configured with varying numbers of PC cards representing widely varying loads (e.g., line cards in a PBX). With centralized power, the power supply must be sized to handle the maximum configured system, which could put the small configurations at a cost disadvantage.

What's more, the remoteness of the supply from the load can negatively impact the ability of the supply to react to a rapidly changing load (i.e., transient response). Also, thermal management can be a special challenge in a centralized architecture, where excess heat could amount to hundreds of watts all in one concentrated area. Large heat sinks and fans are often needed to keep the power supply from becoming overheated. System hotspots are a source of reduced reliability.

Distributed Power Architecture

Distributed power architecture (DPA) addresses some of the shortcomings of a centralized architecture. Distributed power is a decentralized power architecture usually consisting of an AC-DC converter at the AC mains serving DC-DC converters located elsewhere. The AC-DC converter might provide regulation, isolation, noise suppression, and power factor correction as well as an intermediate DC voltage, frequently 48V. This intermediate voltage is converted by DC-DC converters located at the point of the load they serve. Typically, power in a telecom system is distributed on a 48 Volt bus. On-board isolated DC-to-DC converters are matched to the load requirement. This helps with dynamic response and eliminates the problems associated with distributing low voltages around the system. DPA was actually enabled by the development of high-density bricks.

A distributed approach spreads the heat throughout the system, greatly reducing or eliminating the need for heat sinks or high velocity airflow. With temperature more evenly maintained throughout the system, reliability specifications are easier to meet.

DPA, however, can be more costly in a number of ways. For example, isolation, regulation, transformation, EMI filtering, and input protection are all done at every brick. And coming from an offline source, rectification and conversion to the distributed bus voltage are needed so that's an additional power-processing step that reduces overall system efficiency.

Furthermore, if a single DC-DC converter cannot provide adequate power or fault tolerance for a particular output voltage, multiple DC-DC converters will need to be paralleled, creating additional complexity owing to the need to connect remote sense leads from each paralleled converter to a single, common, point and the need for additional circuitry within each paralleled converter to force power sharing among the units.

Intermediate Bus Architecture

The Intermediate Bus Architecture was first to separate the DC-DC converter functions of isolation, transformation, and regulation and allocate them to two devices. The IBC (Intermediate Bus Converter) provides intermediate voltage transformation and isolation and the niPOL (non isolated Point of Load) converter provides final transformation and regulation.

IBA can be a very cost-effective solution because point-of-load converters don't require any isolation and tend to be a lot less expensive. Non-isolated POL converters within the Intermediate Bus Architecture forego isolation and high ratio voltage transformation to improve cost-effectiveness, but they depend upon a nearby bus converter to supply power at a low input voltage. On the negative side, the lack of isolation in niPOL converters make over-voltage sensitive loads vulnerable to deadly faults and the entire system to potential ground loop problems.

The intermediate bus converter introduces a power-processing step to go from, say, the 48 to 12Volts that intrinsically reduces efficiency of the system. Also, the bus converter really does need to be located close to the load, because even at 12Volts, fairly high currents need to be moved around the board so large traces or short runs are needed. The 12Volt bus itself is a bit low for efficient distribution of a lot of power. But it's too high to step down to a very low voltage because of the very low duty cycle on the switch. As a result, it is difficult to make a highly IBA system.

Factorized Power Architecture

Factorized Power Architecture (FPA) also separates conventional converter functionality into two power building blocks. This new architecture, in concert with IC-style chip devices (see Figure 1), provides power system designers with high performance at low cost. FPA is enabled by the power conversion chips, which efficiently process over 200 Watts of power in a small (less than 0.25 cubic inch) and light (less than 13 grams) power Ball Grid Array (BGA) or J-level package, with power densities over 800 Watt/ cubic inch. These functional building blocks are deployed as surface mount (SMD) components to create a flexible Factorized Power system.

Figure 2: The Factorized Power Architecture converter.

One building block, the Pre-Regulator Module (PRM), is designed to accept a wide-range supply voltage and convert it to a Factorized Bus æ a controlled voltage source æ with 97% to 99% efficiency. Another building block, the Voltage Transformation Module (VTM), is designed to convert the Factorized Bus to the voltage levels required by the load with efficiencies as high as 97%. The VTM will also provide input to output galvanic isolation.

The combination of FPA and IC chips give the power designer the flexibility to use only what is needed where it is needed. The minimal complement of PRMs and VTMs depends upon the multiplicity of outputs, power levels, individual regulation and power system fault tolerance requirements. VTMs and PRMs may be paralleled with accurate sharing for higher power or redundancy; in fact, VTMs inherently current share when inputs and outputs are paralleled. This avoids the need for a power-sharing protocol, interface signals and a multiplicity of remote sense connections.

By exploiting a zero-voltage switching and zero-current switching topology, the VTMs limit the common-mode and differential-mode noise at the point of load. For example, the output of a VTM configured to convert 48V to 12V exhibits about 12mV p-p of high-frequency ripple with just 1 _F of bypass capacitance. That noise voltage amounts to only 0.1% of the DC output.

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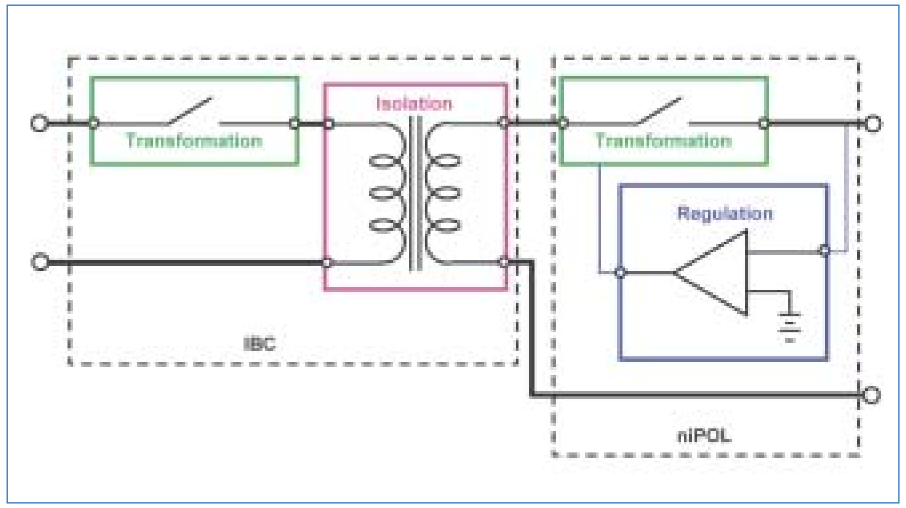

Figure 3: Function blocks of the Factorized Power Architecture converter.

Acoustic evaluation of heat sink attachment

Ensure the integrity of the heat sink function

Many electronic devices employ some type of heat sink to remove heat and prevent the device from failing. Low-power integrated circuits (ICs) often depend on the conduction of heat through a die attach layer onto the die paddle.

By Tom Adams, consultant, Sonoscan, Inc

Since the thermal efficiency required in low-power systems is not generally very high, defects such as voids may be present in the die attach layer without having a significant impact on the heat sink function.

In high-power devices, the subtraction of heat from the device is much more critical, and the thermal efficiency required from the heat sink system is much greater. For example, the die attach layer between a very low-power IC and its die paddle might contain voids (trapped air bubbles) over as much as 40% of the area of the die attach without causing device failure from overheating. In a high-power device, the presence of any voids might be enough to lead to thermally-caused failure.

How ultrasound images heat sink attachment

To ensure the integrity of the heat sink function, acoustic micro imaging can be used to image the attachment layer between the heat sink and the device. In many devices, this layer consists of solder, but it may also consist of a thermal grease or another type of adhesive. If the attachment layer is homogeneous and without anomalies, the acoustic image of the layer will show no features. But if the attachment layer includes a void (or any other type of gap), this anomaly will show up distinctly in the acoustic image.

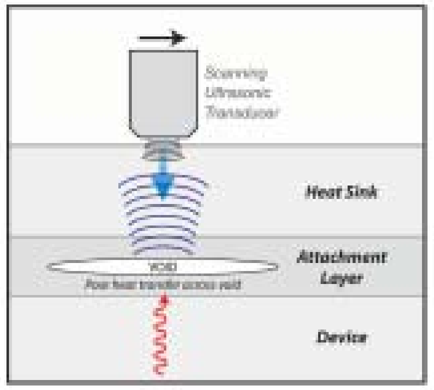

Figure 1: Acoustic image through a heat sink attached to the back of a PC board. The transducer scanned the surface of the heat sink, and the return echoes were gated at the attach layer depth. Two components are visible because cutouts through the board attach them directly to the heat sink. The numerous red areas are voids in the solder attach layer.

Acoustic micro imaging uses a scanning transducer to pulse ultrasound into the heat sink and to collect the return echoes (Figure 1). Pulsing and signal collection both take place several thousand times a second as the transducer scans the heat sink. Each return echo becomes a single pixel in the completed acoustic image. The velocity of ultrasound through most production materials is quite high, and the elapsed time for the pulse-echo round trip is usually on the order of a few nanoseconds.

Despite the high speed of transmission of ultrasound, return echoes from various depths arrive back at the transducer at slightly different times. It is the usual practice to gate the return echoes via a time window, with the result that only those echoes from a desired depth are used to assemble the acoustic image. In the case of heat sinks, this depth is usually the attachment layer between the heat sink and the device itself. Ultrasound is reflected only from the interfaces between materials, and the heat sink itself is presumed to be structurally homogeneous and therefore lacking in acoustic features.

Finding voids in heat sink attachment

Figure 2 is the acoustic image made through a large-area heat sink that has been applied to the back side of a PC board. This is a low-power application, but one that demonstrates nicely the acoustic imaging of heat sink integrity. The return echo signals were gated on the solder layer attaching the metal heat sink to the PC board. The weave pattern of the board is visible, as are irregularities in the heat sink attach layer. The outlines of two active components are visible because cutouts were made in the PC board in order to attach these components directly to the heat sink.

The key features in Figure 2 are the red regions, which are voids in the solder layer attaching the heat sink to the PC board. Their bright color corresponds (in the color map used here) to high amplitude in the ultrasonic echo signals. The voids are numerous, and will to some extent compromise the intended heat sink function. Note that there are even small voids along the edges of the two components attached directly to the heat sink.

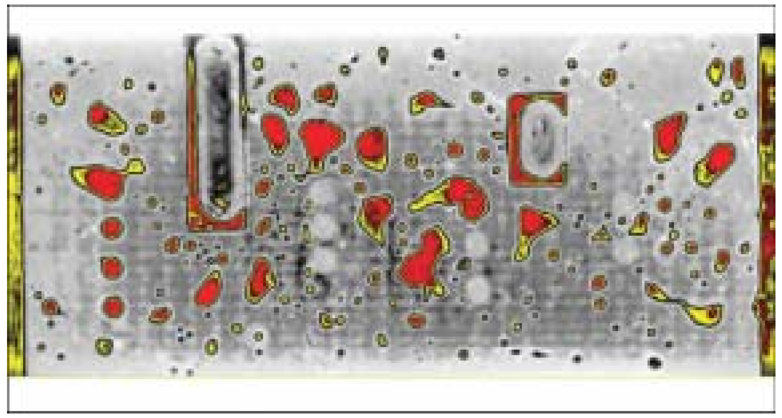

Figure 2: Thermally, a void acts as an insulator and prevents heat dissipation. Acoustically, the great differences in density and in acoustic velocity between the air-filled void and adjacent solid material causes the void to reflect ultrasound at high amplitude.

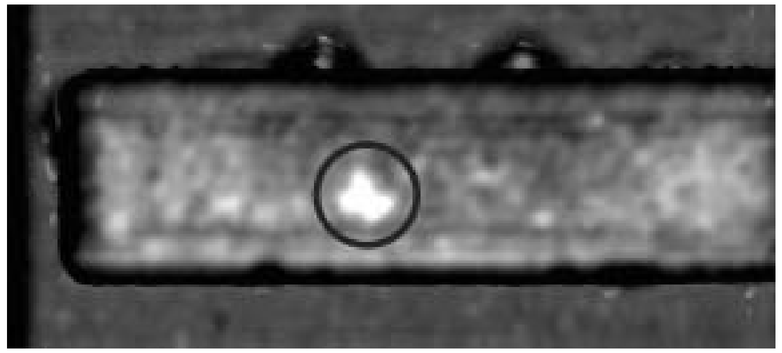

Figure 3: A critical application: the acoustic image of the attachment of a laser diode to its heat sink. The white area (circle) is a heat-blocking void.

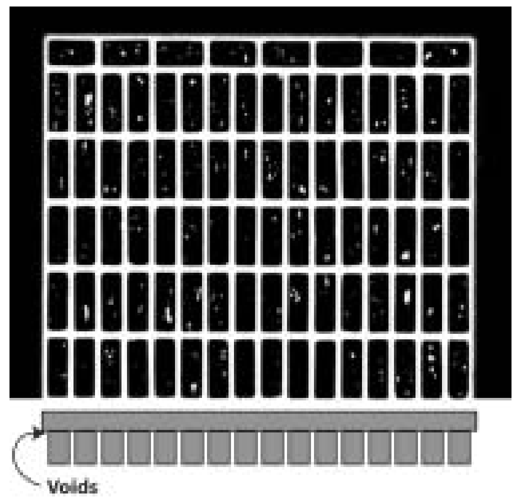

Figure 4: The attachment of a thermo-electric cooler, whose vertical vanes (white in this image) enhance heat dissipation. Black rectangles are areas where the cooler is bonded to the substrate, but these areas contain many small white voids. The diagram at bottom shows a side view.

Reflection of ultrasound from internal interfaces

Ultrasound pulsed into a sample is reflected only from material interfaces, and not from the bulk of a material. Most internal interfaces involve two solid materials, but the presence of a void means that the arriving ultrasound encounters an interface where one of the materials is air. Air (or any gas) differs so sharply in its density and in its acoustic velocity from the overlying solid material that the return echo signal from this point has very high amplitude.

The relatively low acoustic reflection from a well bonded interface between two solids means that much of the ultrasound crosses the interface and travels deeper—and this is why an acoustic micro imaging system can “reach down” through several layers of material to image a single interface of interest. A void or other gap-type defect reflects ultrasound so efficiently that essentially no ultrasound penetrates through the gap to reach deeper layers.

The vertical dimension of the void is relatively unimportant for acoustic reflection. Recent tests show that gaps whose vertical dimension is on the order of 100Å to 1000Å reflect ultrasound with about the same efficiency as much thicker gaps.

Heat sinks in high-power applications

Figure 3 is the acoustic image of a thermally critical application—the attach of a very thin laser diode to its heat sink substrate. Because of the high thermal output of the diode, no voids can be tolerated in the attachment layer. The bright spot (circle) in Figure 3 is a void, conspicuous because of the high amplitude of the echo signals being reflected from the void.

Because laser diodes are themselves very thin (typically between 75 and 100 microns), earlier acoustic imaging systems could not easily gate on the very restricted depth represented by the attachment layer. This problem was solved by the development of higher acoustic frequencies (230 MHz, 300 MHz) that make such precision a routine matter.

Figure 4 is the acoustic image of a thermo-electric cooler. Although the structure of the thermo-electric cooler is more complex than the structure of most heat sinks, the basic principle is the same, and voids at the attachment layer will cause a reduction in heat subtraction function. The black rectangles in Figure 4 are the solder attach of the vertical cooling vanes that increase the surface area. Small white areas are present within the outline of the solder bonds. These features correspond to voids and show the same reflection level as the non-bonded areas between the vane bonds.

Measuring the thickness of the attachment layer

In some applications the absence of voids in the attachment layer is not in itself enough to ensure efficient heat removal. The precise thickness of the attachment layer from one side of the heat sink to the other is also important. If the attachment layer is too thick or too thin, the device may fail, even if no voids are present.

A method developed at Sonoscan (www.sonoscan.com) uses acoustic micro imaging techniques to measure the thickness of the attachment layer nondestructively and with great precision. Measurements are performed at Sonoscan's applications laboratory, and are useful in establishing process parameters for the successful attach of a heat sink to a device under development.

Variations in the thickness of the attach layer can also be demonstrated graphically. At each pixel point, the time difference across the thickness of the attach layer is measured, and colors are assigned to various thicknesses.

Figure 5 shows the thickness profile of the solder attach layer of a direct bond copper substrate to its heat sink. Thickness corresponds to the color map at the left, where red indicates the thinnest attach layer. The thickest regions of the attach layer (green) are at the center because the substrate was slightly warped. There are also numerous voids of various sizes in the attach layer. Although the substrate is warped, the voids are all at the same level and therefore all have the same color.

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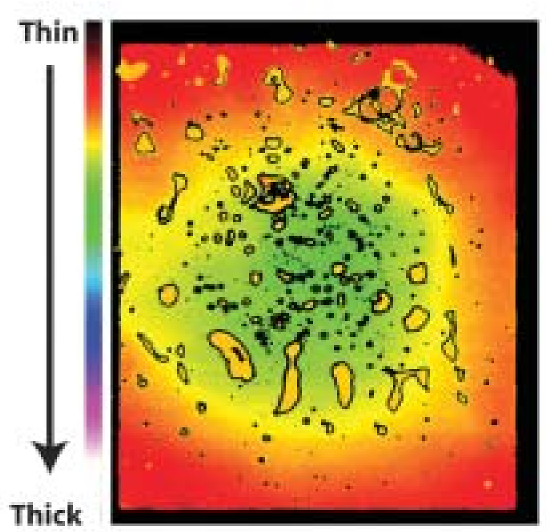


Figure 5: Color visualization of the thickness of the attachment layer. In this acoustic image of the attachment of a direct bond copper substrate to its heat sink, red areas are thinner, and green areas thicker.

Rectifier Bridge

The Easy1 housing offers a well suited module concept for a compact and cost-effective integration of power semiconductors with a footprint of only 33 x 45 mm.

The Easy module series devices demonstrate excellent performance which was now transmitted into a new topology. This newest available topology, called EasyBRIDGE1, extends the existing Easy family with an uncontrolled three phase bridge rectifier including an integrated brake arm. Such a topology provides best adaptation to EasyPACK modules and even Econo modules, due to the common height.

The product range for EasyBRIDGE modules covers the voltage range VRRM (repetitive peak reverse voltage) for 800V and 1600V at an output current for I_d = 50A resp. 40A.

Further addressed to market requirements, EasyBRIDGE modules will be available additionally in versions with improved surge forward current of approx. 60%.

With these extensions, the product portfolio of Easy modules, realizing input rectifier, brake chopper and inverter, are applicable for motor ratings up to 5,5kW.

www.eupec.com

Power Quality Analyser

LEM has introduced an “Advanced function” for its MEMOBOX Power Quality Analyser family. With this enhancement, all aspects of PQ analysis, network optimisation and disturbance analysis (previously only available in separate instruments) are covered in a single instrument. The new version now covers all measuring tasks needed for the operation and maintenance of an electricity supply network for a utility or in large industrial facilities.

The new function enables the user to measure and store 500 relevant parameters simultaneously over a period of up to four weeks. The MEMOBOX can be used in low- and medium-voltage networks up to 830 V peak-to-peak and captures up to four currents. Its compact size allows it to be installed into the smallest cabinets. The isolated case and accessories provide reliable protection against electrical shock.

The MEMOBOX analyses supply quality fully in accordance with EN 50160, including voltage and current harmonics up to the 50th. For analysis, the package includes the new Version 4.0 "Codam plus" software, which is accepted as the leading PQ software providing the user with clear conclusions without extensive training.

www.lem.com

Smallest 100-V Half-Bridge Driver ICs

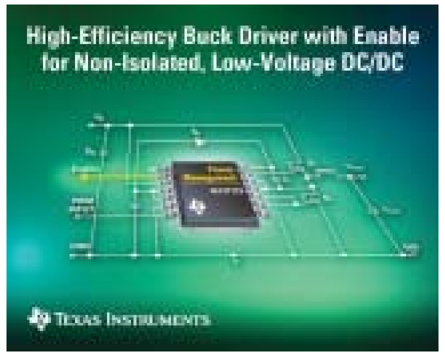
Intersil announced that the very popular HIP2100 and HIP2101 high-voltage half-bridge MOSFET driver ICs are now available in new space-saving and thermally efficient packages. The new 8-lead exposed-pad (EP or E-pad) SOIC package offers enhanced thermal efficiency and the 4 X 4 mm dual flat no-lead (DFN) package yields the world's smallest 100-V half-bridge MOSFET driver. Applications for these thermally enhanced drivers include, but are not limited to, telecom and datacom power supplies, avionics DC/DC converters, two-switch forward converters and active-clamp forward converters.

Intersil's exposed-pad device package is a thermally enhanced eight-lead small-outline integrated circuit (EPSOIC) that enables power supplies to run cooler and more efficiently. This enhanced package features a copper pad connection to the printed circuit board ground, which serves as a heat sink. Transferring heat from the MOSFET driver integrated circuit (IC) through the copper pad reduces thermal resistance by up to 50 percent and enables the MOSFET driver to operate cooler and more efficiently.

The 4 X 4 mm DFN version is sampling to customers now and will be released to full production in about sixteen weeks. It is the smallest 100-V half-bridge MOSFET driver available that allows engineers to ad here to IPC-2221 design standards for printed circuit board layout. The guidelines call for 0.6 mm of spacing between high voltage nodes in order to assure long-term system reliability.

http://www.intersil.com/HIP210X

Drivers for Non-Isolated DC/DC



Texas Instruments announced it is adding an Enable pin to its widely adopted line of high efficiency synchronous buck drivers for non-isolated, low output voltage DC/DC converters. Providing a new driver with Enable gives system power designers improved flexibility and control when managing low output voltages in central processing units (CPUs), computing, telecom, datacom and general merchant power supply systems.

The new UCC27223 driver with Enable, and the previously announced UCC27221 and UCC27222 devices produce ±3 A of output drive current for efficient power MOSFET switching at critical Miller plateau thresholds. The UCC2722x family yields two to four percent better efficiency and up to 40 percent improved heat dissipation compared to competing ICs that support low output voltages.

The UCC27223 device's Enable pin and proprietary Predictive Gate Drive digital control technology reduce diode conduction and reverse recovery losses in synchronous rectifier MOSFETs. Employing a closed loop feedback system that detects body-diode conduction, Predictive Gate Drive adjusts dead time delays in the next switching cycle to minimize the conduction time interval in synchronous rectifiers. In addition, the overall converter efficiency improves up to two to four percent.

The new driver incorporates TI's hybrid TrueDrive output stage with paralleled bipolar and complementary metal-oxide semiconductor (CMOS) transistors to allow efficient current delivery at low supply voltages.

www.ti.com

Low noise 150mA LDO

Ricoh announces the launch of R1115Z LDO Regulator. Ricoh R1115Z comes in a tiny WL-CSP-4P4 package consuming 0.94mm in PCB area and measuring L 0.97mm x W 0.97mm x H 0.59mm.

WL-CSP-4P4 package is its 0.3mm bump size, making it easily recognisable for PCB assembly machines. Ricoh R1115Z uses small ceramic capacitors keeping total PCB area consumption to a minimum. Ricoh R1115Z's high ripple rejection keeps noise to a minimum and the combination of low dropout voltage and low supply current ensure lengthy battery life. Ricoh R1115Z is ideal for creating low power consuming applications for small portable battery operated audio or telecommunication devices.

Ricoh R1115Z uses small external ceramic capacitors of minimum 1.0µF at Vout <2.5V and minimum of 0.47µF at Vout ≥2.5V. Ceramic capacitors are favourable for minimum PCB area consumption. Ricoh R1115Z output noise is kept to a bare minimum with a ripple rejection of 70dB at f=1kHz and 60dB at f=10kHz. Long battery life is guaranteed by a combination of low dropout voltage of 0.22V at 150mA and low supply current of 75µA. The product's maximum output current is 150mA.

www.ricoh-semiconductor.com

Companies in the issus

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