

Power systems Design¹

E U R O P E

Power Control Intelligent Motion

June 2004

Active PFC with Modules

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MOSFET Transconductance
Realistic Simulations
Digital Power Control
Package Selection

Innovative Boost and Step-Down DC/DC Solutions for Today's Portable Applications

TPS61020

White LED Camera Flash Application

3 mm x 3 mm

TPS64202

Single-Cell Lithium-Ion to 3.3 V at 2-A Conversion

3 mm x 3 mm

Other Low-Power DC/DC Converters

Device	Description	Price Starts at 1k*
TPS62220	400-mA, 1.25-MHz Step-Down Converter with 15-µA Quiescent Current in ThinSOT-23	\$1.49
TPS62020	600-mA, 1.25-MHz Step-Down Converter with 18-µA Quiescent Current in QFN-10	\$1.69
TPS62050	600-mA, 10-V V_{IN} Step-Down Converter with 12-µA Quiescent Current in QFN-10	\$1.79
TPS62040	1.2-A, 1.25-MHz Step-Down Converter with 18-µA Quiescent Current in QFN-10	\$2.09
TPS64200	3-A Step-Down Controller in SOT-23	\$0.55
TPS61020	1.5-A Switch Boost Converter in QFN-10	\$1.49
TPS61090	2.2-A Switch Boost Converter in QFN-16	\$1.69
TPS61042	500-mA Switch Boost Converter in QFN-10 for White LED Drive	\$1.10
REG71050	60-mA Buck-Boost Charge Pump in ThinSOT-23 for White LED Drive	\$0.90

Samples, Data Sheets and the NEW Portable Catalog ▶

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TPS64202EVM-023

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DBC Substrates for Power Modules



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0,635 mm



THIN Al₂O₃
0,250 mm

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POWER Systems Design

AGS Media Group

Katzbek 17a
D-24235 Laboe, Germany
Phone: +49 4343 421790
Fax: +49 4343 421789
info@powersystemsdesign.com
www.powersystemsdesign.com

Editor-in-Chief

Bodo Arlt, Dipl.-Ing.
Bodo.Arlt@powersystemsdesign.com

Publisher

Jim Graham
Jim.Graham@powersystemsdesign.com

Advertising & Marketing Director

Julia Stocks
Julia.Stocks@powersystemsdesign.com

Creative Direction & Production

Eyemotive
beata@eyemotive.com
www.eyemotive.com

Circulation Management

circulation@powersystemsdesign.com

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Volume 1, Issue 5



The show goes on—any show, any time, anywhere



Approaching summer I have the impression from attending many shows around the world that business is in recovery which will lead us into a positive outlook for future growth.

The PCIM Europe show in Nuremberg had attracted close to 5,000 engineers and it seems that companies have budgets again to let people travel to learn about new technology and their applications.

Power has been moved into a more important view since energy costs us more money than ever and we have to look for renewable resources. Just to burn fossils like wood coal and oil is not the way to hand over the planet to our kids.

The race for more efficiency can be found at any place in industry. The power supply in any level calls for higher efficiency. Therefore the active switches from MOSFETs in low voltage up to IGBTs in 6.5 KV range get better in their total losses, conduction loss as well the switching losses at turn on and turn off.

The semiconductor industry is working hard to fine tune the last percentages at given technologies. We have structures that constantly shrink towards an ideal point. What we miss to see is the breakthrough of promised technologies like silicon carbide in active switches. In semiconductor development, the development cycle of a new product, not modified devices on existing processes, is about 3 to 5 times the duration of an elephant pregnancy (22 months). All our simulation tools have helped to get better products, as the products get more complex the time element is critical.

It is a promising sign to see silicon carbide diodes with more ideal performance in more applications complement the active switch to minimize total switching losses between IGBT and diode.

So the European industry moves ahead to reduce power consumption in any design they can. A big issue is the consumer having his never ending needs for comfort served by more sophisticated electronics that have smart intelligent functions controlled by micro-controller putting devices to sleep when they are not needed.

The automobiles go hybrid and reduce consumption by regenerative braking. So we continue to look ahead to a number of European events in power. On the following pages for News I included a short "Power Event" section that gives you the focus on what is coming that we should pay attention to. I know that it is an impossible task to be at all of these conferences, but the proceedings are a good backup and can always be used later for self education.

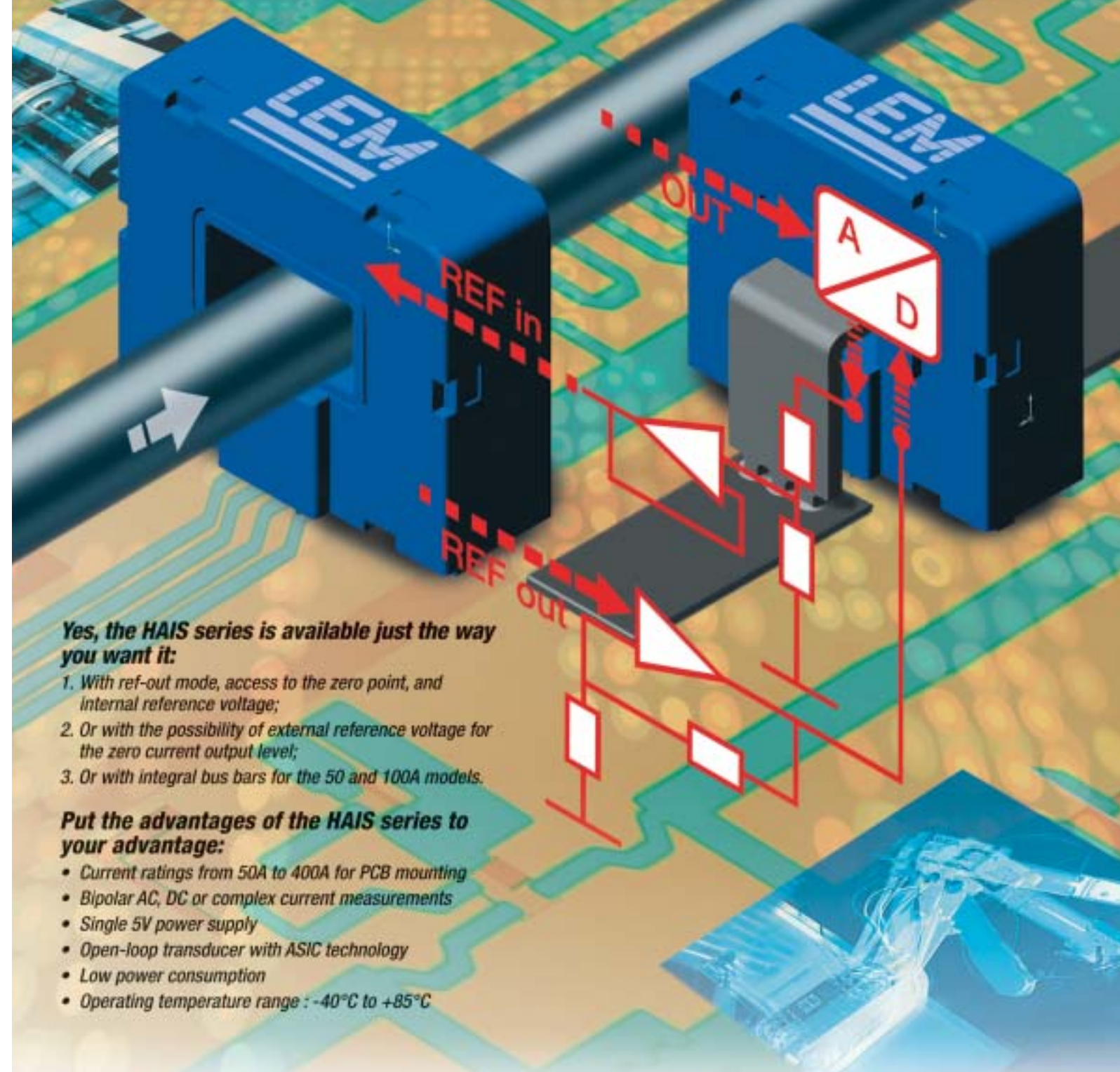
PCIM had generated a number of well recognized papers that inspire me to work with the authors to have future subjects reflected in upcoming articles in our magazine. This will give the authors a broad recognition of their research and design work as well as the benefit to our readers.

As we are Engineers we have learned how to keep a continued progress going. This is the fuel that motivates us for the next design challenge. Looking forward to seeing you at our industry's next show.

Best regards

Bodo Arlt
Bodo.Arlt@powersystemsdesign.com

An easier way to measure currents up to 400A?



Yes, the HAIS series is available just the way you want it:

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2. Or with the possibility of external reference voltage for the zero current output level;
3. Or with integral bus bars for the 50 and 100A models.

Put the advantages of the HAIS series to your advantage:

- Current ratings from 50A to 400A for PCB mounting
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- Low power consumption
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C&D announces acquisition of Datel

C&D Technologies announced that it signed a definitive agreement to acquire Datel, Inc. in an all-cash transaction, terms of which were not disclosed.

Datel is a Mansfield, Massachusetts-based manufacturer with sales of approximately \$60 million for the twelve months ending March 2004. Dattel's business is focused primarily on DC/DC converters, with additional product offerings in digital panel meters and data acquisition components. The acquisition of Dattel will provide C&D with a broader product offering, access to a diverse group of Original

Equipment Manufacturer (OEM) customers as well as an expanded international footprint, notably, including operations in Japan. Dattel has significant market presence in mid-power DC/DC converters, that will expand the total C&D offering, thereby enabling the Company to more fully satisfy customer requirements. When completed, this transaction is expected to be immediately accretive to earnings.

While subject to antitrust clearance and customary closing conditions, the transaction is expected to close in the second quarter.

www.cdtechno.com

International Rectifier investment in Wales

International Rectifier CEO Alex Lidow and Welsh First Minister Rhodri Morgan announced a major initiative to expand IR's workforce and double the production capacity at its facility in Newport, Wales.

The expansion will include the creation of highly skilled engineering and production jobs to fill the nearly 120 vacancies the Company foresees as it brings on-line its 200 mm (8-inch) wafer fabrication facility. Many of the newly created jobs will be devoted to International Rectifier's latest High Voltage IC (HVIC) proprietary technology.

With today's announcement, Dr. Lidow unveiled plans to expand IR-Newport's charter beyond leading-edge low voltage devices to include IR's next generation of HVICs, considered by many to be the best in the industry. This high value HVIC silicon, planned for production on the 200 mm line, will be used in integrated motor controllers for a variety of industrial, appliance and automotive applications.

"IR-Newport is one of our most advanced facilities and, as such, an important part of our business strategy. Since the acquisition, IR has invested over \$66 million dollars to expand our production capabilities in the 150

mm facility and has increased the staff by more than 100. With the great skill sets available here in Wales and greater Europe, and our strong relationships with the Welsh Assembly and Welsh Development Agency, we are ahead of our original expansion plans. These circumstances coupled with strong market demand lead to our decision to bring the 200 mm facility on-line," said Alex Lidow, IR's CEO.

First Minister Rhodri Morgan said, "International Rectifier is a hugely successful company with an international lead in the semiconductor market and this announcement will be very warmly welcomed in Newport and South Wales. I am very pleased that the Welsh Assembly Government has played a key role in the company's expansion in Newport through a Regional Selective Assistance (RSA) grant. Our backing for this project has been crucial in securing a future for Newport's semi-conductor manufacturing skill base and demonstrates International Rectifier's commitment to develop skilled R&D and Operations openings here in the region."

International Rectifier acquired the Newport facility in 2002. Since that time,



the facility has met or exceeded all expectations, including the consolidation of IR's low voltage trench product line production, the doubling of Newport's initial production capacity, and providing exceptional support to IR's low voltage R&D program. These efforts have dramatically accelerated IR's position in this important market segment.

International Rectifier's planned investment of \$40 million in IR-Newport will result in more than 120 additional jobs. Furthermore, this investment will also provide the potential to quadruple the facility's production capability in the future.

www.irf.com

Agilent Technologies and Digi-Key Corporation signed a distribution agreement

Agilent Technologies and Digi-Key Corporation, one of the fastest growing electronic component distributors in the world, today announced that they have signed a distribution agreement. The agreement allows Agilent's Semiconductor Products Group (SPG) to make a broad array of its products accessible to designers via Digi-

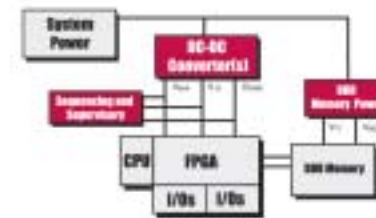
Key's vast distribution channel and real-time online service and support site.

Digi-Key's inventory of Agilent products includes a full range of LEDs and displays, RF and microwave devices and infrared and optical transceivers. These products are used in applications that span industrial, office

automation, consumer electronics, home appliances, signs and signals, wireless, networking and automotive markets.

Agilent's semiconductor products are now available through the Digi-Key Web site. www.digikey.com

www.digikey.com



Power for Your FPGA and DDR Memory Designs

Intersil's switching regulators (PWMs) maintain efficiencies in excess of 90% in your FPGA and DDR memory designs, even when the input and output voltages differ by a large amount and the current requirements range from a few milliamps to 100A. Intersil's regulators are available in several configurations including single-phase, multi-phase, integrated FETs up to 8A and up to 100A with external FETs.

www.intersil.com/data/AG

World's Only 5-in-1 DDR Chip Set Regulators

The ISL6537ACR and ISL6537BCR supply all of the required voltages along a full range of protection features and high integration in small packages. These controllers offer high performance in an ultra-small 6 x 6mm QFN package.

www.intersil.com/ISL6537

Single-Chip, 80A Capable, Two-Phase DC-DC Buck Controller

Intersil's ISL6563 two-phase PWM controller IC integrates MOSFET drivers in a thermally enhanced 4 X 4mm package to deliver a 30 to 80A power solution.

www.intersil.com/ISL6563

Small, Pre-set Output DC-DC Converter

Intersil's ISL6410 and ISL6410A switchers generate 0.5A and pin-selectable output voltages of 3.3V, 1.8V, 1.5V or 1.2V.

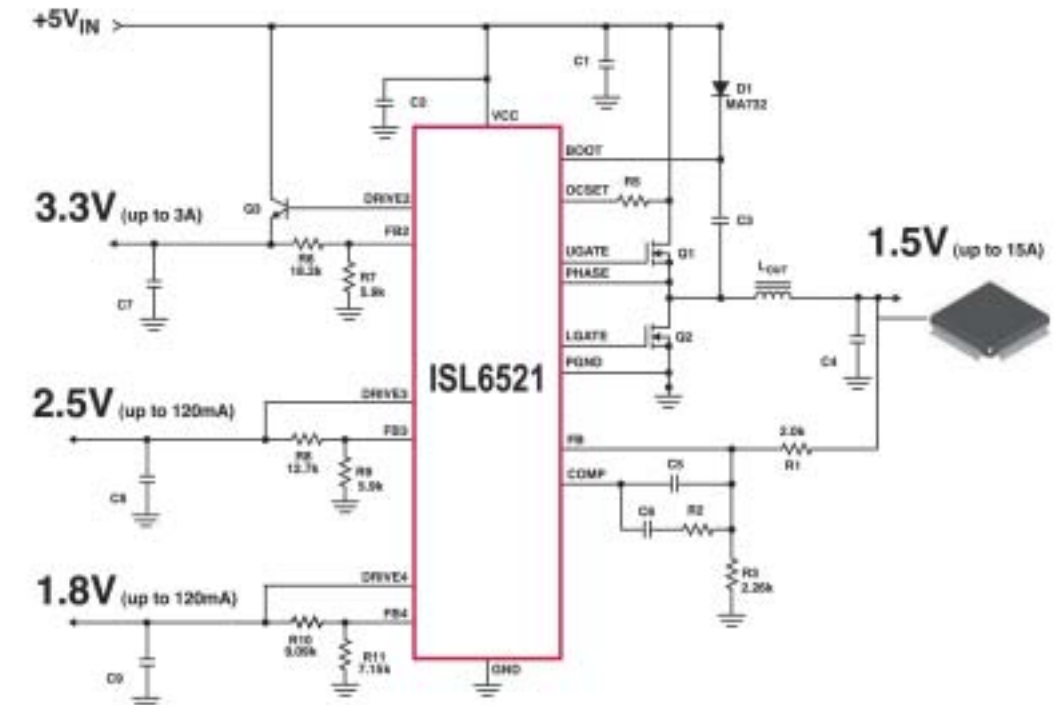
www.intersil.com/ISL6410

How Many Low Voltage Supplies Do You Need?

Multi-output DC-DC Converters from Intersil

Intersil Power Management Solutions

Each technology generation seems to create a new low voltage requirement: 2.5V, 1.8V, 1.5V, 1.25V, 1.2V, 0.9V and on it goes. Intersil offers a broad portfolio of power management ICs to easily generate the voltages you need.



Device	Regulators PWMs	Regulators Linears	V _{in}	Package/Pin	# of Output Voltages
ISL6521	1	3	5V	SOIC-16	4
HIP6021	1	3	5V, 12V	SOIC-28	
HIP6019B	2	2	5V, 12V	SOIC-28	
ISL6537 (new)	2	2 + Ref	5V, 12V	QFN-28	
ISL6532A	1	2	5V, 12V	QFN-28	3
ISL6402/A (new)	2	1	4.5V to 24V	TSSOP-28, QFN-28	
ISL6539 (new)	2	0	5V to 15V	SSOP-28	2
ISL6227 (new)	2	0	4.5V to 24V	SSOP-28	
ISL6444	2	Ref	5V to 24V	SSOP-28	
ISL6530/1	2	Ref	5V	SOIC-24, QFN-32	
ISL6528	1	1	3.3V, 5V	SOIC-8	
ISL6529	1	1	3.3V to 5V, 12V	SOIC-14, QFN-16	

Learn more about this family and get free samples at www.intersil.com/PSDE

Get more technical info on Intersil's complete portfolio of High Performance Analog Solutions at www.intersil.com/info

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HIGH PERFORMANCE ANALOG

IEEE meeting addresses Power Electronics



More than a hundred international participants of the IEEE meetings in May 2004 at German capital Berlin received an insight into the usage of power electronics in electric power systems. In particular having experienced 2003's large area grid outages in Europe and United States, the benefits of rapidly controllable high power converters as

well as the challenges related to their connection with the electric network have attracted increasing attention:

Siemens AG—Power Transmission and Distribution—High Voltage Division—presented state of the art and R&D activities regarding the use of power electronics in high voltage transmission systems, e. g. HVDC and FACTS. The challenge of high voltage high power switching is faced using actual dedicated thyristors as semiconductor valves, taking into consideration functionality like device light triggering or indispensable converter short circuit current limitation.

Alstom Power Conversion GmbH—General Drives—gave an insight into drive systems in the Megawatt range, comprising power electronics—e. g. a multi level medium voltage converter—and machines—e. g. a 5MW permanent magnet generator. The systems have been designed for applications as different as offshore wind parks, pump storage plants or railway traction.

Besides leading industry, Berlin University of Technology had invited to learn about main activities of Electrical Machines, Drives and Renewable Energies Group and Power Electronics Group within Department of Electrical Engineering and Computer Science, where machines or converters for renewable energy and medium voltage drive systems play an important role, proving the relevance of the subjects of current scientific research also for industrial development projects.

Prof. Dr.-Ing. W. Leonhard—TU Braunschweig—gave a thoughtful lecture about sustainable supply of electric energy. It is remarkable that this interdisciplinary event, linking power electronics and power engineering, has been jointly organised by IEEE Joint IAS/PELS/IES and PES German Chapters, represented by several German and international officials, in conjunction with VDE—a fruitful cooperation to be continued in future.

www.fairchildsemi.com

Texas Instruments and Ariston optimized washing machines

eupec displayed its advanced IGBT prodTI's TMS320C24x digital signal controllers leverage Field Orientated Control in three-phase asynchronous motor for low-cost, algorithm-based speed control.

Ariston, one of the leading brands of Merloni Elettrodomestici (MERI.MI), and

Texas Instruments Incorporated (TI) (NYSE:TXN) today announced that TI's -based TMS320C24x controllers reduce noise levels and improve washing efficiency. Ariston's Super Silent line of washing machines. Using TI's low-power controllers, leading white goods manufacturer Merloni

Elettrodomestici has implemented a more efficient three-phase alternating current (AC) motor with Field Oriented Control (FOC) in its designs.

For more information on TI's TMS320C24x, see www.ti.com/merlonipr

www.ti.com

CoolSET provides lowest stand-by power

Infineon announced its third generation integrated multi-chip power IC family, reinforcing the company's position as a leading supplier of power semiconductors for switched-mode power supply (SMPS) applications. The CoolSET F3 family allows SMPS manufacturers to quickly design lighter, more cost-effective power supplies with high reliability and optimized efficiency.

"The U.S. government estimates that the total amount of electricity flowing through external and internal power supplies in that country alone is more than 207 billion kwh/year, or about 6 percent of the national electric bill, and that more efficient designs could save an estimated 15 to 20 percent of that energy," said Arunjai Mittal, Vice President and General Manager, Power Management & Supply Business Unit, Infineon Technologies AG. "With the industry's lowest stand-by power consumption,

the CoolSET F3 family can contribute significantly to achieving those savings."

The stand-by power consumption of Infineon's CoolSET F3 products is the lowest currently available, exceeding the specifications of such standards as Energy Star and the German Blue Angel Eco Norm. For example, in a typical 30 watt (W) DVD recorder, the stand-by power consumption of a CoolSET F3 device is less than 100 mW. The maximum allowed for 15 W-to-50 W supplies under the Energy Star and European energy commission target specifications is 500 mW. The lowest consumption achieved by a competitive device in the same type of application is above 150 mW measured on a 10 W board.

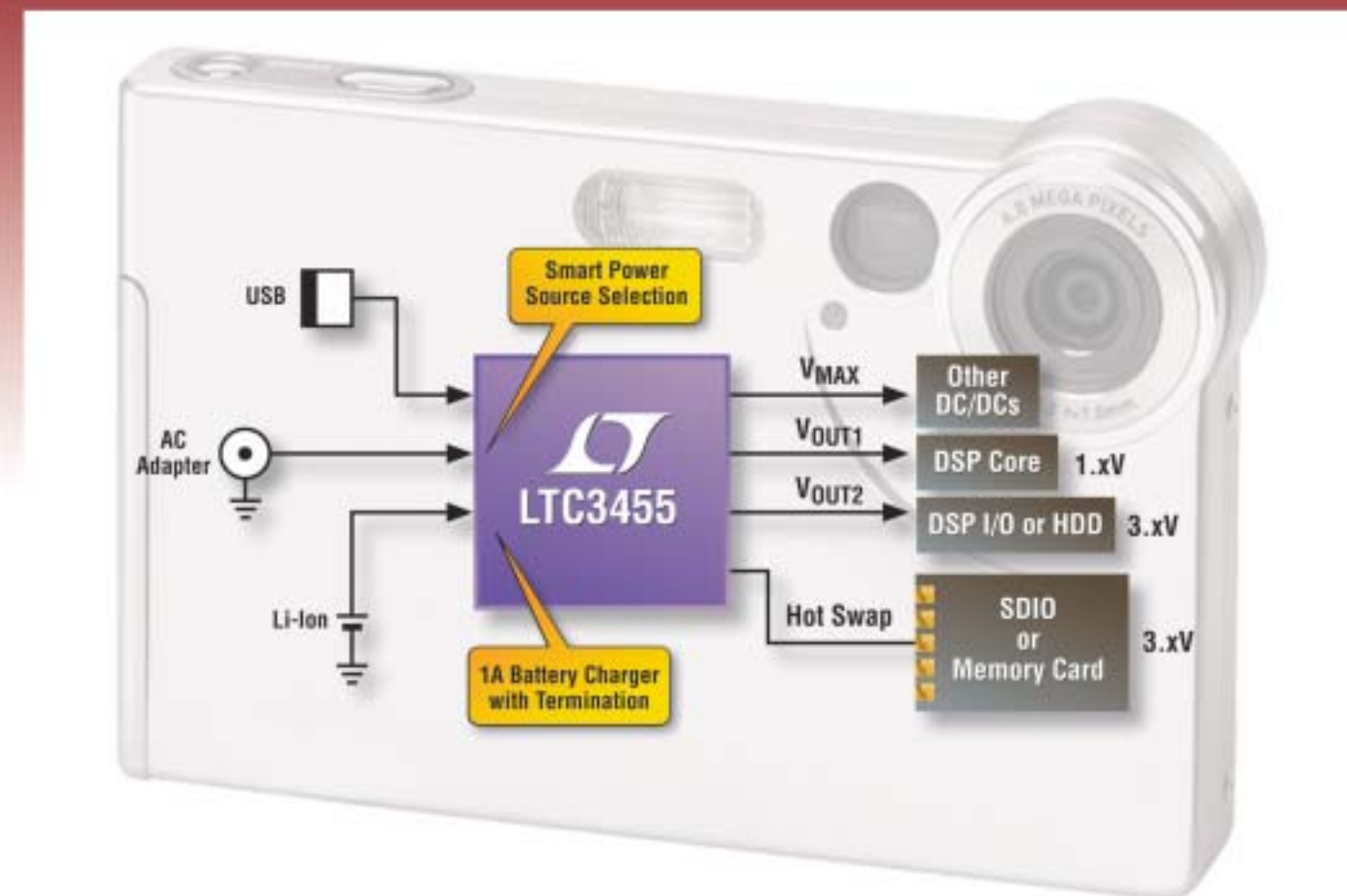
Further information on Infineon's CoolSET products is available at: www.infineon.com/coolset

www.infineon.com

Power Events

- **York EMC 2004**, July 1-2, York Racecourse UK, www.yorkemc.co.uk/emcyork
- **EPE-PEMC 2004**, September 2-4, Riga, Latvia; www.rtu.lv/epe-pemc2004
- **H2Expo 2004**, September 15-17, Hamburg, www.h2expo.de
- **Automotive EMC 2004**, October 12, York Racecourse UK, www.AutoEMC.net
- **Electronica 2004**, November 9-12, Munich, www.global-electronics.net
- **Surface Mount 2004**, November 16-18, Brighton UK, www.smartgroup.org
- **SPS/IPC/DRIVES 2004**, November 23-25, Nuremberg, www.mesago.de

Portable Power Made Easy



USB Power Manager, Charger, Dual Synchronous DC/DCs in 16mm²

Linear Technology offers a true standalone USB power manager, a full-featured linear Li-Ion charger, dual step-down DC/DC converters and Hot Swap™ controller in a 24-pin, 4mm x 4mm QFN package. The LTC3455 simplifies system power design for MP3 players, digital still cameras and PDA/GPS systems since no software or firmware are needed. Unlike conventional systems, the LTC3455 delivers full power to the system from the USB port or wall adapter even when the battery is fully depleted or removed.

Features

- Seamless Transition between Input Power Sources
- No Digital Interface or μ Controller Required
- 96% Efficient DC/DC Converters
- Switchers with Defeatable Burst Mode® Operation and 1.5MHz Switching Frequency
- Full-Featured Li-Ion Linear Battery Charger
- Can Still Charge with Power Source as Low as 4.2V

LTC3455 Typical Circuit



Info & Online Store

www.linear.com
Tel: 1-408-432-1900



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Design Efficient Motion and Conversion Applications

Power Systems solutions are key to success

Power starts at the device level based on controlling functions. The next step is to handle the power switches. The goal is to build efficient systems. To have valid cross communication for improvement

*By Bodo Arlt, Power Systems Design Europe
Editor-in-Chief*

The world is demanding more and more power to serve the peoples need of communication, travel and leisure in life. It starts with power management in handhelds like cell phones and a wide variety of computer oriented tools and toys. It is our life style enhancements and work that can be done with much more ease and efficiency. In this case we are at the low level of power consumption. The amount of devices being built reflect the growing consumption and demand for more.

All around the world engineers are working to optimize device technology and create new topologies to reduce energy consumption waste. The IC and micro-controller manufactures are the ones that look from the bottom to the top of power applications. They are optimizing chip processes and generate the right elements to control the power switches. What ever these switches are. Starting with the popular MOSFETs, having the IGBTs and continuing up to modified turn off devices in the kilo volt range.

Power supply manufactures having the MOSFETs as the active low voltage switch in the DCDC converters. Now they use the MOSFETs more and more to boost efficiency as they replace the rectification diodes by MOSFETs achiev-

ing the active rectification. As a result we have only the Rds on from the MOSFET and gain a few percentage performance that does not heat up our product. DCDC conversion gets more and more important as point of load supply is the key to modern designs. It does not matter if you look into the design on a board or more broad in a system. The driving factor to have point of load supply is the increase of transistors in ICs at higher operating frequency continues to improve IC processes with lower operating voltage. The result are higher peak currents at these loads. Therefore to optimize the supply, multiphase designs have become a standard in the industry. Also the amount of equipment being around the computer and having interface connections by wire and get powered and charged through the data link of the computer. This excess capability must be given in the system design to sense status and function to the demand and availability of power. All IC design manufactures have a focus to serve this market.

To make the power supply more easy to adapt digital controlled power supply is on its way. A great benefit in systems is fine tuning if requested to match variations in end-products that have slightly different parameters to be served. That means set the voltage exact to the

best performing level to supply the micro-controller.

All of that helps in saving energy. If we look ahead we can see that energy storage is the way to recycle the energy and reduce overall consumption. Very popular and efficient is the storage of breaking energy from transportation systems. The train, the streetcar and the hybrid vehicle do it, generate power during braking and feed it back. It is a question how much energy gets back and what source is best to store it. Super-capacitors, flywheel and batteries are the typical storage solutions. To manage all these functionable, semiconductor switches are requested. Here we see the IGBT doing it's best.

The IGBT is a little younger than the PCIM Europe show. Both are mature and we have seen the blocking and current handling capability of IGBTs growing over the years from line voltage at the mains, which are about a few hundred volts, up to substitute today GTO applications in the kilo volt range. IGBTs have reached the 6,5 kilovolt breakdown capability together with an improved save operation area they are moving into the traction applications. PCIM 2004 Conference had a number of good papers to listen to. Everybody that did not make it to the show can contact the

organizer at www.pcim.de for proceedings of the last Conference in May. The next event to look to is the PESC and chips in Aachen at the end of June.

For us in Europe Automotive is a wide field for power electronics. The classic car equipped with a combustion engine gets more and more electronics to improve combustion motor management by micro-controller and having again the IGBT as the switch optimizing the ignition. Ignition IGBTs are tailored to serve the spark plug with the proper electrical pulse. Also including ABS and all the audio and video systems available in our cars. Next generations will go to higher bus voltage. DCDC converters will help to bridge old to new standards. For alternator/generator designs we need even higher bus voltages than 42 volt. To improve efficiency without decreasing performance we need to go to these more complex power systems designs. Automotive applications require for the reliability at higher temperature, a strong interest to have a monolithic device to reduce the failure rate in systems.

Smart Power IC process technology controls functions and switches like MOSFETs on the same die. ICs need more than double amount of wafer processing steps than a MOSFET. Producing a MOSFET in the IC process technology will require the IC cost for the die space. So the technology must benefit doing things like that. Higher operation frequency can be one point. Heat dissipation has been one major topic beside cost to make that product widely usable. Breakdown voltage for these processes in general are running at and below 100 volt. More or less the amount of masks are needed makes the MOSFET very costly. So what we see is a limitation of max current in most applications. Often we have the option to add an external MOSFET as the switch for extended power range.

The range of Smart Power solutions has a wide range of application. DI electrical isolation is a way to generate reliable monolithic power ICs that have a good immunity against reverse inductive voltage that can trigger the thyristor structures in ICs based on junction

isolation. Harris had pioneered in the past the DI process technology to generate reliable products for space. It had been adapted for line interface ICs in telecom. Now we see the approach moving to higher voltage and generating the platform for full inverter designs being achieved on a single chip including the right optimized switches.

Having the right ability to envision the progress and team up with major semiconductor makers and being present at most important events like PCIM in Nuremberg and others on my list are PESC, EPE and APEC. I just named a few that get my attention to serve you with crucial information to do the best possible job in design.

Simulation had made a significant contribution to power systems designs. Nowadays we have the product virtually ready to go for production with very close to reality results. The more and more advanced software and the extraction of data from devices in semiconductors including thermal details gives the platform that allows to work straight ahead. Simulation starts on the semiconductor design level and continues to the device level and goes step for step up and includes the surrounding elements to simulate total power systems.

The computers of today have increased calculation speed together with "unlimited memory space". Working with these tools today we have much more detailed information to describe all elements with more accuracy in the model. That includes today thermal behavior, something very crucial to smart power.

Thermal management is finally the key to any long-term stable design. Simulation is the platform to do it quite efficiently. The junction temperature is the key parameter that gives the leading edge for any calculation. The maximum which is allowed and the one you chose will give you the lifetime by taking the cycling into account. Simple to say. Not easy in some cases to achieve, but that is what physics delivers to us.

When we look into power management, it depends upon the application. Individuals working on automotive controllers may define 42 volts as being a high voltage, high power. Conversely, those in Europe operating at 240 volts or 420 volts, consider any value of voltage below these values as low voltage. However, this voltage region is the most commonly used in industrial and commercial electronics.

The IC manufactures are looking to applications in communications, computer and the portable and wireless portion of that business. Here we have the strong demand to use the given energy at the best performing efficiency.

My listing for contacts below is just an introduction to key players to learn from.

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Digital processes will shape the portable market

By Dave Heacock, Vice President of Portable Power, Texas Instruments

Advancements in portable power management technologies continue to grow rapidly, keeping pace with continued consumer demand for portable devices. Portable power management circuits thrive in a diverse market, with solutions ranging from small, multi-channel power converters for wireless communication products to higher integration battery and power management circuits for digital video recorders and players. With such diversity, there are many factors affecting the entire portable power market. Two technology factors, power semiconductor processes and packaging, play important roles in driving these advancements.

Looking at semiconductor processes, the continual move to smaller geometries in high-density digital chips directly enables greater capabilities within analog and power products. New techniques and methods to improve the way system power is handled as well as driving greater efficiency improvements and power management scheme flexibility are becoming a focus for these new processes. For example, by combining high-density logic with power, greater system control and flexibility is achieved without sacrificing size and cost. In the past, many of the control functions were implemented utilizing fixed discrete combinations of analog and digital control schemes. Adding dense digital logic (0.25 micron or smaller) to a traditional power process allows digital logic to add more complex and adaptive control functions as well as accomplish the more traditional control functions.

Why is this important? The answer lies partly in the ability of the power management products to react effectively



to the changing input and output requirements. As systems continue to increase in power complexity due to multiple rails and startup/shutdown requirements, digital control provides the functionality and flexibility to meet the requirements. Input transients during start-up can require over-design of the power system. Load changes as the CPU switches operating frequency or adding or removing peripheral systems vary the load regulation requirements. Managing the power regulation under all of the varying operating conditions is a complex challenge. Although analog components can provide high speed and small size when managing linear control applications, extending these methods to more complex non-linear control may require a more complex, larger solution. Since the circuit size reduction for analog components on the integrated circuit is not as great as it is in digital logic, adding digital control under some conditions may yield a smaller solution size without sacrificing capability. With a dense digital logic process, greater control over the power regulation can be maintained than is

currently available in a pure analog process. This includes the ability to re-program a standard power management solution for a variety of application requirements as well as add nonlinear control loops to improve load regulation over wider operating conditions.

Adding dense digital logic to a conventional power process also enhances many power management features. For example, a high-speed digital communications interface on the power management unit (PMU) allows the system to adjust output voltages, modify the power sequencing and obtain the status of the converter. This control and status can lead to better efficiency and thermal management. Adding on-chip non-volatile memory further enhances the PMU by allowing flexible system configuration and improved analog performance through precision voltage references and timing control trimming. Power management IC's with multiple power converters capable of supplying 1 to 2A can exist cost-effectively on the same die with dense digital logic, improving system control, conversion efficiency and load regulation over wider input and output conditions.

In summary, power processes with denser digital capability together with chip-scale packaging will help shape the portable power market for years to come. Combining the increased "digital power" capability along with the ability to deliver solutions in a variety of footprints will enable system developers to offer more portable systems features and capabilities in their portable systems while driving solutions sizes smaller.

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Active PFC with Modules

Ensure the functionality of the power grid systems

Design concept for an active Power Factor Correction with power modules with special focus into power loss minimizing and inrush current control.

By Ernő Temesi, Michael Frisch and Peter Sontheimer, Tyco Electronics

As the application of electronic power modules is constantly increasing, new problems are arising beyond the actual discussion about the power factor ($\cos \phi$) in connection with the Power Factor Correction (PFC).

Why Power Factor Correction?

Generally, mains AC voltage is transformed into DC voltage via Rectifier Bridge and capacitor. This configuration is used for most power electronics applications.

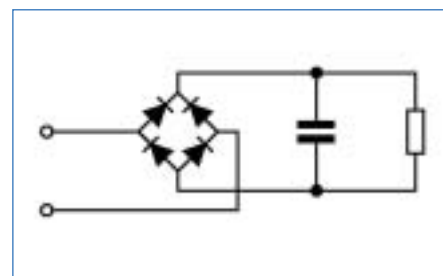


Figure 1. DC voltage via Rectifier Bridge and capacitor

In this configuration, the DC-link circuit will only be loaded, when the sinus maximum of the mains voltage (V_{IN}) is higher than the voltage at the DC-link capacitor (V_{Cap}) circuit voltage. This

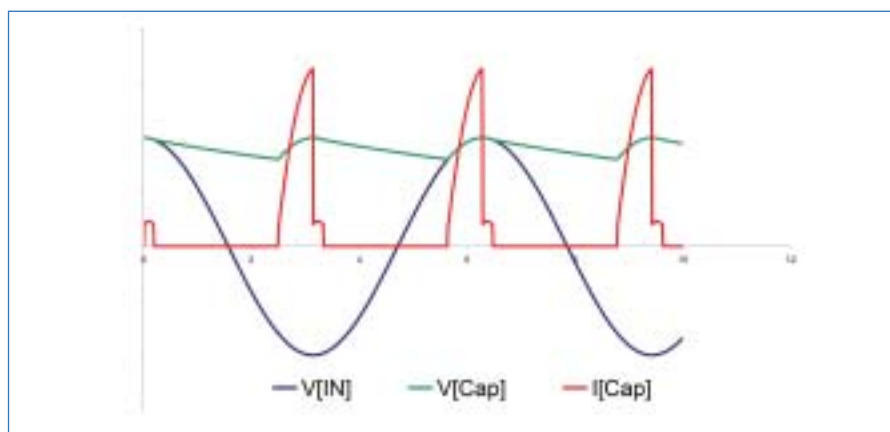


Figure 2. Current pulses.

leads to short and very high current pulses (I_{Cap}), which may interfere other users in the public power supply network.

Actions have to be taken to ensure the functionality of the nationwide power grid systems with a fast growing number of power electronics connected. Applicable international standards demand a sinusoidal current drain. Thus, the developers of power applications to be connected to the public power supply network are now challenged to care for its realization.

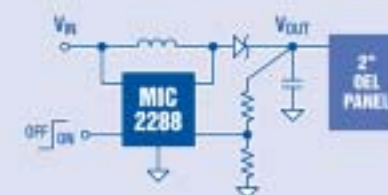
Challenge and Chance

For the development of applications with sinusoidal current consumption more design work will be required than ever before. New national and international standards and laws demand increased activities. And compliance of the applicable standards is a must today. But an active PFC also generates additional advantages, which does not generally lead to additional costs. Precondition is a system design that uses the advantages of an active PFC as smaller DC-link capacitor, loss reduction in the application connected to the

Power and System Management for Battery Powered Applications

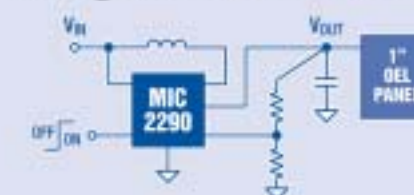
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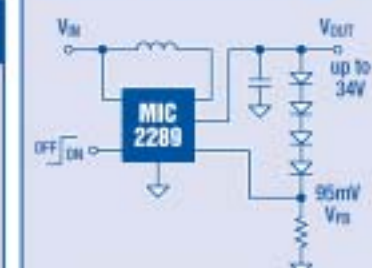
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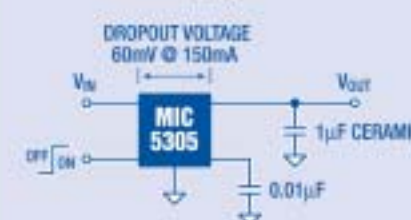
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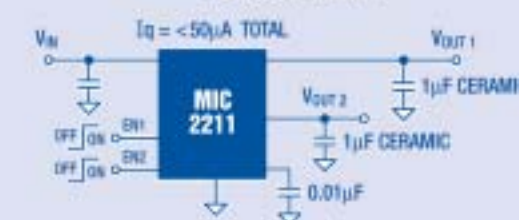
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output achieved by the increased and constant output voltage. Application examples of active PFC solutions are inverter welding machines, as by application of a PFC, the performance can be increased without affecting the mains fuse. Also converter-controlled fans for clean rooms should be mentioned. In clean room production facilities typically hundreds or thousands of such ventilators are used and the current drain from the mains have to be controlled in order to keep the system in function.

General Requirements

Some general requirements are mandatory for all these applications: compact design, low interference level, and power loss optimization. To realize an optimally compact PFC design, the switching frequency must be maximized so that extremely small PFC choke coils can be applied. To control by this caused increased power loss, the coil should have a high-performance core with thermal contact to the cooling element. New semiconductors must be suited for higher performance in order to gain smaller space requirements. At the same time it has to be prevented that the advantage is lost by the demand for a larger cooling element. Here new technologies of the semiconductor industry are opening doors. High switching frequencies are leading to considerable cost savings. A compact design leads to completely new mechanic concepts for an application, which may also lead to considerable savings in system costs. Also a positive interlinking effect can be utilized. Higher switching frequencies allow the application of smaller components for choke and EMC filter. By its compact design, EMC compatibility will be easier. And this will lead to further savings in system costs and development time.

Fundamentals of Active Power Factor Correction

An active PFC switch is basically an AC/DC converter, as its core is a standard SMPS (Switch Mode Power Supply) structure, which controls the current supplied to the consumer via a "Pulse Width Modulation" (PWM). The PWM triggers the power switch, which

separates the intermediate DC voltage in constant pulse sequences. This pulse sequence will then be smoothed by the intermediate DC capacitor, which generates DC output voltage.

PFC—Boost Switch (Boost Topology)

The boost topology acts as boost converter by converting the input voltage into a higher output voltage. This switching system is mainly used for PFC.

Two different modulation procedures can be applied, the continuous mode and the discontinuous mode.

Discontinuous Mode

In the discontinuous mode the transistor is switched on only then, when the energy contained in the choke coil is completely transferred via the diode to the electric DC output circuit. When switching on the transistor the choke contains neither energy nor current. This operation principle has therefore the advantage that switch-on losses will not be generated. Another benefit is that the choke can be very small. But this principle generates strongly increased waviness and switch off losses.

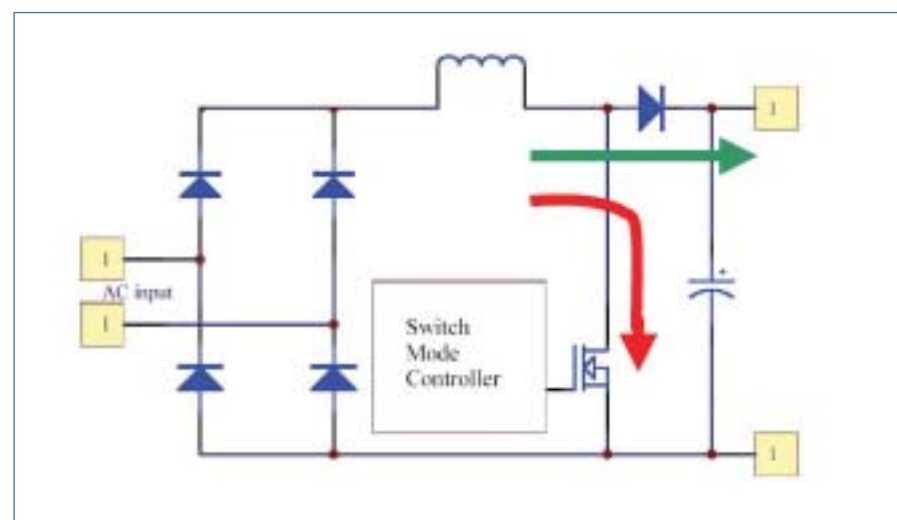


Figure 3. PFC—Boost Switch.

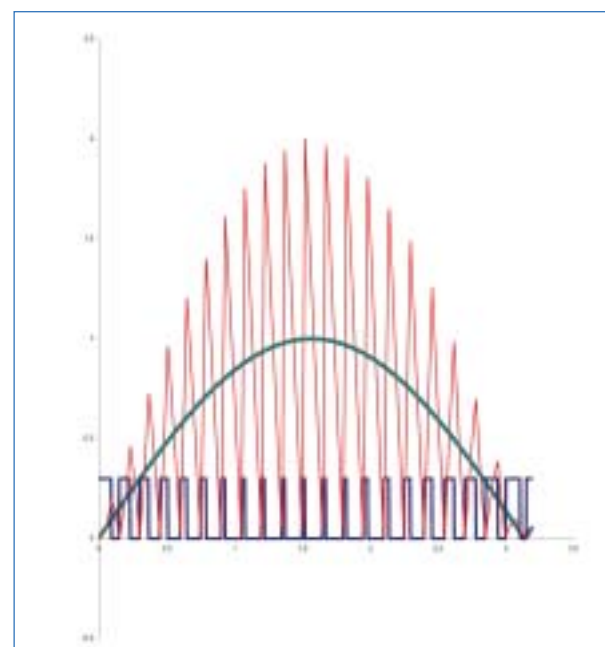


Figure 4. Discontinuous mode.

Continuous Mode

The topology is the same as in the discontinuous mode, but here varies the current in the choke closed to the sinusoidal average. In the continuous mode these large upper waves and the very high switch-off losses (caused by the double as high switch-off current) can be avoided. Therefore, this process will be preferably be used for capacities from about 250W.

He knows how important reliable technology is:

Jan M., Head of Development, Electrotechnology

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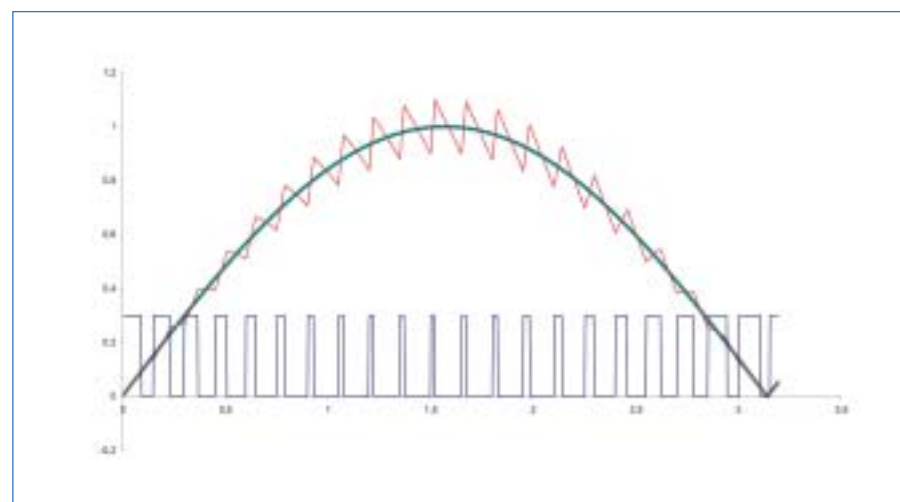


Figure 5 Continuous mode.

Design of a Continuous Mode PFC

Switch-On Losses

In standard PFC switches normally relatively low flow losses are generated compared to the switching losses. Consequently mainly the transistor switching losses are limiting the maximal switching frequency. On the other hand, the reverse current of the diode has a great influence on these switching losses generated in the power switch.

Reverse currents of the diode

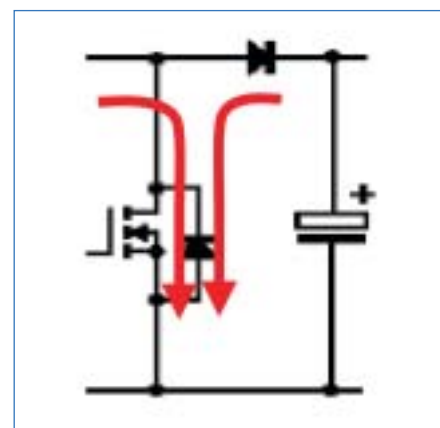


Figure 6. Switching On Losses.

increase the switch-on losses of the transistor and the application of a fast boost diode with a low reverse recovery charge (Qrr) can thus be of great importance. The boost diode has a significant influence into the switch on losses of the power transistor in the boost circuit.

Switch-Off Losses

Any parasitic inductance in the output causes a voltage-overshoot which endangers the semiconductors and increases the switch off losses. Switching-off the transistor results in a current change. This causes a voltage spike by the current change in the parasitic inductances according to:

$$V_{CE(peak)} = V_{CE} + L \times di/dt$$

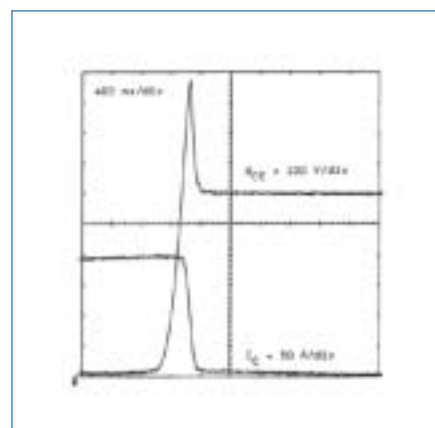


Figure 7. Switch Off losses.

To minimize switch-off losses, prevention of parasite induction loops at the PFC output is of great importance. A particularly elegant solution is to short the inductive loop with a capacitor attached as closed as possible. A fast capacitor integrated into the power component would be the optimum.

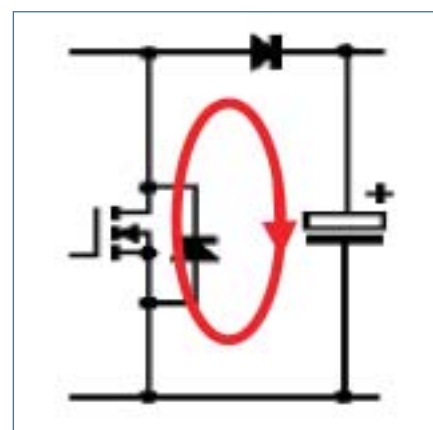


Figure 8. Short the inductive loop.

MOSFET vs. IGBT

IGBT or MOSFET? To answer this question, the efficiency of a frequency-dependent technology isn't a suitable standard. The reason is the switching of variable currents. In the range of the sinus maximum, only a short pulse will be required to increase the voltage from e.g. 325 V (V_{Peak} at 230 V_{AC}) to 400 V DC. In the zero flow range the pulse frequency is higher, but the current to be switched is then lower. For 230 V_{AC}/400 V_{DC} applications and switching frequencies of 60 kHz and more the MOSFET seems to be the better and cheaper solution.

Applications with focus on a wide input range (e.g. 90 V_{AC}, 240 V_{AC}) generate a completely different result. When applying 90 V_{AC} at the input and 400 V_{DC} at the output, also in the sinus maximum, a relatively long pulse will be required for the transformation from 127 V (V_{Peak} at 90 V_{AC}) to 400 V_{DC}. For such applications the static losses are more decisive for the performance balance of the PFC level. For switching frequencies up to nearly 100 kHz, application of very fast IGBT's seems to be more attractive. To optimize system costs, switching and flow-through losses shall always be nearly equal. As a rule, $P_{Stat}/P_{Switch} = 1$ shall apply. Balancing of switching losses with flow-through losses shall always be the target of product designers in low-cost developments.

Input Start Switch as Short-Circuit Protection and Protection against High Switch-On Currents

Output current rates of > 500 W require a specific input control, which limits the higher start-up current generated by the loading procedure of the DC-link capacitor after activation of the PFC. The switching system, for which a patent has already been filed, will not only solve this problem - moreover it also provides a short-circuit protection at the output (Figure 9).

Description of functions:

1. After application of AC voltage at the input, the SCR's of the semi-controlled input rectifier are not activated. The output capacitor is loaded via a current limiter and auxiliary rectifier. As soon as the controller begins to contact the PFC transistor, the PFC coil will be loaded with current. When switching-off the transistor, the output voltage of the PFC coil will be limited to the initial output voltage level at the PFC capacitor via the PFC diode.

2. When the voltage is high enough, the voltage reduced by the winding ratio $N1/N2$ via the auxiliary winding at the PFC coils activates the semi-controlled rectifier, in order to limit the losses at the current limiter.

3. In case of a short-circuit at the PFC output, the PFC diode clamps the voltage at the PFC coil down to zero and disables the semi-controlled rectifier. The current limiter reduces the short circuit current.

PFC Solution with Tyco's PFC-IPM

This intelligent power module (IPM) is a complete, universally applicable PFC solution for currents up to 1 kW. The PFC-IPM is designed to reduce the input current upper waves and has the required features to realize a performance factor > 0.99. The switch is based on a boost topology, provided with a semi-controlled input rectifier (Figure 10).

This solution has an input start switch to limit the input current and a short-circuit protection for consumers connected

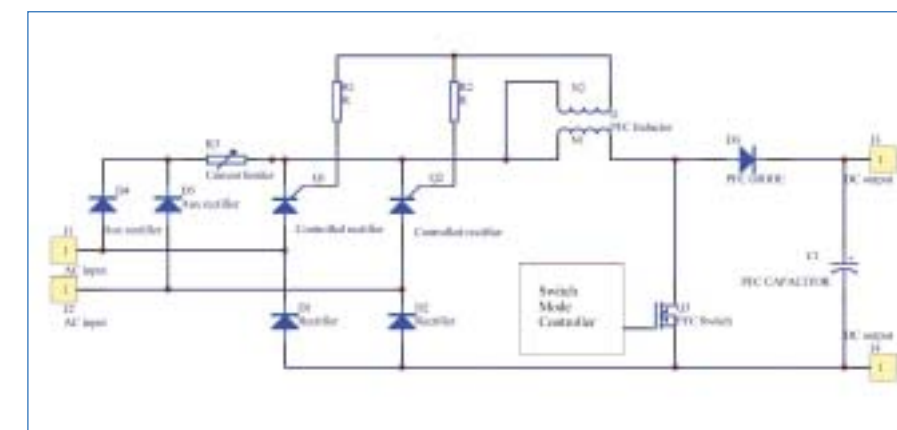


Figure 9. Switching System.

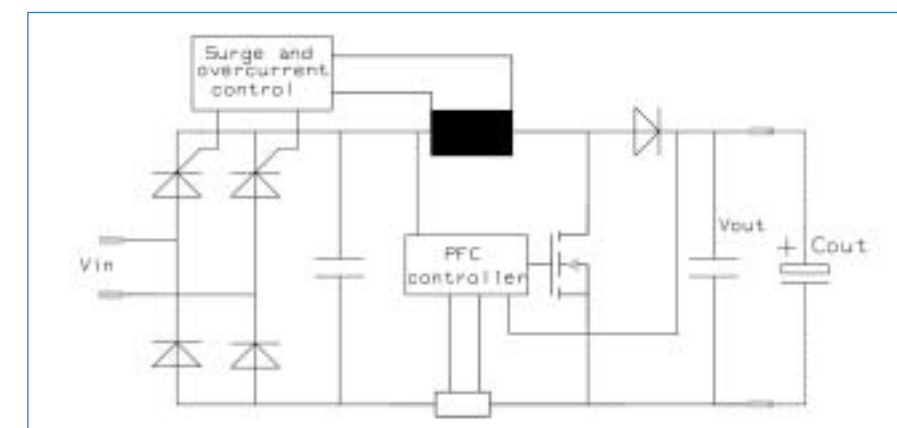


Figure 10. IPM PFC solution.

to the output. Another characteristic feature is the zero load capability. This means that the PFC-IPM can generate a stable DC output voltage without the necessity that a consumer must be connected to the output—a demanded must, when the application requires a highly stable output voltage (Figure 11).

The following characteristic features have been realized in this flexible, universally applicable PFC solution:

- Nominal input voltage 230 V_{AC}
- Output voltage 400 V_{DC}
- Output current (zero load) 0.1 kW
- Efficiency ca. 95% (including the Choke)
- Power factor > 0.99
- Starting current limiter < 12A
- Short-circuit protection for static and dynamic failures at the output

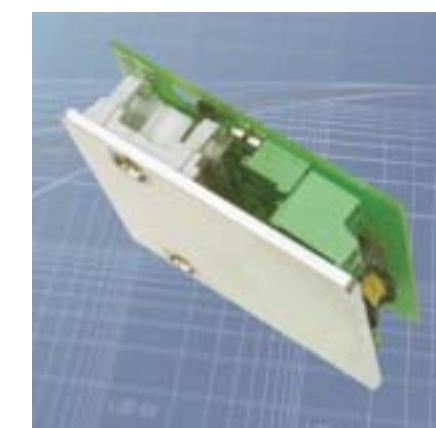


Figure 11. IPM Device Picture.

PFC Solution with Tyco's flowPFC 0

The following characteristic features have been realized in this flexible, power integrated concept:

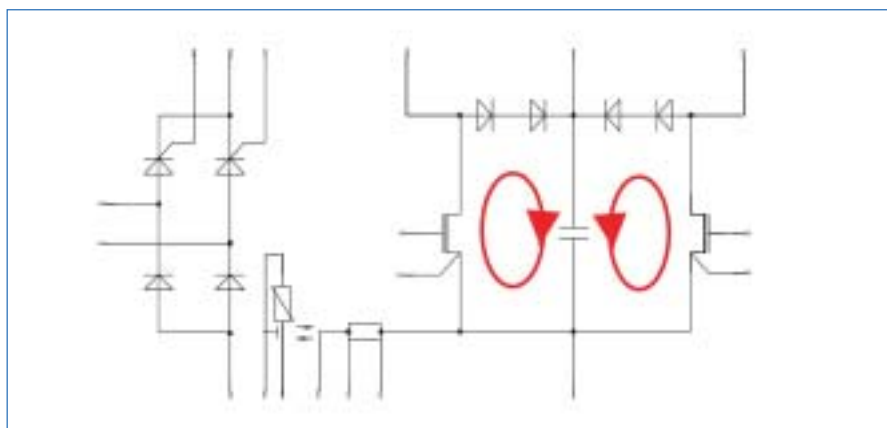


Figure 12. Flow PFC solution.

Features:

- All semiconductors integrated in one module, no additional efforts for thermal contacting required
- Integration of a temperature sensor for detection of the substrate temperature
- The proven flow concept allows a compact PCB design. Plugs with similar voltage are concentrated to voltage islands
- Symmetric design of the PFC transistor for parallel or alternating operation
- Low-inductive current measurement with a shunt for precise control of the PFC switch
- Capacitor for low-inductive bypassing of the high frequency in the module

PFC-Solution with Tyco's flowPIM+P

Drive solutions with PFC require the additional integration of one fast switching transistor and boost diode.

Similar to the standard TYCO flowPIM modules, all power semiconductors are integrated in one module, so that no additional action for the handling of the power dissipation to the heat sink is needed.

Features:

- 1 Phase Input Rectifier
- PFC Transistor + extreme fast Diode
- 3 Phase Inverter IGBT + FRED
- HF-Capacitor in DC Link
- Current sense shunt in the DC-
- Current sense shunt for PFC controlling in the DC-

- NTC temperature sensor
- Approved flow concept for easy routing off the system PCB
- Clip In for mechanical fixing into the PCB

Advantages of PFC solutions with tyco Modules

The Tyco PFC modules offer compact modules and the flow concept offer opportunity to get a compact and easy PCB design. All Tyco PFC solutions short the high frequency with a ceramic capacitor inside the module. The excellent EMC behavior is only possible with module solution and can never achieved with discrete components. The Clip In housing of the modules flowPFC0 and flowPIM0 is adjustable to different PCB and makes the assembly easy and reliable. The integrated temperature sensor protects the module and the application. The UL listing of the module shortens the time to get the application certified. These advantages are a basis for an innovative and cost effective PFC solution.

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Figure 13. Flow Device Picture.

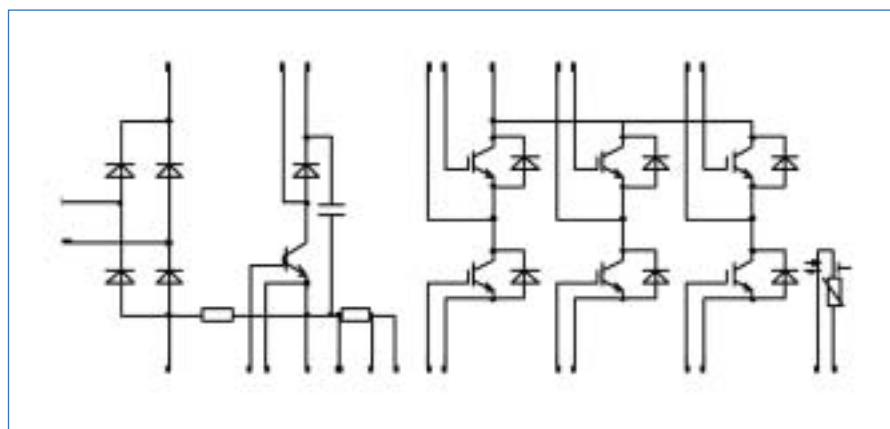


Figure 14. TYCO flowPIM modules.

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The driver is equipped with the award-winning CONCEPT SCALE driver chipset, consisting of the gate driver ASIC IGD001 and the logic-to-driver interface ASIC LDI001.

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- Direct or half-bridge mode
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- Isolated status feedback
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- Schmitt-trigger inputs
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- Duty cycle 0...100%
- Delay time typ. 325ns



Driver stage for a gate current up to $\pm 15A$ per channel, stabilized by large ceramic capacitors

Specially designed transformers for creepage distances of 21mm between inputs and outputs or between the two channels. Insulating materials to UL V-0. Partial discharge test according IEC270.

Isolated DC/DC power supply with 3W per channel

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CT-Concept Technologie Ltd. is the technology leader in the domain of intelligent driver components for MOS-gated power semiconductor devices and can look back on more than 15 years of experience.

Key product families include plug-and-play drivers and universal driver cores for medium- and high-voltage IGBTs, application-specific driver boards and integrated driver circuits (ASICs).

By providing leading-edge solutions and expert professional services, CONCEPT is an essential partner to companies that design systems for power conversion and motion. From custom-specific integrated circuit expertise to the design of megawatt-converters, CONCEPT provides solutions to the toughest challenges confronting engineers who are pushing power to the limits.

As an ideas factory, we set new standards with respect to gate driving powers up to 15W per channel, short transit times of less than 100ns, plug-and-play functionality and unmatched field-proven reliability. In recent years we have developed a series of customized products which are unbeatable in terms of today's technological feasibility.

Our success is based on years of experience, our outstanding know-how as well as the will and motivation of our employees to attain optimum levels of performance and quality. For genuine innovations, CONCEPT has won numerous technology competitions and awards, e.g. the "Swiss Technology Award" for exceptional achievements in the sector of research and technology, and the special prize from ABB Switzerland for the best project in power electronics. This underscores the company's leadership in the sector of power electronics.

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2504 Biel-Bienne
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Influence of MOSFET Transconductance

Linear and switch mode applications are the focus

HT MOSFET devices offer faster switching slew rate performance and reduced conduction losses relative to MT, desirable for SMPS power supply design and SMPS motor control, but not beneficial for linear mode regulators.

Alain Laprade and Alex Craig, Fairchild Semiconductors

Differences in MOSFET cell structures and technologies provide the power electronics design community many options as to the selection of an appropriate device for a given application. Medium transconductance (MT) MOSFETs may be appropriate for some applications requiring extended periods of linear operation, whereas high transconductance (HT) MOSFETs may be the best device for other applications. However, failure to consider differences in gate charge and thermal impedance may result in different operation.

Differences between Medium and High Transconductance Power MOSFETs

HT MOSFET technology has a higher channel density than MT MOSFETs. Structural geometric differences (Figures 1 and 2) depict a significantly reduced die specific on-resistance (R_{sp}) for the HT structure, rendering these devices superior to the MT structure of Figure 1 for switch mode operation. Circuit design challenges originate from failing to consider the effect from HT technology's higher gate charge per unit area, higher transconductance, faster switching slew rate, increased thermal impedance from the use of a smaller die, reduction of

device safe operating area (SOA), and lower unclamped inductive switching (UIS) capability. These differences are discussed in this article.

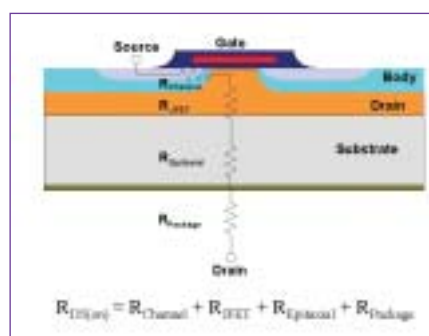


Figure 1. Medium transconductance MOSFET using planar technology.

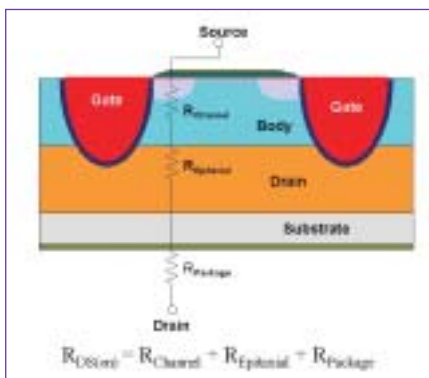


Figure 2. High Transconductance MOSFET using trench technology.

Issues guiding the selection of MOSFET technology can be roughly broken down into three application categories:

- high frequency switched mode power supplies
- switch mode motor control
- linear mode regulation

High Frequency Pulse Width Modulation (PWM) Power Supply

HT devices are best suited to achieve system efficiency improvement. To achieve best operating performance, the gate drive circuitry may be optimized when substituting an MT device. A figure-of-merit (FOM) frequently referenced for device comparison is: $r_{DS(on)}(T_J)_{HT} \times Q_{G_HT} \leq r_{DS(on)}(T_J)_{MT} \times Q_{G_MT}$ as gate charge becomes an important loss contributor at high switching frequencies.

PWM Motor Control

Both MT and HT MOSFET devices are appropriate technologies. Equivalent or lower loss performance is possible with smaller die size HT MOSFETs. It may be incorrect to simply use the same $r_{DS(on)}$ HT device when substituting a MT device. An $r_{DS(on)}$ reduction may be necessary to maintain equivalent performance. An approximation for determining HT $r_{DS(on)}$ requirement is to use a power-density-equivalency

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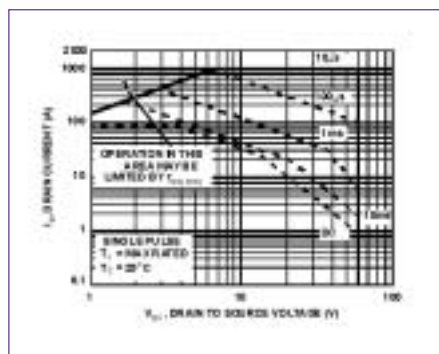


Figure 3. Forward bias SOA curve.

where: $r_{DS(ON)}(T_J)_{HT} \times R_{\theta JC_HT} \leq r_{DS(ON)}(T_J)_{MT} \times R_{\theta JC_MT}$

Differences in gate charge characteristics are typically not a significant consideration as motor drive MOSFET operating frequencies rarely exceed 20 KHz. The gate drive circuit may require optimization when replacing MT devices with HT for similar EMI system performance with controlled switching slew rate. Snubbers are useful for this purpose.

Use of parallel HT devices in applications meant to have slow slew rate switching transitions may be more difficult. The consequence of mismatched threshold voltage ($V_{GS(th)}$) between devices must be carefully considered to avoid inter-device gate oscillation. Under some circumstances, oscillation can occur in spite of the use of individual gate decoupling resistors. Layout modification should also be considered particularly if one is replacing a number of MT devices with a lesser number of HT devices.

Linear Mode Regulation

It is incorrect to attempt die size reduction for linear mode regulation by using HT devices as an alternative to MT devices. Die volume (Z_{JC}) is the only factor of consequence when performing junction temperature calculations. There are no operational benefits from the use of HT technology.

It is not possible to generalize the effect of MT and HT MOSFET technologies on device performance. Die size, packaging technology, layout parasitics,

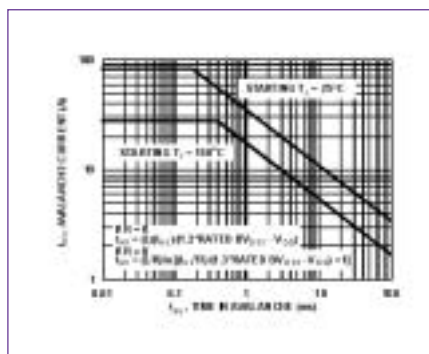


Figure 4. Unclamped inductive switching capability.

temperature dependent transconductance and gate threshold voltage characteristics, and SOA operating point influence performance. Power applications with die sizes requiring larger packages (e.g. TO220, TO263) are subject to uneven die surface temperature distribution, and some current focusing may result. The negative temperature coefficient of the voltage transfer characteristic accentuates the extremes in die surface temperature, resulting in increased current density focused at the die thermal center. HT devices are more susceptible to this than are MT devices. MT technology may be the more appropriate technology in applications having high linear mode power dissipation.

HT MOSFETs are optimized for high frequency operation. A consequence of optimizing MOSFET die designs for high frequency operation is that device transconductance is greater than that of MT devices, rendering them more sensitive to electrical noise and susceptible to high frequency oscillation with circuit parasitics. For same die size devices, HT device SOA is less than that of MT. It is possible to design a device using trench technology optimized for linear mode operation with increased R_{sp} as a trade-off. At the time of this writing, such devices are commercially unavailable.

Other Issues

Unclamped inductive switching (UIS) performance of HT technology is less than that of MT for same die size devices. As HT devices offer reduced $r_{DS(ON)}$ at a reduced die size, use of such devices are often made and occasional-

ly encounter problems when testing outside normal operation. While UIS energy capability depends on die size in a given application, the temperature at which the device fails is a function of the epi doping. The energy required to reach that temperature is a function of time spent in avalanche (t_{AV}) and avalanche current (I_{AS}); Avalanche energy $E_{AS} = \frac{1}{2} \times 1.3 \times BV_{DSS} \times I_{AS} \times t_{AV}$.

MOSFET SOA capability is die size and the channel density dependent. Failure temperature is also a function of epi doping. Depending on the SOA event, the current, voltage, and time required to reach failure point in HT devices may be less than that required for a same size MT device.

Circuit designers are often unaware of the device die sizes, so careful consideration must be given to avoid device failures. MOSFET manufacturers must assist the circuit designer to avoid such failures. To this end, Fairchild Semiconductor provides SOA (Figure 3) and UIS rating graphs (Figure 4). The criteria for safe usage are to find the circuit's peak load current and t_{AV} , and to plot the information on the UIS graph in the data sheet example shown in Figure 4. If the operating point is below and to the left of the appropriate $T_J(START)$ line, the part is being used within its capability. Also provided is a simple transient thermal impedance model which may be used to obtain a reasonable junction temperature approximation during transient events.

HT MOSFET devices offer faster switching slew rate performance and reduced conduction losses relative to MT, desirable for SMPS power supply design and SMPS motor control, but not beneficial for linear mode regulators. HT device selection as a replacement for an MT device in PWM designs should be performed using a power-density-equivalency or figure-of-merit. Not to be forgotten is the potential effect of UIS in a circuit using HT technology.

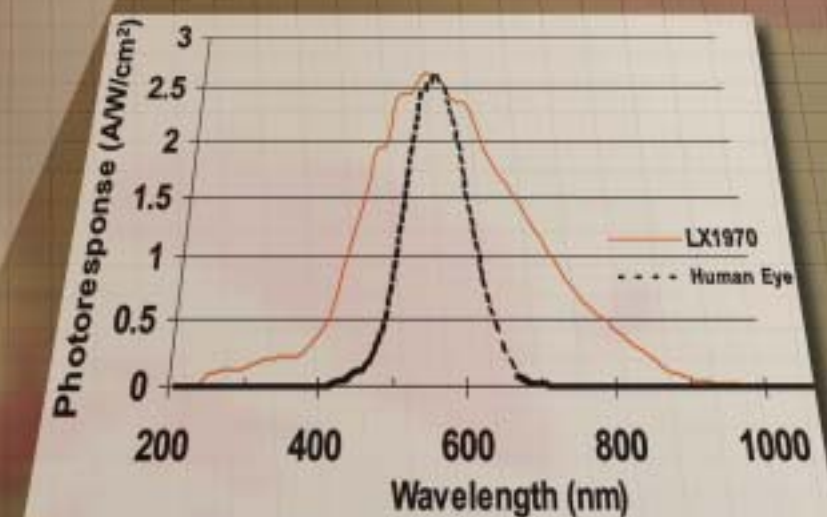
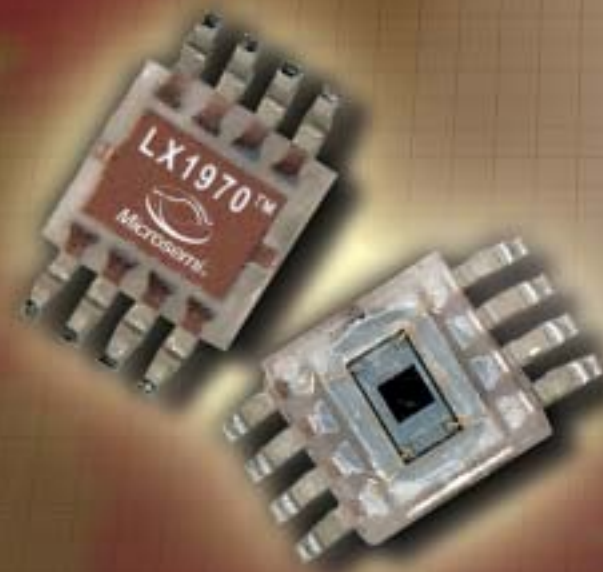
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Lossy Models Offer More Realistic Averaged Simulations

Including the true diode SPICE model

Standard averaged models do not include the various losses that degrade the converter efficiency but also it's small-signal AC response.

Christophe Basso, ON Semiconductor

When one derives the equations related to a given topology operation (e.g. BUCK, BOOST etc.), perfect or ideal elements are usually installed on the schematic and various drops are omitted in the calculations. If this option obviously simplifies the analysis, it perceptibly alters the DC operating point as well as the AC response. Figure 1a and 1b depicts a BUCK converter that includes losses attributed to a) the inductor wire resistance, R_{lf} b) the power switch $R_{DS(ON)}$, R_{on} c) the diode forward drop, V_f and its dynamic resistance

$$R_d = \frac{dV_f}{dI_d} @ I_d :$$

When the switch closes, the inductor voltage V_L and capacitor current I_c can be defined through the following equations:

$$V_{LON} = (V_{in} - V_{out}) - I \cdot (R_{on} + R_{lf}) \quad , \text{eq. 1}$$

$$I_{CON} = I - \frac{V_{out}}{R_{load}} \quad , \text{eq. 2}$$

At the switch opening, the current I keeps circulating in the same direction, but now flows through the free-wheel diode to keep the amp-turns constant in the inductor. Equations become:

$$V_{LOFF} = -I \cdot (R_d + R_{lf}) - V_{out} - V_f \quad , \text{eq. 3}$$

$$I_{COFF} = I - \frac{V_{out}}{R_{load}} \quad , \text{eq. 4}$$

Theory dictates that the average voltage $\langle V_L \rangle$ across the inductor must be null when the converter has reached the equilibrium: $\langle V_L \rangle = D \cdot V_{LON} + D' \cdot V_{LOFF} = 0$, which by combining eq. 1 and eq. 3 gives:

$$\left[(V_{in} - V_{out}) - I \cdot (R_{on} + R_{lf}) \right] \cdot D + \left[-I \cdot (R_d + R_{lf}) - V_{out} - V_f \right] \cdot D' = 0 \quad , \text{eq. 5}$$

The above statement regarding the inductor average voltage also translates to a capacitor where its average current $\langle I_c \rangle$ shall be null when the converter operates in steady-state: $\langle I_c \rangle = D \cdot I_{CON} + D' \cdot I_{COFF} = 0$, which by combining eq. 1 and eq. 3 gives:

$$\left[I - \frac{V_{out}}{R_{load}} \right] \cdot D + \left[I - \frac{V_{out}}{R_{load}} \right] \cdot D' = 0 \quad , \text{eq. 6}$$

By solving eq. 6 and plugging I into eq. 5, we obtain the complete transfer function of the BUCK affected by static losses:

$$\frac{V_{out}}{V_{in}} = D \cdot \left[\frac{1}{1 + \frac{R_{on}}{R_{load}} \cdot D + \frac{R_{lf}}{R_{load}} + \frac{R_d}{R_{load}} \cdot D' - \frac{V_f}{V_{out}} \cdot D'} \right]$$

, eq. 7

Equation 7 shows that losses are weighted accordingly to the time sequence in which they play: R_{lf} is present during both T_{on} and T_{off} whereas R_{on} and R_d are respectively active during T_{on} (D multiplication) and T_{off} only ($[1-D]$ multiplication).

In previous averaged models, the state-space averaging technique or switch waveforms analysis were usually applied over perfect elements, non-inclusive of the above ohmic losses. However, if these elements play an active role in the DC transfer function, they affect the small-signal AC analysis quite significantly by introducing various damping effects. In a paper presented in

PCIM Nuremberg 2001, Sam Ben-Yaakov from the Ben-Gurion University (Beer-Sheva, Israel) presented his modified Generalized Switched Inductor Model (GSIM) where all conduction losses were modeled [1]. Without entering into the details of the model derivation, Ben-Yaakov did not depart from his original model but added in series with the inductor the losses specific to a given time interval (e.g. V_f and R_d during D' in a BUCK, etc.). One very interesting feature consisted in including the true diode SPICE model and the real MOSFET $R_{DS(ON)} @ V_{gs}$ if necessary. Figure 2a shows how to implement this model in a BOOST voltage-mode application (see Figure 2a and 2b).

The internal R_{on} was passed as a standard resistor parameter to keep the simplest implementation. The diode model is however kept external. A DC sweep was performed on the schematic where V_{Don} was swept up to 900mV (90% duty-cycle). Figure 2b reveals the results showing the latch-up characteristic of the BOOST when the ohmic losses become more significant compared to the load. The above model subcircuit netlist can be downloaded in both IsSpice4 and PSpice from the author website [2]. Other models include lossy BUCK in voltage and current-mode

control. Please note that more complex models including dynamic switching losses were derived by the Colorado Power Electronics Center (CoPEC). An extensive documentation related to the subject, including tutorials, is available from the university web site, <http://ece-www.colorado.edu/~pwrelect>.

Christophe BASSO
ON Semiconductor
14, rue Paul Mesplé - BP1112 - 31035
TOULOUSE Cedex 1 - France
33 (0)5 34 61 11 54 e-mail:
christophe.basso@onsemi.com

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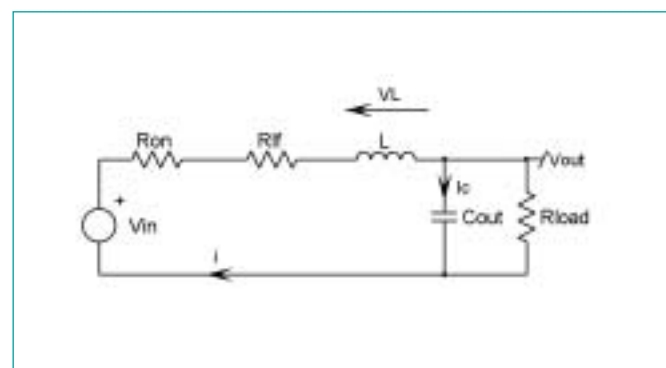


Figure 1a. Component arrangement during the ON time.

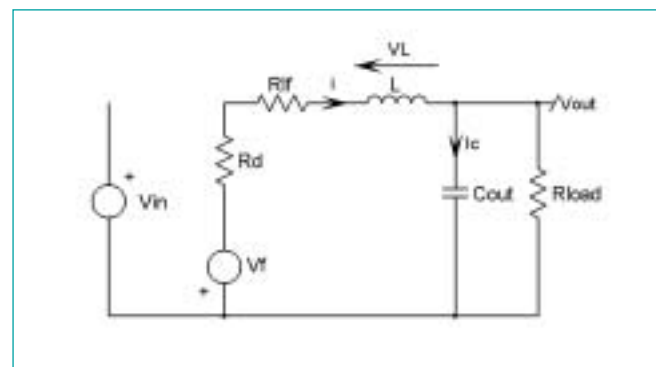


Figure 1b. Component arrangement to the switch turn-off.

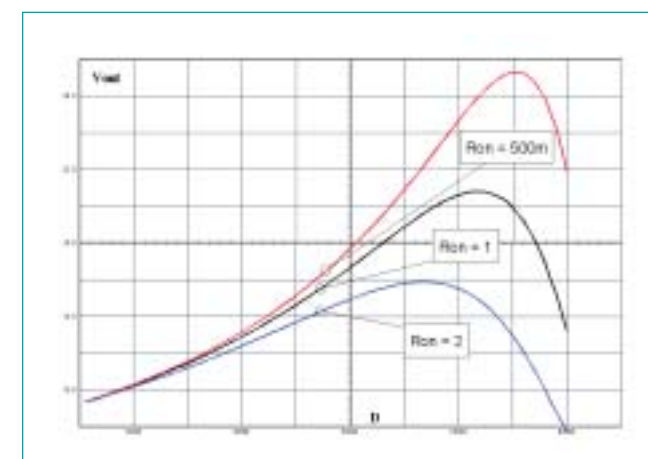


Figure 2a. The BOOST model features a true diode SPICE model.

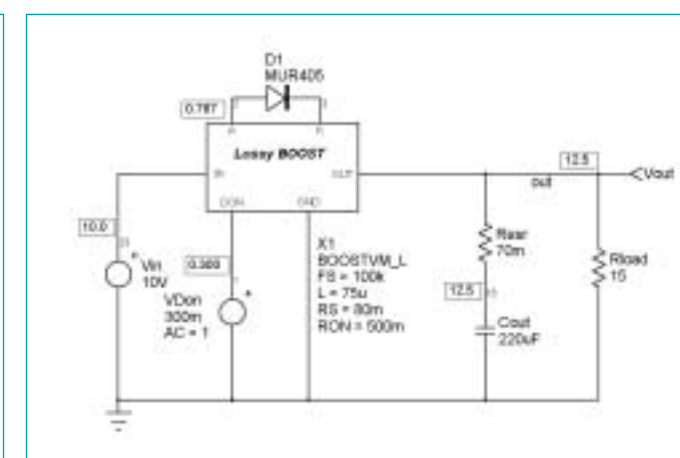


Figure 2b. V_{out} versus D exhibit the classical BOOST latch-up effect.

More Power for the Rails

Concentration on capacitor energy storage systems

Ultracapacitor energy storage systems help mass transit systems avoid sudden power outages, and as a pleasant side effect, they yield energy savings of up to 30 percent.

By Dr. A. Schneuwly, J. Auer, G. Sartorelli, Maxwell Technologies

If you frequently travel from place to place via tram or the underground, you are familiar with the problem of power outages. Travel suddenly comes to a stop, delays occur, and within a few minutes there may be several trains stuck one behind the other somewhere between stations—typically at peak hours, when all of the coaches are full. For individual passengers, this initially only causes a few minutes' unpleasant delay, but in a sort of chain reaction, such an incident can affect large portions of the rail network, particularly if several trains must resume their journeys after being backed up in a tunnel. If they all draw energy from the same network at practically the same time, they can pull the network voltage below a critical level.

The local transport authorities of several European cities such as Cologne and Madrid, as well as several metropolises in the US such as Portland, Oregon, are now tackling this previously unsolved problem with an innovative energy storage system that is also designed to recover braking energy. This system is called SITRAS SES, and it was developed by the engineers of Siemens Transportation Systems. It allows system operators to achieve energy savings of up to thirty percent. SITRAS SES also makes a decisive contribution to stabilising the network, which not only enhances the reliability of mass transit systems, but also improves the tempers of passengers.



Figure 1. A SITRAS SES unit can absorb the braking energy released by all stopping trains within a radius of up to three kilometres.

Underground trains that feed braking energy back into the electricity supply system first entered regular service around twenty years ago. When such a train brakes, its electric motor acts as a generator and feeds the regenerated energy back into the supply lines. However, this excess energy can only be used if there is an increased energy demand somewhere else in the network, which can for instance arise from a train just starting off. Otherwise, only approximately sixty percent of the regenerated energy can be used in normal operation. The remainder is dissipated as heat in the braking resistors of the vehicles, without being put to good use. Since energy costs form a significant portion of operating budgets, amounting to 25,000 to 150,000 euros per year depending on

the vehicle type, system operators have a major interest in reducing their costs by achieving energy savings.

Around four years ago, the engineers first started thinking about an energy storage system that could absorb braking energy and release it later on to trains that are starting to move. Simulations and practical tests in various cities showed that using a suitable energy storage system operationally for around 22 hours per day could reduce the annual primary energy demand by as much as 500,000 kilowatt-hours or 30 percent. That corresponds to a reduction of CO₂ emission of 300 tons.

Before choosing ultracapacitors as energy storage source the engineers first decided to use flywheel storage systems. But already after the first extended service tests, it was clear that they were not suitable for long-term use, due to their complex maintenance. That's why the engineers then concentrated on developing capacitor energy storage systems.

The Maxwell ultracapacitors used in the SITRAS SES system have a capacitance of 2600 farads with a size of a small soda can. Each device is operated at a voltage of 2.3 volts. The complete energy storage unit contains approximately 1300 of these 2.3-volt units. The system provides a peak power capacity of one megawatt.

Figure 2a and b. A glimpse into the heart of the SITRAS SES system: The 2600 farad BOOSTCAPs can be easily recognised.

The system, which includes a connection unit, a voltage converter and control electronics in addition to the capacitors, is housed in two rows of cabinets, each of which is 3 metres long and 2.7 metres high. If one or more trains start at the same time, the SITRAS SES system releases the energy absorbed during braking, and the network voltage never drops below the critical level. The system thus not only saves energy, with its fast response time it also prevents a sudden loss of power for the trains and thus avoids leaving hundreds of frustrated passengers sitting stranded.

Ultracapacitor technology

In Maxwell ultracapacitors, carbon powder electrodes are combined with an organic electrolyte. By using extremely large surface area carbon electrodes, such capacitors can contain an active surface area corresponding to two football pitches in a volume of half a litre. Compact in size, ultracapacitors can store an incomparably higher amount of energy than conventional capacitors. Indeed, ultracapacitors from Maxwell offered under the trademark BOOSTCAP are currently available on the market with capacitance ranges from prismatic 5 and 10-farad cells up to cylindrical 2600 Farads. They can repeatedly provide very high power pulses, recharge as fast as they are discharged, while little affect on the life of the product. Because they are capable of cycling millions of times, they are virtually maintenance-free over the life of any product in which they are used. As a result, they need not be disposed—making them a very "green" form of energy storage.

Maxwell is able to supply BOOSTCAPs in volumes and at price points that are opening numerous market opportunities for energy storage and peak power delivery. To facilitate adoption of ultracapacitors for applications which require integrated packs consisting of multiple ultracapacitor cells, Maxwell provides fully integrated power packs that satisfy

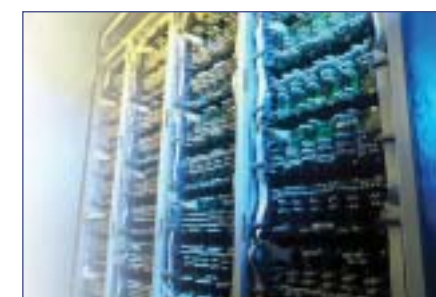


Figure 2a.



Figure 2b.



Figure 3a.

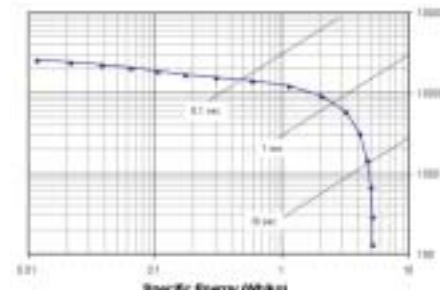


Figure 3b.

the energy storage and power delivery demands of large systems.

Our large cell ultracapacitors have been designed into industrial applications such as uninterruptible back up power systems, pitch systems of wind turbines and transportation applications such as hybrid buses and trucks, electrical rail systems and capacitive starting systems for diesel engines. Our small cell ultracapacitors have been designed into consumer electronics such as remote transmitting devices, digital cameras, bar code scanners, computer memory boards and transportation applications such as electrical rail alarm systems and electric actuators, or latches, for aircraft and automobile doors. Many of the end products into which BOOSTCAPs have been designed now are ramping into commercial production.

Product news

Maxwell recently developed a new high power ultracapacitor that features a revolutionary case design. The BCAP0350 D cell BOOSTCAP is the first in a series of new ultracapacitors to be standardized on battery-sizing to drive down the costs and ease the integration of the technology. By standardizing its ultracapacitors, Maxwell is reducing its manufacturing costs by more than 50 percent and passing that savings

directly to OEMs, as well as reducing time-to-market by providing engineers a known form factor for seamless, rapid product integration.

Figure 3a and b. New high power BCAP0350 D cell BOOSTCAP and its Ragone plot showing the specific power density against the specific energy density.

The 350-farad ultracapacitor is designed for maximum power throughput. Weighing only 60 g, it features a power density of up to 25 kW/kg and energy density of 5.1 Wh/kg. The new BOOSTCAP is designed for a rated voltage of 2.5 V and can withstand a peak of 2.8 V. The operating temperature range extends from -40 to 70 °C. Thanks to the outstanding performance as well as the low cost design this cell is ideally suited for application such as automotive multiple zone electrical distribution systems, wind turbine pitch systems, aircraft door opening systems, actuator applications, medical systems, battery support applications in general and many high volume consumer applications.

Authors:

Dr. A. Schneuwly, J. Auer, G. Sartorelli, Maxwell Technologies SA, 1728 Rossens, Switzerland

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Digital Power Control Highlights

Digital controller requires fewer components

Digital controllers offer many advantages over their analog counterparts: improved system reliability, flexibility, and ease of integration and optimization. The use of software to change the controller functionality makes a system based on a digital controller very flexible.

Zaki Moussaoui and Greg Miller, Intersil

Power requirements for high-performance microprocessors have become increasingly demanding (see Figure 1). Prior to the Pentium class of processors, 5 Volts directly from the AC-DC silver box was used as the processor core voltage. As core voltages dropped and current demands increased, the industry moved to using 12V from the silver box as the input voltage to a synchronous Buck converter to generate Vcore. In an attempt to decrease the high ripple associated with regulating Vcore from 12V, the use of a multiphase buck converter became the standard starting with Pentium 4 class processors. In order to satisfy processor power specifications, such as soft start, power sequencing, VID and load line specifications, dedicated multiphase controller ICs like the HIP6301 from Intersil were introduced. The ICs were conceived based on analog PWM technology.

In addition to voltage and current control, the new multiphase controllers were required to satisfy many other specification requirements: VID programming, load line regulation, power sequencing, phase current balance, and monitoring and protection. The PWM function in the multiphase controller is becoming a

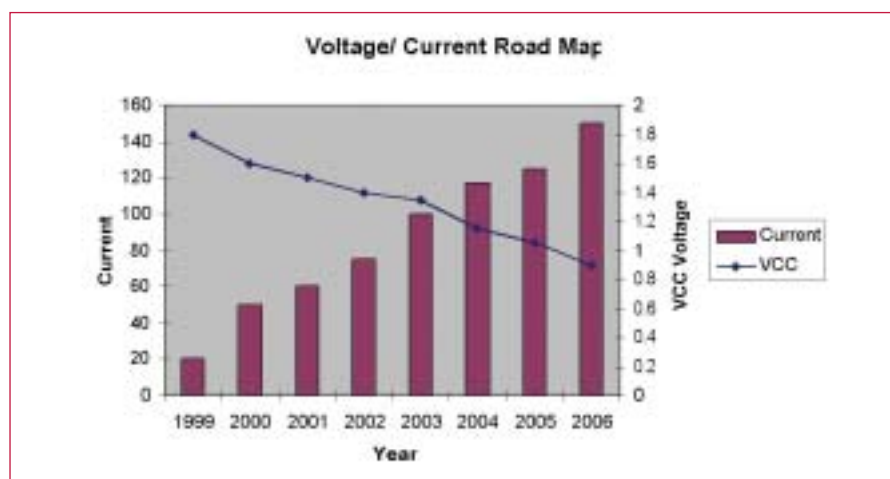


Figure 1. Voltage/ Current Road Map.

small part of the controller functionality. This demand for more functionality from the controller and the continuing advance of digital technology has pushed many companies to look at digital multiphase control. The proposed solutions vary from the use of digital processors (DSP), microprocessors, and microcontrollers, to the latest software-programmable mixed-signal IC, the ISL6590 introduced by Intersil.

Benefits of Digital Control

Digital controllers offer many advantages over their analog counterparts: improved system reliability, flexibility, and ease of integration and optimization. Overall, they offer an elegant solution to many requirements in the Vcore power regulation specifications.

A system based on a digital controller requires fewer components, which decreases the mean time before failure (MTBF) of the system. For example, all

the components for the feedback loop are eliminated; the select on test and select according to design specification components are also replaced by software programming. A change to the design to meet a new requirement may not require new board layout and more engineering time; the changes could be implemented in software.

The added capability of monitoring protection and prevention will also increase the system reliability. For instance, an engineer can choose to monitor the system temperature to decrease the current limit level, or turn on a fan. This scenario will decrease the stress on the power components and fans that in turn will improve the system reliability and would eliminate over specification of components.

The use of software to change the controller functionality makes a system based on a digital controller very flexible. The digital controller offers the ability to add, eliminate or change any system parameter in order to meet new requirements, or to optimize and calibrate the system. For example, the same voltage regulator model (VRM) can be programmed to meet different processor specifications such as Load Line (LL), voltage identification (VID), and current or voltage requirements, without any hardware changes. Due to the ease of integrating communication capability, the digital controller also facilitates the ability to integrate and cascade multiple systems together. For example, in multi-VRM boards, current sharing could be implemented through a standard communication bus without the need for any hardware additions.

Digital Control IC Implementation

In order to choose the ideal digital controller IC for the application, the power supply engineer will have take into consideration the performance and the capabilities of many digital IC blocks that normally do not exist in an analog controller IC. Three blocks in particular form the heart of a digital controller: an anti-aliasing filter, an analog to digital converter (ADC), and a digital pulse

width modulator (DPWM). See Figure 2.

a) Anti-Aliasing Filter

The Sampling Theorem indicates that a continuous signal can be properly sampled, only if it does not contain frequency components above one-half of the sampling rate. So, if the sampling rate is 2MHz, then an anti-aliasing filter with -20dB gain at 1MHz would be practically expected. The importance of the anti-aliasing filter arises from its effect on the total system bandwidth. For example, assume that we only can have an RC type of low pass filter, with transfer function of the form:

$$H_{Alias}(s) = \frac{DC_{gain}}{s + DC_{gain}}$$

To have -20dB gain at 1MHz, half the sampling frequency of 2MHz, the pole of H_{Alias} has to be at 100kHz, which will introduce a phase lag of 45° at 100kHz. If a power stage is switching at 1MHz, an analog control loop with a crossover frequency of 200kHz can easily be obtained. With this digital implementation, the crossover frequency will be limited to below 100kHz if we do not allow any phase lag to be introduced in the feedback loop by the anti-aliasing filter. To solve this problem we could use an active filter with more poles, or increase the sampling frequency.

b) A/D Converter

The A/D Converter block consists of two main sub-circuits: the sample and hold and the ADC itself. The sample and hold block adds a delay in the loop according to $e^{-sT_{SH}}$ that can be approximated as:

$$H_{SH} = \frac{1}{1 + sT_{SH}}$$



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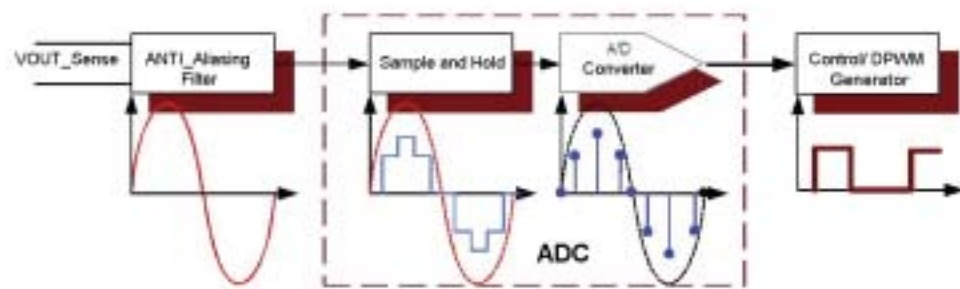


Figure 2. Major Digital Controller Blocks.

where T_{ADC} is the A/D Converter sampling period.

In order to decrease the delay, i.e. decrease the phase lag, the sampling period T_{ADC} of the A/D Converter needs to be increased.

A wide choice of ADC architectures exist that differs in resolution, bandwidth, accuracy, and power requirements. The major ADC architectures are flash (all decisions made simultaneously), successive approximation (where a successive approximation shift register is the key defining element), and pipelined with multiple flash stages. Each has its own unique set of pros and cons.

The Flash Architecture: Sets of 2^n-1 comparators are used to directly measure an analog signal to a resolution of n bits. The flash architecture has the advantage of being very fast because the conversion occurs in a single cycle. The disadvantage is that it requires a large number of comparators; the number of comparators needed for an n -bit ADC is equal to 2^n-1 . For instance, a 10-bit A/D converter needs 1023 comparators, which makes it hardware intensive even for an integrated controller.

The Successive Approximations Architecture: This approach uses a single comparator over many cycles to make its conversion. The successive approximation (SAR) converter only needs a single comparator to realize a high resolution ADC, but it requires n comparison cycles to achieve n -bit resolution.

SAR has a major disadvantage since it takes too many cycles to convert the analog signal, which will introduce a large phase lag in the feedback loop. For example, a 10-bit conversion will introduce $10T_{ADC}$ delay.

The Pipelined architecture with Multiple Flash: This is the middle ground between the fast flash converter and the high resolution SAR. A pipelined converter divides the conversion task into p consecutive stages. Each of these stages consists of a sample and hold circuit, an n -bit flash converter, and an n -bit D/A converter (DAC). A pipelined converter with p -pipelined stages, each with an n -bit flash converter, can produce a high-speed ADC with a resolution of $k = p \times n$ bits using $p(2^n-1)$ comparators. For example, a 10-bit, two stage pipelined converter would require 62 comparators as compared to 1023 for the flash, and will take only two cycles for the conversion compared to $10T_{ADC}$ on a SAR.

From the discussion regarding the anti-aliasing filter and the delay introduced by the Pipelined or the SAR A/D converter, we see clearly the need for high sampling rate.

The number of bits needed can be based on the resolution of the measurement required. In order to satisfy a specified output voltage regulation ΔV_{out} , the ADC resolution has to have an error less than the allowed variation of the output voltage.

If the maximum output regulation is ΔV_{out} , the maximum voltage of the ADC is $\Delta V_{out\max}$ and the output voltage V_{out} is scaled by a gain G to meet the ADC voltage levels, then the least significant bit of the ADC has to be less than the product of the maximum ripple and the Gain.

$$\Delta V_{out} G \geq \frac{V_{ADC\max}}{2^k}$$

where k is ADC number of bits
Solving for k we get:

$$k_{ADC} = \text{int}(\log_2(\frac{V_{ADC\max}}{\Delta V_{out} G}))$$

For example, if the output voltage ripple ΔV_{out} is 5mV, the output is 2V, and the maximum ADC input voltage is 1V, a scaling of $G = 0.5$ will be required before the input to the ADC. At a minimum, an ADC with $k_{ADC} = 10$ bits is required in this case.

c) Digital Pulse Width Modulator

An analog controller has no inherent limit on the possible pulse width generated. On the other hand, a DPWM produces a discrete and finite set of PWM widths. From the output point of view in steady state, only a set of discrete output voltages is possible. Because DPWM is part of the feedback loop, it is necessary that the resolution of the DPWM be high enough so that the output will not display what is known as a limit cycle. In a limit cycle the output

goes into an oscillation of fixed amplitude and frequency, irrespective of the initial state.

The minimum number of bits needed so as not to display any limit cycle depends on the topology, the output voltage, and the ADC resolution. For example, in the buck converter:

$$V_{out} = DV_{in} \text{ where } D \text{ is the Duty Cycle.}$$

If we differentiate the above equation, we get:

$$\Delta V_{out} = V_{in} \Delta D$$

Replacing V_{in} by $\frac{V_{out}}{D}$, we get:

$$\Delta D = \frac{D \Delta V_{out}}{V_{out}}$$

Therefore, if we have k_{pwm} bits in our PWM modulator, the least significant bit is:

$$\Delta D = \frac{1}{2^{k_{pwm}}} = \frac{D \Delta V_{out}}{V_{out}}$$

From the preceding paragraph, the minimum output ripple is:

$$\Delta V_{out} = \frac{V_{ADC\max}}{2^k G}$$

Using the result from above we get:

$$k_{pwm} = \text{int}(k_{ADC} + \log_2(\frac{GV_{out}}{V_{ADC\max} D}))$$

Where k_{ADC} is the ADC number of bits.

As was shown in the previous example, if $\Delta V_{out} = 5\text{mV}$, the output is 2V, the maximum ADC input voltage is 1V, and a scaling of $G = 0.5$, then a minimum of 10 bit ADC is required. With $k_{ADC} = 10$ bits and assuming a minimum duty cycle of 0.1 ($D = .1$), a minimum of 14 bits is required for the Digital PWM.

Over the years, power supply designers have gained a strong knowledge of how to choose an analog power supply controller in order to meet the required specifications. With the introduction of digital controllers, the choices are not as clear. The digital controller requires the designer to pay attention to more complex IC blocks. In order to achieve the digital controller advantages of improved system reliability, flexibility, and ease of integration and optimization, the power supply designer must select the correct ICs for the application. The anti-aliasing filter, analog to digital converter (ADC), and the digital pulse width modulator (DPWM) are the heart of the digital controller IC. Special design considerations of these blocks are key to achieving superior overall system performance.

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Power Manager is Easy to Design and Program

Programmability reduces prototype-debugging time

Modern electronic systems have complex power requirements; the control and sequencing of the various voltage supplies that are incorporated into these complex systems is a major problem faced by today's design engineer.

By Johannes Fottner, Lattice Semiconductor

The Power Manager series from Lattice Semiconductor is capable of performing all power supply management functions for contemporary low voltage and multi voltage systems in a single chip. The Power Manager is a family of in-system-programmable components which facilitates setting up to 12 monitoring thresholds, setting precise delays, generating absolutely flexible monitoring and sequencing functions and outputting both logic signals as well as driving n-channel-MOSFETs. The programmable logic core also controls the output voltages of these MOSFETs. This article covers a typical supply voltage sequencing and monitoring application from a component design and programming view.

Being the first mixed signal PLD in the world the Power1208 provides the following programmable modules to implement the sequencing and monitoring functions:

- On-board ispMACH sequence controller CPLD
- Delay timers (for sequence delays and watchdog timers)
- Internal oscillator for precision timing and clocking the CPLD
- Multiple analog inputs with programmable precision analog threshold



- Buffered comparator outputs
- Programmable N-channel MOSFET drivers (Power1208 only)
- General-purpose open-drain digital logic outputs
- General-purpose logic inputs.

A typical application

Figure 1 shows a typical power control system, such as that which might be used on a PCB board with CPLDs and FPGAs requiring multiple supply voltages. In this circuit, the ispPAC-POWR1208 monitors the input supply (+5VIN), and controls the local supplies, as well as the interfaces to on-board logic through SYSRESET and SHUTDOWN signals. To power this system up, the 3.3V supply must be brought up first, the 2.5V supply next, and finally the 5V supply. The system should pause approximately 10msec between ramping

each supply in order to allow for stabilization of the circuitry on the board. Additionally, SYSRESET must be held LOW until all supplies have been activated. When all the supplies are activated, SYSRESET is brought high. When the SHUTDOWN line is brought HIGH, the power supplies must be turned off in the reverse order; 5V, 2.5V, and finally 3.3V.

Development Tool is PAC-Designer. The programmable functions, which make the ispPAC-POWR so flexible, are easily configured by use of a special software tool called PAC-Designer. The PAC-Designer, currently available as rev. 2.1, offers a hierarchical design entry system, which allows the user to define all analog and I/O characteristics through the use of Windows based graphical user interfaces in conjunction with dialog boxes.

For the design of the programmable logic core inside ispPAC-POWR a front end called LogiBuilder is used. It is a design environment that exists within PAC-Designer and provides a simple, easy-to-learn method for configuring the small embedded PLD incorporated within the ispPAC-POWR devices. The LogiBuilder shields the user from the

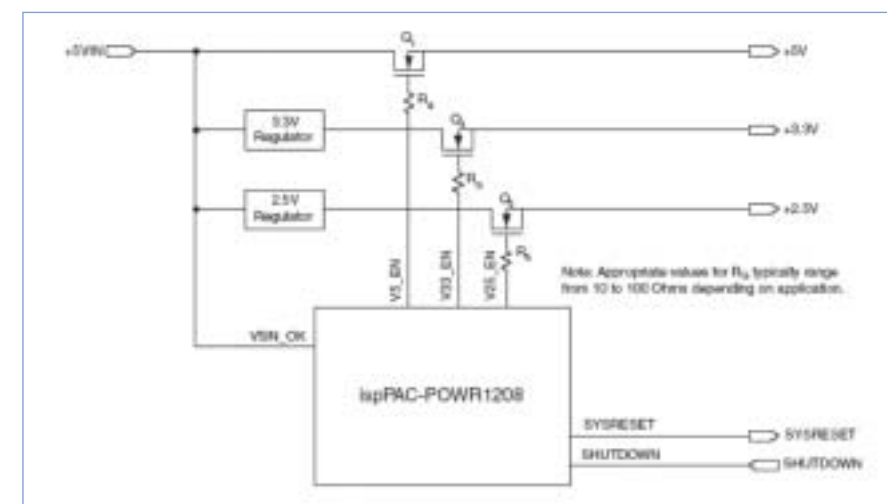


Figure 1. Power1208 controls power sequencing and generates supervisory signals.

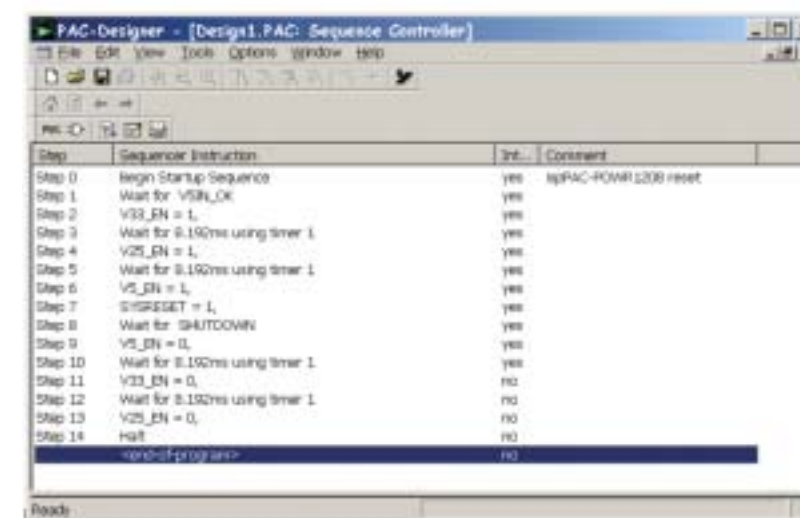


Figure 2. The first LogiBuilder example

complexity and details of the underlying PLD logic by presenting a higher-level architecture, which the design engineer uses to construct the required function.

For building sequence controllers, LogiBuilder provides an instruction set called LogiBuilder Sequence Controller (LBSC). Instead of worrying about product terms and macrocell configurations, the designer develops configurations as a program containing short sequences of LBSC instructions, which are sequentially executed. In addition, LBSC supports both looping and conditional execution through GOTO and IF-THEN-ELSE instructions. WAIT instructions are provided to support both waiting for specified events and user-defined

delays. In the ispPAC-POWR1208 a bank of four independent timers (TIMER1-TIMER4) is provided for implementing user-defined delays.

Looking at the application problem in figure 1 again, from a "programming" perspective the sequence can be paraphrased as follows:

1. Wait for +5V to rise
2. Activate 3.3V supply
3. Wait ~10msec
4. Activate 2.5V supply
5. Wait ~10msec
6. Activate Local +5V supply
7. Bring SYSRESET HIGH
8. Wait for SHUTDOWN
9. Turn off +5V supply
10. Wait ~10 msec

11. Turn off +2.5V supply
12. Wait ~10 msec
13. Turn off 3.3V supply
14. HALT

As can be seen from figure 2 the LogiBuilder vocabulary contains just these basic functions:

OUTPUT

```

WAIT FOR <Boolean Expression>
WAIT FOR <time> USING TIMER
<1,4>
IF <Boolean Expression>
THEN GOTO <step x>
ELSE GOTO <step y>
GOTO <step x>
NOP
HALT.

```

Because LogiBuilder is dialog-driven, as opposed to a free-form text language, it is easy to use, and does not require learning a large number of syntactic details, as the various dialogs guide the user in supplying the necessary information. Not only does it support sequences but also a capability called an exception. Exceptions provide the ability for a LogiBuilder program to quickly respond to conditions that are not specified in the main sequence. If we add over-voltage detection to the example cited above, the circuit must be modified to permit sensing of the output voltages.

As soon as an over-voltage condition is seen, the specified action will be to turn everything off fast and HALT. This can be accomplished without any changes to the sequence. Exceptions are listed in LogiBuilder in the exception table (Figure 3), which is usually displayed immediately beneath the sequence table. Each exception occupies one row in the exception table and allows branches to a step in the sequence window or to change outputs directly or both.

In addition to supporting the creation of user-defined control sequences, LogiBuilder also supports the implementation of simple logic circuits, both combinatorial and synchronous designs using 'D' flip-flops can be easily realized. To achieve this, the function of the respective output pin must be defined

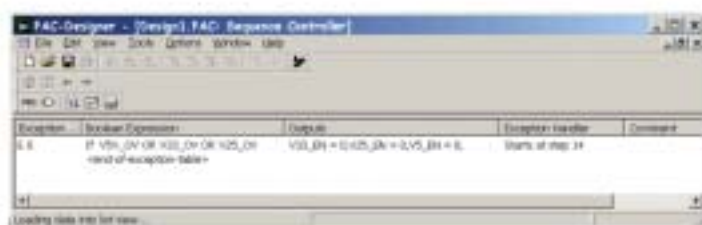


Figure 3. Exceptions allow reaction at any time.

as combinatorial or D-type flip-flop, and the equations entered in a window similar to the exception window.

During the design phase, LogiBuilder provides immediate feedback as soon as inconsistent or erroneous input is identified. Instead of waiting until the design has been entered to report errors LogiBuilder checks equations for inconsistencies and reports errors as soon as the individual equation is entered. During the compilation run LogiBuilder provides numerous post-design checks. Not only does this result in near-instantaneous feedback to the user of both real and potential problems with a design, but also by flagging these problems at an early point in the process LogiBuilder can provide concise feedback as to the exact cause of the problem, and where it is located in the device configuration.

If required, for very complex designs the ABLE code, which is generated during the compilation process, may also

be edited, PAC-Designer provides ABEL editing for these cases, as well as a logic simulation tool.

As the Power Manager components are in-system programmable devices programming is performed through a 4-wire, IEEE 1149.1 compliant serial JTAG interface. Once a device is programmed, all configuration information is stored on-chip, in non-volatile E2CMOS memory cells. In the evaluation and prototyping phase the Lattice ispDOWNLOAD cable may be used to connect the parallel port of a PC to the part's JTAG interface. The download process itself is controlled by the PAC-Designer software or another suitable JTAG programming tool like the ispVM System from Lattice Semiconductor.

Integration and Programmability Benefits with Power Manager

The power manager family from Lattice Semiconductor greatly simplifies implementation of complex power-supply sequencing and monitoring systems

and reduces design time. Programmability reduces prototype-debugging time, and by programming the threshold voltages, power supply margining tests can be performed even on the production line.

The PAC-Designer software package which can be downloaded from the Lattice Semiconductor website (www.latticesemi.com) free of charge fully supports the parts' re-programmability and offers an easy to learn approach to device configuration and programming.

Contacts:
Lattice Semiconductor
Johannes Fottner
Senior Analog Field Application Engineer
Lilienthalstrasse 27
D-85399 Hallbergmoos
Germany

Johannes.Fottner@latticesemi.com

Lattice Semiconductor UK Limited
Bernie Perrin
European Marketing Manager
1st Floor Melita House
124 Bridge Road
Chertsey
Surrey
KT 16 8LH
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Power MOSFET Package Selection

Support next-generation DC/DC applications

Emerging requirements for the MOSFET primary switch must be evaluated against newer packages and silicon technologies.

By Yalcin Bulut and Andrew Smith, Siliconix

Today's DCDC converters can generate large amounts of power despite their small size. Power architecture changes, including the introduction of an intermediate bus voltage rail, have resulted in a shift to point-of-load (POL) implementations for lower-voltage and non-isolated converters. Consequently, the area available for the primary switch is reduced and the power space allocation must now accommodate both POL converters and intermediate bus rail power modules. Examining the size, thermal limits, and electrical performance required by next-generation DCDC converters with respect to power elements in Table 1.

As power converters become smaller, the SO-8 footprint area occupies a relatively large part of the available board area for DCDC converters. Therefore, maximum MOSFET space utilization is critical. Table 2 summarizes the thermal conductivity for different packages, including small-footprint options. The smaller packages become, the more that non-scaling factors such as wire bond terminations and voltage isolation circuitry occupy the available die area for active silicon.

In applications where a large die area is required, such as in higher-current primary switches running at low switching frequencies, an increasingly popular

approach is to assign the required silicon area to several power MOSFETs working in parallel. The smaller packages aid the board designer in positioning power components close to the power train while preventing excessive heat build-up in that area of the PCB.

The criterion for determining the optimum thermal package for the MOSFET is its ability to conduct heat away from the silicon (Table 2), limiting the temperature rise on the surface of the die to less than 150 °C without occupying excessive board space.

Package Type	Maximum Dimensions (mm)				Rth (°C/W)
	L	W	H	Footprint (mm ²)	
So-8	5	6.2	1.75	31	16
TSSOP-8	3.1	6.6	1.2	20.46	52
PPAK1212	3.5	3.3	1.07	10.89	2.4
TSOP-6	3.1	2.98	1.1	9.24	30
SSOT-23	3.04	2.64	1.12	8.03	50

Table 2. Thermal Conductivity by Package Type.

These criteria enable designers to match package configurations to design applications based on the power dissipated by the primary MOSFETs in each switching topology.

Required Performance Characteristic		Units	1/2 Brick	1/4 Brick	1/8th Brick	1/16th Brick
Power Brick Parameters	Current Rating	A	150	100	50	40
	Target Efficiency	%	95	95	95	98
	Maximum Ambient Temperature	°C	50			
Board Space	Available Footprint ~ 10%	Inch ²	4.93	3.01	1.86	1.15
Switching Voltage (48-V Bus) Allowing for Typical Switching Transient	1/2 Bridge/Full Bridge	V	80-100			
	2 Transistor Forward		150-200			
	Single Transistor		150-250			
	Immediate Bus		40-50			

Table 1. Basic Requirements for Power Bricks.

Primary switch power loss is a combination of conduction losses and switching losses. Because $r_{DS(on)}$ is proportional to temperature, maximizing the transfer of energy away from the MOSFET die will improve efficiency. The relationship between die temperature and conduction loss can be described by the following equation:

$$T_s = C / (1 - C/125)$$

Where

$$C = R_{thja} \times I^2 \times r_{DS(on)} (25) \times K$$

K = Normalized variation of $r_{DS(on)}$ with temperature (typically around 1.8)

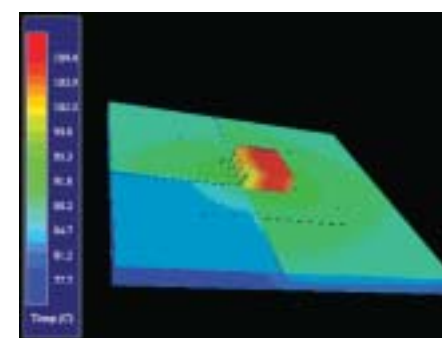


Figure 1a. Thermal Model of SO-8 and PowerPAK 1212-8 Parts Delivering Equal Power Die Temperature: Maximum Die Size in Single SO-8.

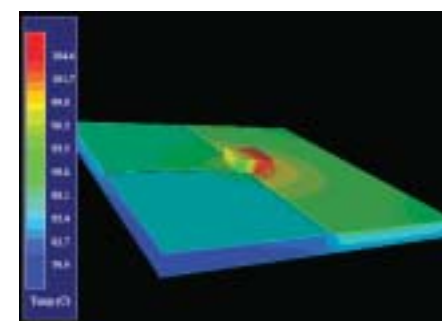


Figure 1b. Thermal Model of SO-8 and PowerPAK 1212-8 Parts Delivering Equal Power Die Temperature: Maximum Die Size in Single PowerPAK 1212-8.

The thermal simulation models in Figure 1 use 1 W of power and a 1-in. by 1-in. FR-4 double-sided 0.062-in. thick PCB with 100% Cu on both sides—the same PCB type used for

datasheet characterizations while specifying R_{th} values. The temperature values indicate a maximum die temperature for 1 W at 25 °C ambient. Figure 1a shows the maximum die temperature as 109.4 °C for a bond-wired SO-8 device using the maximum die size available. The die temperature drops to 104.4 °C for a bond-wired PowerPAK® 1212-8 device with a maximum die size (Figure 1b).

By minimizing the temperature rise of the die with good thermal conductivity, it is possible to reduce conduction power losses by reducing the increase in $r_{DS(on)}$ due to temperature.

Figure 2 shows a comparison of two generations of PWM-optimized silicon technologies in the same unit area. Recent improvements allow MOSFET manufacturers to offer similar electrical performance in substantially smaller



Figure 2. Comparison of 113M- and 300M-Cell Trench Processes.

die sizes, and hence smaller packages, compared to previous-generation devices.

Different switching topologies require power MOSFETs with different breakdown voltages. Increasing the V_{DS} rating

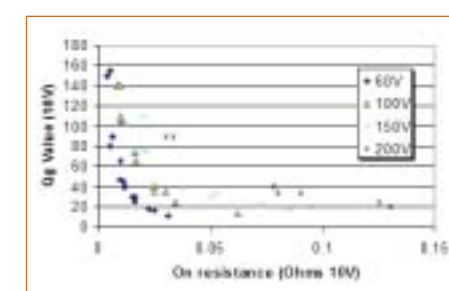


Figure 3. Effect of V_{DS} Ratings on MOSFET Performance.

has a detrimental effect on $r_{DS(on)}$ due to longer channel lengths. This translates into an undesirably larger figure of merit ($r_{DS(on)} \times Q_g$) for the device.

MOSFET power losses consist of conduction losses, dependent on $r_{DS(on)}$, and Q_g switching losses, which are dependent on frequency. At low frequencies or in a high-current application, conduction losses account for most of the overall power dissipation. To reduce the size of the power magnetics used in the converter, designers use higher switching frequencies, which in turn increase switching power losses to a level at which they may be the predominant loss factor in the switch.

Switch transition losses and turn-on delay times— Q_{gd} - and Q_{gs} -related parameters, respectively—are a function of die size for a given technology, where as $r_{DS(on)}$ losses are inversely proportional to the active area of the MOSFET die. Thus, at low switching frequencies, the largest possible die size is the best solution. At higher frequencies, a smaller die reduces switching losses.

A graph mapping power loss against die size for different switching frequencies determines the optimum die size for an application. Different MOSFET voltage ratings exhibit different power-loss characteristics. Figures 4a and 4b show typical frequency-response characteristics for a 60-V MOSFET and 200-V MOSFET. The plots are highly dependent on drive conditions and load current.

Key Parameters at Fig. 4a	
Iout, Amps	4
Idrv-on, Amps	1
Idrv-off, Amps	1
Vin, V	48
Duty Cycle	75%
Vdrive, V	8.5
Package Resistance, mOhm	1.3
Rds Factor	0.7
Qg Factor	1.6

Estimated performance for half-bridge configuration with 25 °C die temp.

Key Parameters at Fig. 4b	
Iout, Amps	2
Idrv-on, Amps	1
Idrv-off, Amps	1
Vin, V	48
Duty Cycle	35%
Vdrive, V	8.5
Package Resistance, mOhm	1.3
Rds Factor	0.7
Qg Factor	1.8

Estimated performance for half-bridge configuration with 25 °C die temp.

The graphs show a crossover in performance for different die sizes at high frequencies. As switching losses become predominant, smaller die become the optimum solution, as represented by the lowest point on the curve. Lower VDS-rated MOSFET dies have lower crossover points than the higher-voltage silicon processes. The selection of MOSFET VDS rating and hence silicon process is governed by switching topology and associated voltage. Graphical data (Table 3) identify the ideal power MOSFET die size for a particular frequency range and drive/load condition.

Combining this data with die size limits for different packages (Table 4) yields

Silicon Process (Vds)	Frequency (kHz)				
	200	400	600	800	1000
60	7mm	4mm	3mm	3mm	3mm
100	7mm	6mm	4mm	3mm	3mm
150	7mm	5mm	4mm	4mm	3mm
200	7mm	5mm	5mm	5mm	4mm

Table 3. MOSFET Optimum Die Active Area vs. Frequency



Figure 4a. Graph of Optimal Efficiency Converter Application (60-V MOSFET).

the best package type for a particular switching condition. Thermal and electrical characteristics also must be considered. A 7-mm-square die using the process geometry selected for a 60-V process corresponds to an $r_{DS(on)}$ of approximately 12.5 milliohms. The $r_{DS(on)}$ for a 200-V process with the same die size would be approximately 100 milliohms for a V_{DS} of 4.5 V.

Silicon Process (Vds)	Frequency (kHz)				
	200	400	600	800	1000
60	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212
100	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212
150	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212
200	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212	SO-8 TSSOP-8 PPAK1212

Table 4. MOSFET Selection Based on Die Size for a 200-W Application.

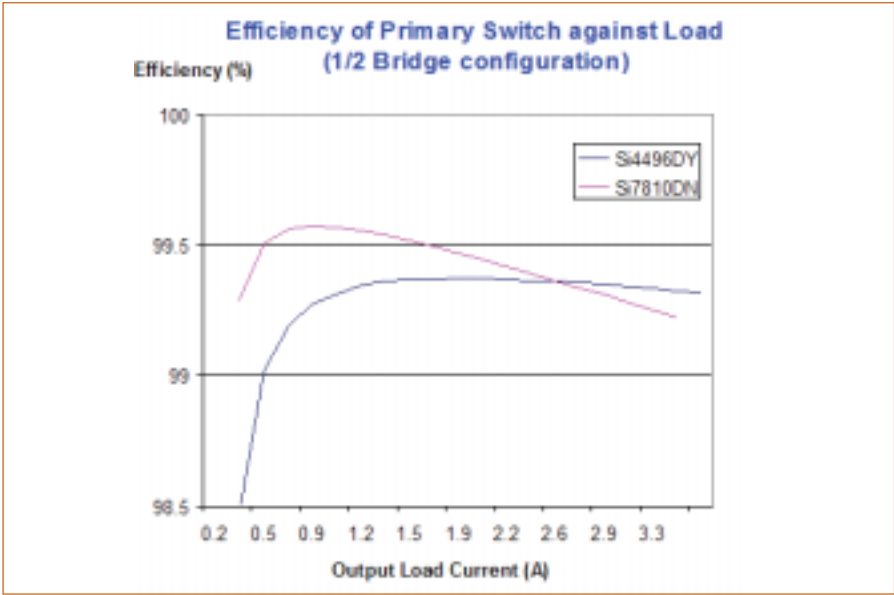


Figure 5. Efficiency of Primary Switch vs. Load.

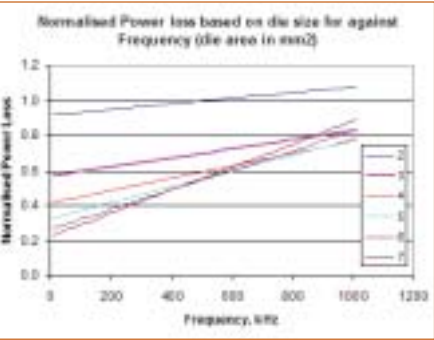


Figure 4b. Graph of Optimal Efficiency Converter Application (200-V MOSFET, 48-V Input Voltage).

Using a MOSFET optimized for the switching conditions to give lowest total power loss will demote the importance of SO-8 and similar large packages, especially for smaller designs, but they will continue to play an important role in high-power applications and at lower switching frequencies.

The importance of correct MOSFET sizing is demonstrated through a design exercise employing two devices using similar silicon, the PowerPAK 1212-8 Si7810DN and the SO-8 Si4496DY. The PowerPAK 1212-8 device has half the silicon area of the SO-8 device, but for dc-to-dc load currents up to approximately 30 A, it provides a better primary switch option. Performing a first-order thermal calculation suggests that with its improved thermal performance, the PowerPAK

1212-8 will run about 15 °C cooler than the SO-8 part for a given power loss.

Si4496DY in Fig.5	
Qg (nC)	29
Qgs (nC)	9.9
Qgd (nC)	10.3
Rdson 6V (Ohms)	0.031

Si7810DN in Fig.5	
Qg (nC)	13
Qgs (nC)	3.5
Qgd (nC)	4.6
Rdson 6V (Ohms)	0.084

Parameters of Fig. 5		
Input Voltage	V	48
Duty Cycle		0.64
Switching Frequency	Hz	350000
Vgs	V	4.5
Output Efficiency	%	0.95
Output	V	2.5
On Driver Current	A	1
Off Driver Current	A	0.8

Estimated power loss per MOSFET in a half-bridge configuration.

High thermal conductivity from die to substrate (R_{thj-c}), as demonstrated by the PowerPAK 1212-8, offers power savings and allows the die to switch higher currents with increasing power density.

Maximum efficiency in dc-to-dc converters can be achieved by selecting the appropriate die size to carry out the switching application, reducing heat build-up in the die area by means of good thermal conductivity within the MOSFET, and using board space effectively with packages that can accommodate a large silicon area.

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Monolithic Inverter IC to Meet Strict Regulations

Dielectric isolation: Latch-up avoidance

Single Chip Monolithic Inverter ICs have made a giant leap towards improving low power low cost solutions for many consumer and industrial motor drive and multiplexer based applications.

But could they be one giant leap too far for the unsuspecting?

By Neil Markham and Akira Uragami, Hitachi

With or without European legislation stipulating energy conservation, the world's manufacturers of power systems have been quick to adopt new technologies aimed at energy consumption reductions. Not least Hitachi—first to design and market the monolithic inverter IC to meet strict regulations in Japan for Brushless DC (BLDC) based air conditioning systems some 15 years ago. The principle of inverter control for motor drives has been, and will continue to be, a key influential factor in reducing losses and meeting energy targets.

Motor control development engineers are well aware of the many off-the-shelf motor control solutions; single chip, power module, pre-driver and IPMs to name but a few generic types. These can be cost effective and reduce time-to-market—allowing motor drive designs to be turned around relatively quickly in a modular approach. But what about longer term operation? With every effort made to ensure trouble free operation, could you be inadvertently designing problems in?

Integrated circuit solutions may utilize a host of different technologies within production, but perhaps one that is not covered often enough is isolation structure. Isolation described here refers to cell-to-cell isolation.

The single-crystal silicon island in Figure 2 incorporates transistors, MOS, and other devices. The depth of this single-crystal island can be several micrometers, although this varies depending on the voltage withstand capability required. The silicon dioxide (SiO_2) film isolates the single-crystal silicon island electrically whilst the poly-crystal silicon supports the single-crystal silicon island mechanically.

One of the principal features of Hitachi's dielectric isolation (DI) inverter and pre driver technology is its Latch-up-free performance. This is achieved by the fact that isolators surround specific active devices. Latch-up occurs on a cross-section of a device where a pnpn structure is formed, including the Si board. The pnpn structure may have the tendency to function as a thyristor, such that if this thyristor portion is triggered, perhaps due to noise or other system factors, that portion is short-circuited by a single diode. In this case, the maximum current that can be produced by the specific power supply unit will continue to flow until the power supply is powered off. These circumstances require either controlled turn off by a separate monitoring circuit or in a worst case scenario, turn off will occur due to device destruction. PN junction isolation used in general ICs always has a pnpn structure somewhere, so latch-up may potentially be unavoidable.

The DI process can easily be replicated for higher voltage levels. For example a dioxide film that surrounds a single-crystal silicon island may have a voltage withstand of close to 300V with a size of about 1 micrometer. Using thicker deposits, for example, allows a 600V withstanding voltage.

The use of DI is not limited to device type either. The entire device is integrated with a DI structure, including thyristors, GTOs, IGBTs, and various other devices, so all may be integrated into an IC. Circuit diversity may be arranged quite independently on a silicon board, so that it is possible to produce various circuit arrangements as described below:

1. The logic ground and power ground can be completely isolated from each other, and a potential difference of more than 1V can be tolerated between the ground.
2. totem pole circuit can be composed of pnp-npn transistors.
3. A floating circuit can be built.

Dielectric Isolation ICs can function in a higher temperature range than that of a PN junction isolation structure that is used in most general ICs. In the case of PN junction isolation for example, the leakage current of a diode used as an isolation layer rises quickly due to secondary temperature rises. Unlike standard PN isolation techniques, each

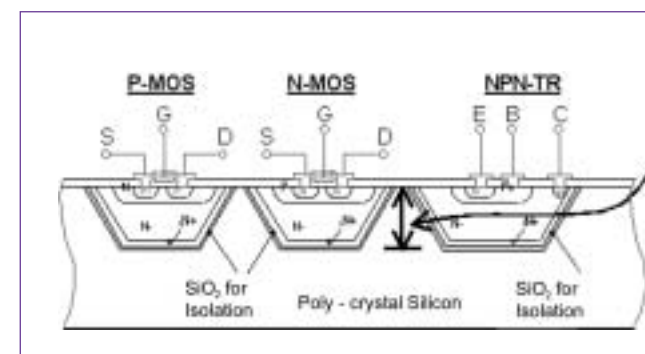


Figure 1. Cross-section of the dielectric isolation structure.

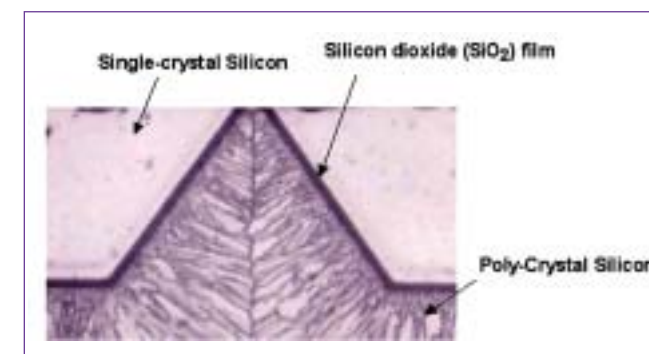


Figure 2. Cross-sectional photograph of a dielectric isolation structure.

device within a dielectrically isolated IC is covered with an isolator, so that it can function in a relatively high temperature range.

In summary Hitachi's dielectric isolation single chip inverter IC series, ECN3xxx, can avoid catastrophic field failures during un-foreseen latch-up con-

ditions. The monolithic structures can combine logic and power stages for high efficiency, small footprint, and low cost HVIC inverter solutions with peak currents up to 5.0A and single VSP or six inputs.

For more information, please contact:

Neil Markham

Tel: +44 (0)1628 585 000

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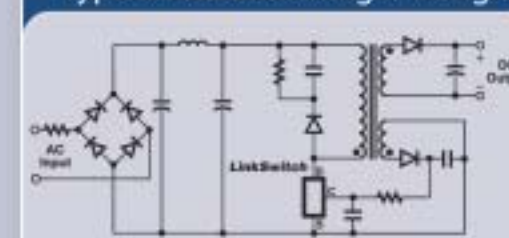
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Typical LNK520 Charger Design



Output Power Table

Product	Power Rating	No-load Input Power	CC Tolerance
	230 VAC ±15%	85-265 VAC	
LNK520	4 W	3 W	<300 mW
P or G	5.5 W	3.5 W	<500 mW
			±24%



P = DIP-4



G = SMD-6

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POWER
INTEGRATIONS

PolySwitch Devices to Protect Linear Transformers

Applications are now at line voltage conversion circuits

The dual protection capability and resettability characteristics allow the LVR devices to integrate the functions of two devices into one and can help reduce warranty and service costs for equipment manufactures.

Matthew Chamberlain, Raychem/Tyco

This article provides recommendations for using Raychem Circuit Protection's LVR Series of PolySwitch polymeric positive temperature coefficient (PPTC) devices to help protect linear transformers in line-voltage conversion circuits. The new LVR devices are capable of operating at line voltages of 120 VAC and 240 VAC, making them suitable for protection on the primary side of transformers. The LVR devices can help protect transformers and electronic circuits from two major fault modes—excessive voltage on the primary side and short circuits on the secondary side. In addition to the current limiting function of the LVR devices, their ability to sense and respond to elevated temperatures can make them suitable for protecting the primary windings of the transformers.

There are several strategies that can be used to protect linear transformers from excessive current, excessive voltage, and overheating damage. A common method is to use a thermal fuse on the primary side and a current-limiting

device on the secondary side. This solution can help protect against both overheating and over-current conditions. A weakness of this approach is that thermal fuses are one-shot devices, and a fault will disable the transformer. Since thermal fuses are typically embedded into transformers, if the fuse blows, the transformer or even the entire circuit board may have to be replaced.

The LVR device family is designed to bring the overcurrent and overtemperature protection advantages of PolySwitch PPTC devices into AC Mains line voltage applications. With its 240VAC rating the LVR series can continue to help protect equipment against overcurrent faults as well as help provide thermal protection in step down and isolating transformers. The dual protection capability and resettability characteristics allow the LVR devices to integrate the functions of two devices into one and can help reduce warranty and service costs for equipment manufactures.

Tyco Electronics has recently released Raychem Circuit Protection's PolySwitch LVR devices, designed to help provide primary side protection for linear transformers and secondary side electronic circuits. The LVR technology is built on the well-known and proven capabilities of PolySwitch devices but features a higher voltage rating, allowing them to be considered for circuit protection designs that might otherwise require more expensive solutions. In addition to the traditional current limiting capability of PolySwitch devices, the LVR devices can also help protect equipment against elevated temperature conditions. This can make them suitable for thermal protection of transformers as well, offering both overcurrent and overtemperature protection in a single device. Also, because the LVR device can be reset after a fault event,¹ it does not normally require replacement. These advantages help equipment manufactures reduce product, warranty, service, and repair costs.

Linear transformers are widely used in power conversion devices for appliances, building automation systems, portable electronics, rechargeable power tools, answering machines, travel power converters, cordless phones and cell phones. The power supplies for these devices are usually taken for granted by the end user. If they fail, the result may be significant down time or need for replacement.

LVR Devices Provide Overcurrent Protection

A common electronics system fault is a short circuit on the transformer's secondary side. Such a fault can be caused by a failure within the equipment or by shorts in the connected loads. This fault condition will cause an increase in current in both the secondary and primary windings, resulting in increased temperature in the windings which can lead to degradation and eventual failure.

The LVR device, when wired into the transformer's primary, is subjected to this increase in current and helps provide overcurrent protection for the system by transitioning to its high impedance state at its specified trip point. This limits the primary side current and consequently the secondary current, thus helping protect the secondary electronics from overcurrent damage. The LVR device remains in the high impedance state until the fault is removed and the LVR device is allowed to cool down to return to its low resistance state. In most cases, to allow the LVR device to reset, the fault condition and power to the equipment may have to be removed. Once the LVR device has reset, normal equipment operation may be resumed.

LVR Devices Sense Overtemperature Conditions

PolySwitch devices will also trip when their internal temperature rises above a certain level regardless of the amount of current flowing in the device and the LVR devices are no exception. This property allows the LVR device to be used as an overtemperature protection device as well as an overcurrent protection device. The overtemperature sens-

ing component of the LVR device can be critical in applications where a fault may cause a rise in the winding temperature without a substantial increase in current draw. Replacing the thermal fuse that is typically wound into a transformer with an LVR device can fully leverage the dual protection capabilities of the LVR products.

For example, consider a fault in which a loose neutral wire causes 240VAC to be applied to a 120VAC Mains circuit. In this case, the increased current in the transformer primary may not exceed the trip current of the overcurrent device. This is typically the reason a thermal fuse is placed in a transformer primary side in addition to an overcurrent device in the transformer secondary. The thermal fuse senses the transformer temperature rise and stops the flow of current by opening the circuit when it reaches a specific temperature. This can prevent failure of the transformer but requires replacement of the transformer component or its circuit card once the loose neutral condition is repaired. This means equipment down time and a service call or replacement.

Alternatively, an LVR device can be used in place of the thermal fuse. The LVR devices are typically small enough to be integrated into a transformer in a similar manner to the thermal fuse. Heating of the transformer will cause an associated rise in the LVR device temperature causing the LVR device to trip. This reduces the current flow, preventing further temperature rise in the transformer. Therefore, not only will the LVR device trip due to excessive currents, it will also trip if the transformer overheats. As in the overcurrent case, the LVR device remains in the high impedance state until the fault is cleared and power is removed and the LVR device is allowed to cool down. Once the LVR device has reset, normal equipment operation may be resumed. It is important to note that the LVR device not only helps protect the transformer and secondary electronics from overcurrent and overtemperature damage, it is a resettable device. Therefore, the equipment it helps protect does not typically require a

service call to return to operation. This is not true of equipment that uses single use fuse protection schemes. Therefore, equipment that uses an LVR device can save equipment users time and expense by eliminating or minimising expensive service calls and equipment downtime.

Ceramic PTC devices are another resettable protection option for transformers. Compared to a CPTC device in this application, the LVR device can limit the maximum temperature of the windings to a lower level and offer a lower surface temperature (100°C to 120°C) in the tripped state. Depending on the voltage applied, a CPTC device may reach a surface temperature of 180 to 220°C in its high resistance state. This renders it an unsuitable solution for overtemperature protection when the insulation rating of the windings is lower than the CPTC surface temperature. The composition of the CPTC also tends to be brittle, which makes it vulnerable to damage from shock, vibration, or the thermal stress of heating and cooling found in many transformer applications. The LVR device typically has lower resistance in the circuit, is much lower in capacitance, is less frequency dependent, and is smaller than a comparable continuous current rated CPTC device. The characteristics of LVR devices can make it a preferred solution to help provide both overcurrent and overtemperature protection on the primary side of linear transformers.

The LVR series of PolySwitch resettable devices are rated at 240 VAC, permitting maximum voltages of up to 265 VAC, and are available in hold currents from 50 mA to 400 mA. The packages are simple round or rectangular radial-leaded devices of various sizes. Some important device parameters are shown in Table 1.

Definitions:

Hold Current—the largest steady-state current that, under specified conditions, can be passed through a PolySwitch device without causing the device to trip.

Trip Current—the smallest steady state current that, if passed through a PolySwitch device, will cause the device

Device Number (mA)	Hold Current at 20°C (mA)	Trip Current (ohms)	Initial Resistance (ohms)	R1 MAX (ohms)
LVR005	50	120	18.5-32.5	65
LVR008	80	190	7.4-13.0	26
LVR012	120	330	3.0-6.5	12
LVR016	160	440	1.9-3.4	7.8
LVR025	250	700	1.1-1.9	3.8
LVR040	400	980	0.6-1.7	2.3

Table 1. LVR Product Overview.

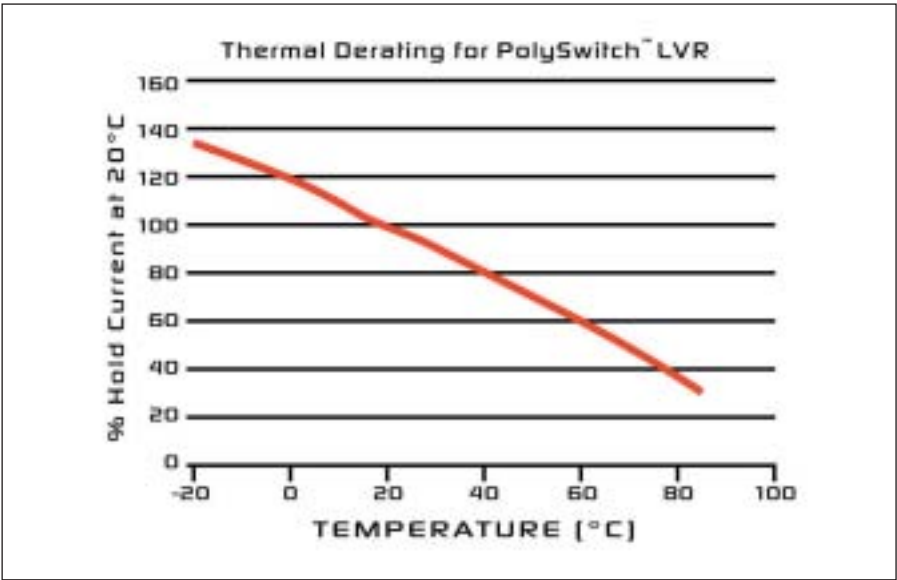


Figure 1. Thermal Derating Curve.

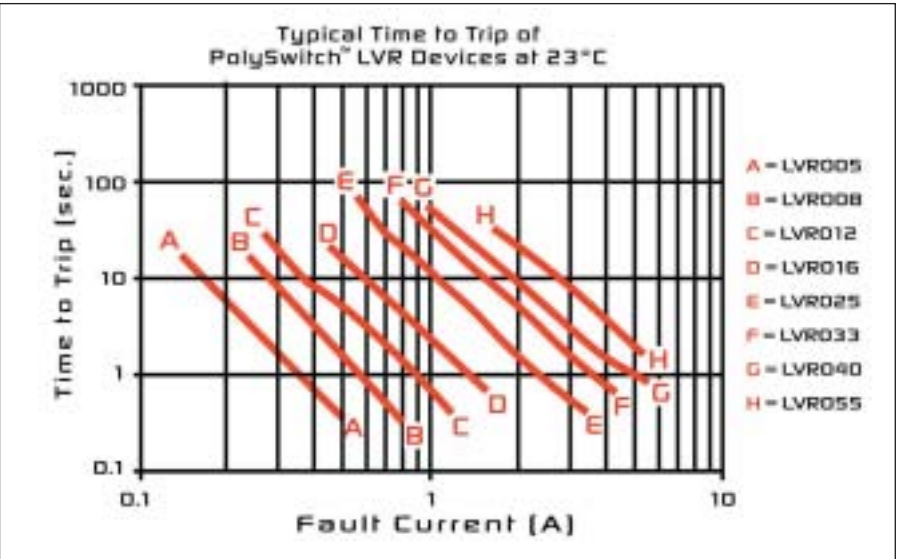


Figure 2. Typical Time-to-Trip Characteristics.

to trip, under specified conditions.
 R_{1MAX} —the maximum resistance of a PolySwitch device at room temperature

one hour after being tripped or after reflow soldering.

Several device characteristics must be considered when applying the LVR device to a linear transformer circuit. Selecting the best device for the application requires an understanding of the thermal derating characteristics shown in Figure 1. As shown, the average hold current rating decreases by about 1% for every degree of increase in ambient temperature. This means that the actual operating temperature of a transformer must be considered when evaluating the hold current capability of the LVR device.

Another design consideration is time-to-trip. As shown in Figure 2, the typical time-to-trip of a device is dependent on the trip current and the device size.

When integrating an LVR device into the transformer assembly, the LVR device is chosen so that it trips at the desired current level and the required overtemperature level. Care must be taken to consider the heating contributions of both current and transformer heating when selecting an LVR device for an application.

PPTC circuit protection devices are made from a composite of semi-crystalline polymer and conductive particles. At normal temperature, the conductive particles form low-resistance networks in the polymer (Figure 3). However, if the temperature rises above the device's switching temperature (TSw) either from high current through the part or from an increase in the ambient temperature, the crystallites in the polymer melt and become amorphous. The increase in volume during melting of the crystalline phase causes separation of the conductive particles and results in a large non-linear increase in the resistance of the device.

The resistance typically increases by three or more orders of magnitude, as shown in Figure 4. This increased resistance helps protect the equipment in the circuit by reducing the amount of current that can flow under the fault condition to a low, steady state level. The device will remain in its latched (high resistance) position until the fault is cleared and

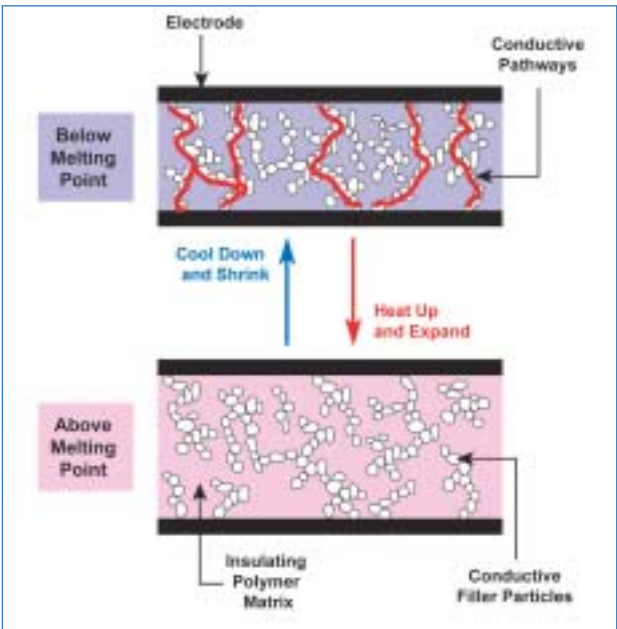


Figure 3. PPTC Crystalline Structure.

power to the circuit is removed—at which time the conductive composite cools and recrystallises, restoring the PPTC device to a low resistance state, and the circuit and the affected equipment to normal operating conditions.

Raychem Circuit Protection's LVR devices now offer overcurrent and overtemperature protection options for the transformer primary. These devices provide the advantage of being able to perform the functions of both overcurrent and overtemperature components within a single device. This can help equipment manufacturers reduce costs by reducing component count and the number of suppliers they must maintain. The resetability of the LVR PPTC devices also benefits equipment manufacturers by helping to reduce service and warranty costs. These advantages are not matched by existing single use fuse solutions.

1 WARNING: Under a fault condition all LVR devices go into a high resistance state. This allows proper operation, but it can still result in hazardous voltage being present at the LVR device locations. Also, after a fault triggers the LVR device, the power and the fault condition must be removed from the circuit for a short period of time to allow the LVR device to cool down and return to its low impedance state.

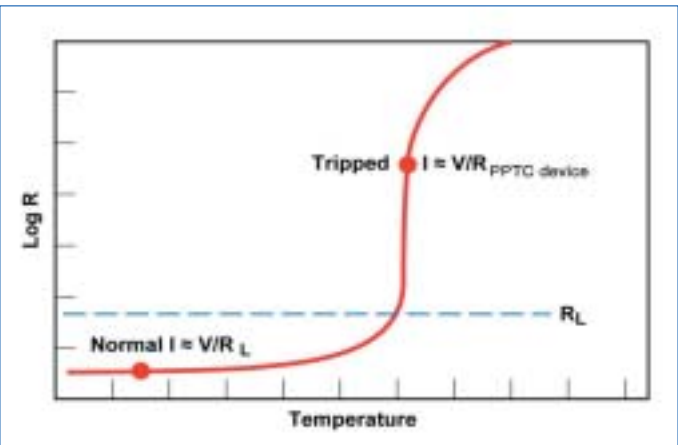


Figure 4. Typical operating curve for a PPTC device.

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Adaptive deadtime control IC for halogen lamp



An internal sample and hold system allows approximately the same delay to be used to set the high-side driver (HO output) high after LO has gone low. Adaptive deadtime control reacts on a cycle-by-cycle basis of the oscillator and adjusts dead time as necessary to maintain soft switching regardless of external conditions.

Mike Wigg, International Rectifier Co Ltd,
European Regional Centre, 439/445
Godstone Road, Whyteleafe, Surrey,
CR3 0BL
Tel; + 44 (0)20 8645 8003
Fax; + 44 (0)20 8645 8077
e-mail: mwigg1@irf.com

www.irf.com

TIR introduced the IR2161 control IC specifically designed for electronic transformers that drive low voltage halogen lamps. All necessary features are integrated into a single 8-pin DIP or SOIC.

The device can adapt to changing supply voltage, frequency conditions, and lamp conditions enabling the introduction of highly-reliable halogen transformers while streamlining their design and manufacture.

Featuring IR's rugged high voltage IC technology, this compact 8-pin device incorporates a 600V half-bridge driver, advanced overload and short-circuit protection circuitry with high temperature shutdown and adaptive control techniques offering a reliable alternative to the traditional approach based upon self-resonating, bipolar transistor half-bridge circuits. The IR2161 also accommodates external dimming with a standard phase-cut, triac-based dimmer. Compared to similar circuits using discrete components, the IR2161 can reduce component count by 20%.

Adaptive Deadtime Control is a key feature of the IR2161, which increases transformer reliability by continually maintaining soft switching. The IC has an active deadtime circuit that detects the point at which the DC bus voltage in the half bridge slews to 0V and sets the low-side driver (LO output) high.

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6.5kV IEGT Module for high-power



Toshiba has combined multiple IEGT (Injection Enhancement Gate Transistor) chips, the latest fast recovery diode technology, and an advanced standard package design, to create a compact,

high-efficiency and high-isolation 6.5kV, 600A IEGT module.

The MG600JXH1US53 IEGT module will be ideal for traction control and industrial drives operating under 3kVDC or 4.2kVAC line voltage. The module is based around the company's low saturation, ultra thin punch through (UTPT) IEGT semiconductors. Multiple IEGT ICs have been integrated alongside free wheeling diodes (FWDs) in a plastic package that incorporates an aluminium silicon carbide (ALSiC) base plate. Each IEGT is optimised to achieve the best possible balance between fast switching performance and low conduction loss,

while the FWDs make use of optimised lifetime control techniques for improved reverse recovery characteristics. Use of an ALSiC baseplate ensures high thermal cycling capabilities for extended reliability and lifetime operation.

Angela Fehrenbach, Toshiba Electronics Europe
Hansaallee 181, D-40549 Düsseldorf, Germany
Tel: +49 (0) 211 5296 254
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E-mail: info@toshiba-components.com

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Drive Technology in Hybrid and Electric Vehicle



This power electronics system features pressure contact technology and a high degree of mechanical integration,

both of which are milestones along the path to hybrid and electric vehicles.

The optimized module SKAI (Semikron Advanced Integration) from Semikron, which was developed for hybrid and electric vehicles, fulfils the high reliability performance requirements of the automobile industry thanks to its special pressure contact technology and mechanical integration. In terms of performance features, the SKAI module brings substantial improvements compared with previous product developments.

SKAI is a 3-phase inverter used to convert DC voltage (from the fuel cell) into AC voltage (to the motor drive) with

the additional option of power feedback. The system features an integrated DSP controller, driver and protection functions, DC-link capacitors, semiconductors, isolation, sensors and liquid cooling and communicates with the vehicle via CAN bus.

The power electronics module comes in two typologies. The IGBT module is designed for 600V/1200V, 500A/400A output current, and between 50 and 200 kW motor power, while the MOS-FET typology provides 75V/100V/150V, 700A/600A/500A output current and between 3 and 20 kW motor power.

www.semikron.com

6.5kV High Voltage IGBT Modules



Mitsubishi Electric has newly developed a 6.5kV class IGBT in order to meet the requirements of 3kV DC

catenary voltage in traction applications.

To realise a low loss performance and at the same time a wide RBSOA, Mitsubishi Electric 6.5kV HV-IGBT chips use a Light Punch Through (LPT) design in which the internal chip structure has been optimised for 6.5kV. Development of three modules containing these new 6.5kV class IGBT chips is currently underway: 200A and 600A single switch types, and a 400A chopper module.

These new modules feature a low leakage current, total loss reduction, wide RBSOA and SCSOA. Base plate

material is ALSiC and package isolation (Viso) is guaranteed up to 10.2kVrms at 1min. As all Mitsubishi HV-IGBT modules, this new product range is also subject to 100% production and shipping tests (static and dynamic tests). This extensive test procedure improves module production yield and reduces field failure rate significantly. Thus customers benefit from highest performance and reliability.

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High power IGBT modules up to 6.5 kV



ABB launches a new generation of high power IGBT modules in industry standard housings with the popular 140 mm x 190 mm footprint.

The presently launched HiPak family brings unprecedented electrical robustness thanks to the latest generation of high voltage SPT chips (Soft Punch Through technology).

The presently offered devices use the metal matrix composite material

Aluminium Silicon Carbide (AlSiC) for its base-plate and Aluminium Nitride (AlN) as the isolating ceramic substrate on which the chips are mounted. AlSiC conducts heat almost as well as a metal (e.g. aluminium) but has the thermal expansion coefficient close to that of a ceramic. This technology minimises the stresses between the base-plate and the ceramic substrate during thermal cycling allowing the modules to be used in demanding applications such as Transportation Systems.

ABB uses its well-established SPT technology in an advanced version for the high voltage chip sets (2.5 – 6.5 kV). HV SPT is a breakthrough in IGBT performance as it allows unprecedented turn-off ruggedness i.e. it allows a large Safe Operating Area (SOA). SOA has

been the traditional Achilles Heel of HV IGBTs, forcing users to employ protective techniques such as slow switching or active clamping of the devices. Additionally, recourse to passive clamping and snubbers was also required to avoid costly de-rating. The HV SPT requires no such measures allowing, for the first time, full device rating with efficient, hard (i.e. low loss) switching.

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Electronics Power Systems

announces a new inverter family. The

Electronics Power Systems "flow-through" concept a low inductive system design is easy to realize and it simplifies layouting of a PCB. With 17 mm in height and an outline dimension of 66 by 34,5 mm it is an extremely compact package relative to its applicable power range, which defines an unequalled product in this market.

The new Tyco Electronics Power Systems flowPHASE 0 module family is designed to reduce the expenditure for a solution and to make PCB based inverter design efficient and reliable. The module

is structured as an IGBT half bridge with the opportunity to combine 3 modules to a 3-phase inverter bridge.

Tyco Electronics Power Systems
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Rupert-Mayer-Strasse 44
81359 Munich / Germany
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Fax : + 49 89 722-43 791
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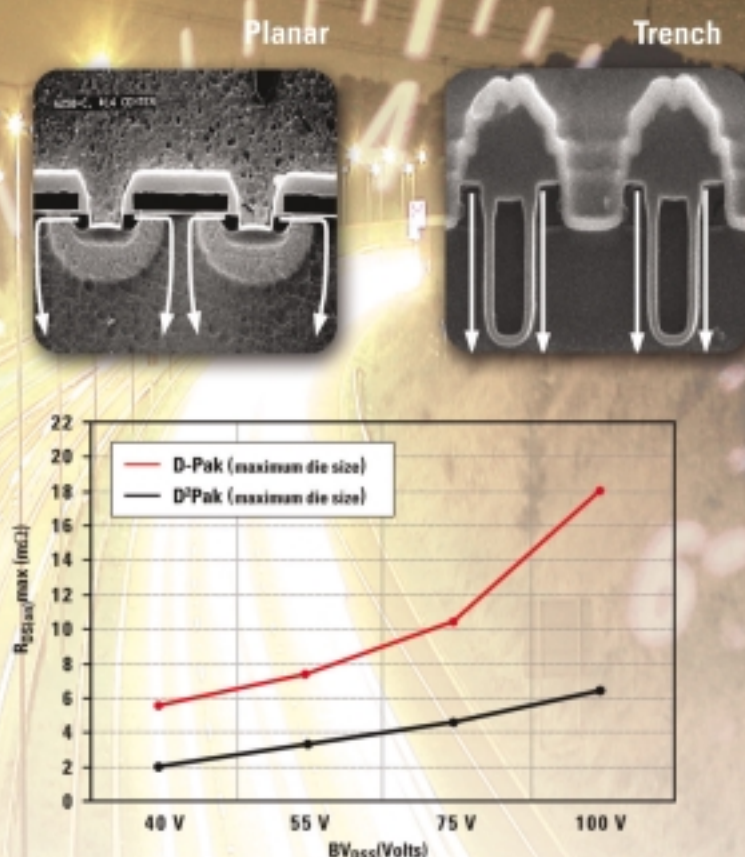
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IRFR4104	D-Pak	40V	5.5mΩ	42A	1.05	1.80	Std	Q101
IRF1406ZS	D-Pak	55V	4.9mΩ	75A	0.85	2.10	Std	Q101
IRFR4105Z	D-Pak	55V	24.5mΩ	30A	3.12	2.10	Std	Q101
IRF1010EZS	D-Pak	60V	8.5mΩ	75A	1.11	2.20	Std	Q101
IRF2807ZS	D-Pak	75V	9.4mΩ	75A	0.90	2.25	Std	Q101

Notes: (1) Package limited value. (2) All D-Pak and D²Pak devices also available in TO-220 and die form in various chip packaging media.

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