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Digital Controlled Supplies Advanced Packaging High Performance Diodes Choose Proper Core

Protection by detection

ISSN : 1812-6385

Fairchild MOSFET BGAs deliver 40A per Phase @ 50 W/in²



Setting the new standard in packaging and performance:

- Superior parasitic source inductance (6 pH for 5.0 mm x 5.5 mm package)
- 50 W/in² power density
- Excellent thermal performance 0.5 °C/W R_{OJC}
- High efficiency
- Exceptional Footprint Figure of Merit (R_{05(pr)} x footprint)

Introducing the package destined to be the industry standard in the world of high current, high switching frequency VRMs for PCs. Fairchild's MOSFET BGAs offer unparalleled high current densities in a package that arguably has one of the smallest footprints and parasitics in its class. So for your next VRM, design-in MOSFET BGAs and get an impressive combination of high efficiency, high power density, highly optimized board space and great time to market.

MOSFET BGAs from Fairchild — setting the new standard in packaging and performance. For more information on Fairchild MOSFET BGAs, go to:

www.fairchildsemi.info/powerbga7

Across the board. Around the world."



Viewpoint It is Worthwhile to go to California in the Winter Industry News Mountaintop, PA expands to 1200 wafers per day Hi-Rel Power Management Research and Design Center Tyco and SynQor form alliance Freescale Semiconductor EPCOS and Continental Temic announce automotive collaboration UK Partner for Advanced Power Conversion Intersil acquires Xicor Cover Story Controlling and Protecting Door-Opening Systems Features Technology Review—Does Digital Controlled Power Supplies Beco Power Player-The Long Way from Electric to Hybrid to Electric to... Thermal Management—Advanced Packaging Boosts Power MOSF DC/DC Conversion—Defining an Intelligent Pin-Out for High Amper-Power Semiconductors—High Performance CAL HD Diodes for 1700V Trench and SPT IGBT's Transformers—Transformers Keep Pace with DC/DC Technology Power Distribution—PCI Bus Systems Thermal Management-Miniaturized IC Packaging for Consumer . Optoelectronics—Optical-Based Analog Front End Transformers-How to Choose the Proper Core for Power Magnetic New Products Power Systems Design Europe Steering Committee M Member Representing

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### It is Worthwhile to Go to **California in the Winter**



To escape from the cold European climate, although the rain in California has taken care, that the ones left at home, have no reason to complain. So my full focus has been dedicated to APEC. No beach time, only work and always Goofy hanging around watching us. Being held in Anaheim at the Disney Hotel adds an extra level of energy.

APEC (Applied Power Electronics Conference and Exposition) has the full support of the IEEE Power Electronics Society. IEEE Industry Applications Society and the PSMA (Power Sources Manufacturing Association). The show and conference had stimulating sessions. A lot of the discussions as well as debate at APEC, centered around DC/DC conversion going to digital control. A way that has to be proven for the broad industry only if it is achievable on cost. Alternative ways of getting power to handheld equipment using signal line connections and the ability to power over Ethernet, is in an intelligent way to provide a new approach to save power and make it more handv for many applications.

I ran into Myron Miller, the founder of PCIM Show and magazine for more than three decades ago. We reflected on PCIM starting at the same time that the inspiring California Beach Boys began their career. Their songs continue to be popular. PCIM had become a well known brand all over the world but the new owners and different business decisions resulted in the closure of the magazine.

PCIM Europe magazine would have shared a 15 year anniversary this March. We have learned that this industry has to look forward. That is very important for progress, but we have to gain enough knowledge from history that we

are not lost in our direction. I can look forward to provide you the latest information on new product and technical applications to stimulate the future designs.

Mark your calendar for the last week of May to attend the most important European event in Power. The PCIM Europe Conference and Exhibition celebrate it's 25th year anniversary. My association of more than one and a half decades as a board member of the PCIM conference will provide additional fuel for our magazine and keep the focus strongly set for technology and their advanced application.

I will be handling the podium discussions at PCIM 2004 in Nuremberg in the exhibition hall, please make a point to stop by and make your comments. Each day around lunchtime we will have short presentations from experts followed by an open discussion. The subjects include semiconductors as the focal elements for power electronics. MOSFETs on Tuesday, IGBTs on Wednesday and Rectifiers on Thursday. I am looking forward to seeing you and chat with you at the podium.

If you have any comments or suggestions on Power Systems Design Europe, before I see you in Nuremberg, please send an e-mail.

See you at the show in Nuremberg!

Best regards

Bodo Arlt Bodo.Arlt@powersystemsdesign.com

# An easier way to measure currents up to 400A?

Yes, the HAIS series is available just the way you want it:

- 1. With ref-out mode, access to the zero point, and internal reference voltage;
- 2. Or with the possibility of external reference voltage for the zero current output level;
- 3. Or with integral bus bars for the 50 and 100A models.

#### Put the advantages of the HAIS series to your advantage:

- Current ratings from 50A to 400A for PCB mounting
- Bipolar AC, DC or complex current measurements
- Single 5V power supply
- Open-loop transducer with ASIC technology
- Low power consumption
- Operating temperature range : -40°C to +85°C

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#### Mountaintop, PA expands to 1200 wafers per day



Fairchild announced an expansion of its Mountaintop 8-inch facility, dedicated to manufacturing power components. The expansion includes refurbishing a 15,000 square-foot clean room

and installing state-of-the-art tooling and support systems to increase Fairchild's production capacity, particularly for its discrete power line. Upon completion, the plant will be capable of producing 1200 wafers per day.

Fairchild will invest \$143 million in the

expansion, creating 320 new jobs over four vears. The announcement was made with the State of Pennsylvania, offering an Opportunity Grant financial package including an initial arant of \$1 million over two fiscal years, training funds and an offer of low interest loans through the PA Industrial Development Authority. Fairchild's Mountaintop facility is one of the few wafer fabrication facilities in the world dedicated to manufacturing 8-inch discrete power devices including IGBT products and trench MOSFETs.

"Our bookings are running at their highest level in more than three years, and we want to ensure Fairchild has the capacity to meet

this increased demand for power solutions," Pond said. "We're pleased to partner with the State of Pennsylvania to strengthen our 8-inch facility, while contributing to the economic growth of the Mountaintop community. This is truly a win-win situation for Fairchild and for the State. Total power component sales now represent 72% of our revenue. By increasing our operational efficiency through modernizing our factories, increasing our capacity at Mountaintop, and ramping our new Suzhou, China assembly and test facility, we are well poised to meet increased end market demand."

www.fairchildsemi.com

#### **Hi-Rel Power Management Research and Design Center** in Denmark

International Rectifier announced the opening of IR Denmark ApS (IRD), a research and design center for advanced high-reliability DC-to-DC converters and other power management solutions. The latest addition to IR's growing network of R&D facilities around the world. IRD is located in Skovlunde near Copenhagen. The center will focus on higher level solutions for space applications and house a team of highly trained engineers with extensive experience in space-level power management design

and customer support. IR Denmark complements International Rectifier's strong heritage and design expertise in space level power management applications.

"The establishment of IR Denmark will allow us to deliver not only the most reliable products for one of the most demanding applications, but also an outstanding level of customer service, especially to our large and growing customer base in Europe," said Bel Lazar, Vice President of Operations and R&D for International Rectifier Hi-Rel Products.



Products designed at IR Denmark will be manufactured at International Rectifier's space qualified facility in Santa Clara, California.

www.irf.com

#### Tyco and SynQor form alliance



Tyco Electronics Power Systems and SynQor have formed the Distributed-power Open Standards Alliance (DOSA) to ensure future DC-DC product compatibility and standardization within the increasingly fragmented power converter market. Ultimately, the alliance will be the vehicle that establishes standards over a broad range of power con-

and functionality for both non-isolated (POL) and isolated applications, including intermediate bus converters. Alliance membership is open to qualified companies per the alliance charter. DOSA converters will be geared towards wireless infrastructure, optical switching, networking, storage and industrial systems. Siegfried Kreuzer, SynQor and Manfred Krimbacher, Tyco introduced the DOSA standards to Europe. Under the terms of the alliance, the members will independently develop DC-DC converters with pinfor-pin compatibility, identical form factors and functionally equivalent feature sets,

verter form factors, footprints, feature sets

thereby guaranteeing end users the benefits of true second sourcing options. Tyco's recently announced Austin Lynx II POL converters will be the first product addressed by the alliance. DOSA will also align future product roadmaps, including a new sixteenth brick converter, while developing other requirements, including high current quarter brick pin-out designs, output voltage sequencing for POL modules in the Austin SuperLynx™ module form factor and consensus for standards on surface-mount technology and leadfree initiatives.

www.synqor.com

www.power.tycoelectronics.com

#### **Freescale Semiconductor**

Motorola unveils Freescale Semiconductor as semiconductor unit sets its course for future independence. The name is planned for separation from Motorola later this year.

Freescale Semiconductor's name was chosen to reflect a new focus for the semiconductor company. The naming process was built upon interviews and research

conducted among the company's Employees, customers and analysts worldwide.

www.motorola.com



#### Power for Your FPGA and DDR Memory Designs

Intersil's switching regulators (PWMs) maintain efficiencies in excess of 90% in your FPGA and DDR memory designs, even when the input and output voltages differ by a large amount and the current requirements range from a few milliamps to 100A. Intersil's regulators are available in several configurations including singlephase, multi-phase, integrated FETs up to 8A and up to 100A with external FETs. www.intersil.com/data/AG

#### World's Only 5-in-1 DDR Chip Set Regulators

The ISL6537ACR and ISL6537BCR supply all of the required voltages along a full range of protection features and high integration in small packages. These controllers offer high performance in an ultra-small 6 x 6mm QFN package. www.intersil.com/ISL6537

#### Single-Chip, 80A Capable, Two-Phase **DC-DC Buck Controller**

Intersit's ISL6563 two-phase PWM controller IC integrates MOSFET drivers in a thermally enhanced 4 X 4mm package to deliver a 30 to 80A power solution

www.intersil.com/ISL6563

#### Small, Pre-set Output DC-DC Converter

Intersil's ISL6410 and ISL6410A switchers generate 0.5A and pinselectable output voltages of 3.3V, 1.8V, 1.5V or 1.2V.

www.intersil.com/ISL6410

# Do You Need?



Each technology generation seems to create a new low voltage requirement: 2.5V, 1.8V, 1.5V, 1.2SV, 1.2V, 0.9V and on it goes, intersil offers a broad portfolio of power management ICs to easily generate the voltages you need.







Device	Regulators PWMs	Regulators Linears	Vin	Package/Pin	# of Output Voltages
ISL6521	1	3	5V	SOIC-16	
HIP6021	1	3	5V, 12V	SOIC-28	
HIP6019B	2	2	5V, 12V	SOIC-28	4
ISL6537 (new)	2	2 + Ref	5V, 12V	QFN-28	
ISL6532A	1	2	5V, 12V	QFN-28	2
ISL6402/A (new)	2	1	4.5V to 24V	TSSOP-28, QFN-28	3
ISL6539 (new)	2	0	5V to 15V	SSOP-28	
ISL6227 (new)	2	0	4.5V to 24V	SSOP-28	
ISL6444	2	Ref	5V to 24V	SSOP-28	2
ISL6530/1	2	Ref	5V	SOIC-24, QFN-32	1.0
ISL6528	1	1	3.3V, 5V	SOIC-8	
ISL6529	1	1	3.3V to 5V, 12V	SOIC-14, QFN-16	

#### Learn more about this family and get free samples at www.intersil.com/PSDE

### **How Many Low Voltage Supplies**

Multi-output DC-DC Converters from Intersil



### **EPCOS** and Continental Temic announce automotive collaboration



EPCOS and Continental Temic have agreed to work closely together in the devel-

opment of components for power electronics in hybrid vehicles. In the Electronic Powertrain Controller (EPC) Project, Continental Temic is using capacitors based on EPCOS' innovative stacked winding technology to produce extremely compact and efficient converters for automotive power trains.

The extremely light and space-saving design of EPCOS power capacitors enables the realisation of ultracompact designs in automotive electronics. Rated at 2000  $\mu$ F, the power capacitors have a dielectric strength of 450 V DC. Thanks to their space-saving

stacked winding technology, they measure only 292 x 146 x 56 mm. At an operating frequency of 8 kHz, a current up to 150A RMS can be applied to the capacitor.

In turn, the very low-inductance capacitors optimise converter design because only low voltage peaks, for example, can occur. Further advantages of the capacitors include their oil-free design and self-healing capability. Wide operating temperature range extends from -40 to +105 °C.

www.epcos.com

#### **UK Partner for Advanced Power Conversion**

Advanced Power Conversion PLC of Farnborough, England announces the appointment of Gresham Power Electronics as their latest Sales Channel Partner. Gresham will be able to offer the complete range of APC's ultra-high efficiency full brick DC-DC converters, AC-DC power supplies, DC-DC bulk power supply, Configurable Multi-slot SMPS, Value Added and Complete Custom Power Solutions through their established sales network.

Gresham has been in the power conversion business and distribution for some 50 years and specialises in "off the shelf custom" power supplies and has it's own ISO certified manufacturing facility in Salisbury. It has a great deal of experience of supplying non-standard solutions at commercial-off-theshelf (COTS) prices.

"We believe that Gresham's strength in industrial markets will bring major benefits to a much broader range of end users" says Tim Worley, CEO of APC "their long history and great experience will really add to our sales channels".

Jake Moir, Managing Director of Gresham comments, "the wide range and flexibility of APC's products are a great fit alongside our existing highly configurable power supplies. Our sales and engineering teams will readily



be able to exploit APC's unique features to help our customers"

www.apcuk.com

www.greshampower.com

#### **Intersil acquires Xicor**

Intersil Corporation (Nasdaq:ISIL - News) and Xicor, Inc. (Nasdaq:XICO - News) today announced the signing of a definitive agreement for Intersil to acquire Xicor. With this acquisition, Intersil, a world leader in the design and manufacture of high performance analog solutions, significantly expands its portfolio of high growth, standard analog products. Under the terms of the agreement, each Xicor shareholder will receive the value of \$8.00 per share in cash and 0.335 a share of Intersil common stock (equivalent to \$15.58 per share of Xicor stock, based on the closing price of Intersil stock on March 12, 2004). Each Xicor shareholder may elect to receive all cash, stock, or a combination of cash and stock, subject to proration based on the total cash and shares available in the merger. This reflects an aggregate purchase price of approximately \$529 million.

The transaction combines two strong high performance analog companies and significantly strengthens Intersil's portfolio of general purpose standard analog solutions. Xicor is a leader in digital potentiometers and system management products that complement Intersil's current standard analog portfolio. Xicor also has a rapidly expanding portfolio of real time clocks, voltage references, power sequencing and display products that provide a natural extension to Intersil's leadership position in the computing power management and flat panel display markets. This will be the second analog acquisition for Intersil, which acquired Elantec Semiconductor, Inc. in May

> www.xicor.com www.intersil.com

#### Power Events

- PCIM China, March 17-19, Shangai, China
- Electronica USA, Power Electronics Conf.
- March 29-April 1, San Francisco
- Hanover Industrial Fair, April 19-24,
- Hanover, Germany

• Semicon Europe, April 20-22, Münich,

agement Germany

- PCIM 2004, May 25-27, Nüremberg, Germany
- Fisita 2004, May 23-27, Barcelona, Spain

Barrage Sales Offices France 33-1-41.070565; Baly 39-02-3603050; Berning, 47-80-062450; Swelen 46-8-622-600; Bieled Gapter 44-0226-477056; Finland: 255-0-86733690 Distributors Anthelic Scanar 01-2-0741-0122; Belgium ALM, rvtrahle 32-0-2-7202055; Finland: CV Finlowick AB: 268-9-867231; France: Annue Electronique 53-3: 33-1-40 78-40 78: Teladic Antonic: 33-1-40220425; Bernarg toxight CMEH-40-80-812080;



### 90% Efficient PoE



#### Fast Time-to-Market with Linear's Proven Power Over Ethernet Solutions

Linear Technology's growing portfolio of flyback and forward DC/DC converters provide high efficiency, minimal thermal de-rating and design simplicity – ideal for Power over Ethernet (PoE) isolated supply requirements. The LT1725 delivers 3.3V at 3.5A with 90% efficiency from a 48V input at a cost that module alternatives can't match. See the table below for a selection of our PoE product family and our web site for our complete offering.

#### Powered Ethernet Solutions DC/DC Converters Insisted Efficient Yes/No LT*1725 No Optocespler Fleback 90% TC*3863 ThirdSUT** Floback Yes/No 82% Synchronous Ryback No. 97% TCHER IEEE 802" Jal Power Interface Controllers PO/PSE Channelly 104257 Orboard 100V, 400mA MOSFET ₹D. **Onboard 100V MOSPET** LTCASED 1 ₽D ÷. Deal Current Limit Jusci Controller with LTC-USE INSE 4 C Disconteact Quad Controller with DD & AD Disconnect 120 TEASTER 4

#### Actual Size Demo Circuit



#### VInfo & Online Store

#### www.linear.com

Literature: 1-800-4-LINEAR Support: 408-432-1900



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### Does Digital Controlled Power Supplies Become the Future?

#### Signal connections are effectively serving supply

DC/DC conversion and the appropriate point of load (POL) supply in all kind of power classes has a step into digital controlled Power Supply solutions. Supply Manufacturers have to approach the semiconductor design level to get efficient results.

By Bodo Arlt, Power Systems Design Europe Editor-in-Chief

Power supply technology has developed from linearly controlled power supplies to the switching power supplies used almost exclusively today. Most of the semiconductor manufactures offer reference designs and multi-phase solutions to power the computer demands. That helps to speed up the design at the motherboard manufacturer in Asia and helps standard converters to improve.

Digital control at the distributed power supply architecture as shown recently by Power One at APEC (Applied Power Electronics Conference and Exposition) in Anaheim can lead us to future level of power supply technology. Achieving control and fine tuning in the manufacturing process to supply a number of loads with even lower and fine adjusted voltages by point of load supplies is a challenge to be done digital to have easy control of fine adjustment. That is achieved by going from the system level power supply manufacture to a semiconductor defining situation to achieve the end product.

Now we are looking to a range of power supplies in DC/DC conversion of all levels. Here we have a wide map of demands for applications in all power classes. To understand the common subjects, I like to start the view from device level understanding and materials to have a solid platform for choosing the right elements and components to systems.

Modern designs minimise losses in systems, starting on the device level. Minimising switching loss and conduction loss is the way to success. Eliminating unnecessary thermal resistance in the heat extraction pass is the trick besides improvement in silicon. Better magnetics and higher switching frequency gives more compact designs. Current technology advances with trench-gate components are bringing significant advantages thanks to the improved conduction characteristic in low-voltage applications with MOSFETs. The MOSFET is making its main contribution in the DC/DC converter, which in combination with optimised passive components demonstrates over 90 percent efficiency.

In the area of DC/DC conversion the manufacturing companies form alliances in standardisation of footprints for the brick converter class. It is important that second source and full electrical compatibility is given to serve the customers need.

The pin-out is a big challenge to do it right. Just now, SynQor and Tyco have formed an alliance having converters being compatible with the rest of pin-out in industry and having the extra pins for more current to be like "twist a pair" having alternated the output voltages at the extra pins to compensate electrical fields that effect peak current behaviour.

Still, synchronous rectification with suitable MOSFETs and necessary control is of crucial importance. The supply voltages demanded by modern IC technology cover an increasing range with the tendency for controller ICs at ever lower voltage. These systems can be only optimally configured with distributed power technology. Point of load (POL) supply is one of the very critical steps in board level supply where bus voltages go down with IC voltage needs. Package technologies such as the Thin Flat Package (TFP) that offers volume reductions over previous TO-220SM packages helps without compromising performance. This is achieved in part by the fact that the TFP is driven by four pins representing gate, drive source, main current source and drain. The bottomless packages has a dramatic reduction in package resistance and secondly provides an improvement in thermal performance by improving the thermal conductivity between the die and the PCB. This eliminates parasitic conductance and improves noise immunity during driving, making it possible for high switching speeds to be achieved. A very important point in DC/DC converter design to achieve more dense systems by having smaller coils and magnetics operating at higher frequency.

Listening to Don Burke, former director of discrete device engineering at Harris, and my former boss are perfect to fill in here. Power Design is a matter of seeing how hard one can push the silicon, rather than a myriad of mask designs of a standard process, so the processing and design experiments go hand in hand, the process is never a fixed one. So people who are making ICs may have difficulty in producing good power switches. We need to keep that in mind if we look towards monolithic products doing the full conversion. The switch will be seen still as an extra element beside the driver and control ICs.

We see an area of monolithic power supply solutions that has been developed from the new generation of products that are playing around in the hand-held arena. They all need power from batteries. They may require an external MOSFET as explained above.Most of the portables have rechargeable batteries. Talking recently to Dave Bell, president of Linear Technology about the way powering from given sources like connections over the Ethernet link or what ever becomes available like the DC power outlet in the car or boat. By that the amount of wall outlets can be significant reduced by using power over Ethernet. So we save standby power. Anyone of us has at least half a dozen wall outlet power supplies around his working desk.

The introduction of modern micro-controller and DSPs has influenced requirements regarding the electromagnetic effects from intelligent switching and compliance with legal standards. This is the domain of MOS-controlled components mainly the MOSFETs as well as of the IGBT. The gate drive conditions for dv/dt are the fine tuning to stay within the limits the legal standards require. The goal is not to generate EMI and avoid therefore tough shielding of your unit. The designers need to follow the advise the EMI labs and consultants offer before hand rather than to try to fix it in the approval process. World-wide legal standards require the attention at the manufactories and the user side.

Also not to overlook the passive components, they also play an important role in the power supply. Lifetime of capacitors are critical to create a reliable supply over time. Resistors are much more stable from their physics than capacitors. Coils and magnetics operating at high frequency are the absolute complementary parts to have the design optimised to best efficiency. From a total point of view ventilation is crucial to get the heat out. Mechanical ventilators have a lifetime based on their ball baring. All these are points to decide on when you are going to built or to purchase a power supply. Modern computer technology with the capability to perform complex simulation programs gives the designer a decisive time advantage.

Thus with good components available it is still most important to simulate the thermal requirements, improving reliability and system lifetime of today's power supply converter generation. One thing is certain, the portable electronics age with all of is power feeding and back up cannot endure without power and it is therefore vital to understand how power is generated and distributed including the usage of signal connections like the Ethernet link.

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### **The Long Way from Electric to Hybrid** to Electric to...

By Uwe Knorr, Vice President Sales Ansoft Corp.

ver the last few years we could see a variety of activities related to hybrid power for our mobile life style. Driven by environmental concerns governments and agencies sponsored numerous programs supporting the development of electric and hybridelectric vehicles. Primary driver is the desire to lower fuel consumption and consequently lower emissions. After working for a number of years with a variety of automotive manufacturers on their hybrid electric programs I can say that there have been remarkable results on this way und at the same time I can see a remarkable number of stumbling stones ahead.

After the euphoria about fuel cell technology and its potential applications in electric vehicles reality has taken its toll. Fuel cells still weigh too much and their use in mobile applications is limited to larger vehicles where the loss in space and gain in weight is not as dramatic as in passenger cars. Although there are a number of promising developments, such as micro fuel cells, most of the devices are still too big. Another-still unsolved—problem is the hydrogen storage and fueling problem. Refractors that generate hydrogen from gasoline add additional equipment to the vehicle and consequently further reduce the available space. Hydrogen tanks present a safety issue, not to mention the existing fuel station infrastructure that would be developed. And by the waywhere does the hydrogen come from? As far as I know the problem of core fusion is still far away from being solved and solar power driven electrolysers will

probably not be able to able to provide sufficient power to supply the whole earth's fleet of vehicles.

However there is a lot of activity in industry and research to overcome these obstacles. General Motors, Toyota and other companies heavily invested in their fuel cell activities and begin to derive first results from these programs -even if they are not necessarily commercially available fuel cell vehicles yet. The most promising current application is stationary power systems for industrial and residential use in critical or remote applications. The good news however is that power electronics and drive technology have significantly advanced during this process. This progress was primarily driven by weight, size and safety constraints, thermal and extremely high efficiency requirements. Design engineers deployed numerous innovations in the areas of power semiconductors, burst power with ultracapacitors, electrical machines, magnetic components and controls in order to meet these challenges. Meanwhile the second generation of transportation inverter technology is much smaller and way more efficient in their use of the ever limited onboard electrical power. At Ansoft we were able to deliver the tools needed to design these systems efficiently and enable virtual prototyping of complete electrical drive trains. Many of the automotive and aerospace manufacturers and suppliers working in this field are successfully using our EM design environment for the analysis and optimization of electrical machines, inverters or complete systems.

The unique combination of electrical and electromagnetic simulation algorithms with non-electrical domains such as mechanics, hydraulics and

controls helps

streamlining the design process within a single design environment.

Ironically currently a number of automotive manufacturers make use of these great advancements in electric drive trains in a way that is especially by environmental groups considered not very consistent with the original idea of clean vehicles powered by electrical energy. There are a number of projects going on to give SUV's (sport utility vehicles)the enfant terrible of the automotive community—an additional acceleration burst in demanding situations. Hybrid SUV's can add the high and guickly available torque to the motor torque during the acceleration phase which will ultimately reduce the fuel consumption of the vehicles but probably not to a degree that would be considered significant by environmental groups. The technology is promising and the legal and social pressures are in place. It will be an exciting journey on the way to cleaner, electrically powered vehicles and I feel luck to be able to take part in it. I'll keep you posted...



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### Controlling and Protecting Door-Opening Systems

#### Open-loop hall effect based technology

Door opening systems must provide safety and protection for users. Imagine the consequences of a garage door closing itself on a person or a vehicle. Current measurement can provide this protection.

lectrical opening systems for garage doors, gates, shutters or awnings are becoming more and more common in day-to-day life, and protection is an important function that must be taken into account during their design. This protection can be provided by current measurement.

The DC brush motor used for garage door openers, electrical gates, awnings or shutters has its own repeatable current profile during normal opening or closing. This profile can be stored in a microcontroller. A current transducer provides the information on the current drawn by the DC motor against time, and this is compared to the profile stored in the microcontroller, allowing a tolerance defined by the manufacturer of the opening system. If it doesn't match, there is a problem. The microcontroller can then give an alarm, switch off the system or reverse the drive. This offers protection for the obstacle, human or otherwise, and also protects the motor from the effects of drawing too high a current.

The protection requirement is to detect that a person or an object is located in

#### By Stéphane Rollier, LEM

the path of the doors, gates, shutters or awnings, preventing correct closing or opening. This can be achieved by monitoring the current consumed by the motor that powers the movement. The space available for electronics in these applications is often very limited, so it is important to use a compact current transducer, such as LEM's HTS 10 with its a 17x19 mm footprint. The accuracy is not the most important parameter in this type of application. The aim is not to control and regulate the motor but to ensure protection by detection. The current transducer is used to detect whether the motor is drawing too high a current at a given instant, for example when a door runs into an obstacle. In such applications the HTS operates as a replacement for mechanical limit switches.

If pumps become jammed, the motors coupled to these pumps consume more current. The HTS can be used to detect the presence of these overcurrents and to switch off the installation and/or switch on back-up motors and pumps. A similar function is provided for crushers and grinders.



When motor rotors become locked, current transducers offer a safety benefit, with an early warning of the defect. This can also prevent motor damage.

In lighting applications, the integration of such a transducer offers current overload detection at the level of the ballast for its protection. The transducer output is coupled with an electronic circuit that manages the warning levels or triggers a circuit breaker.

Other applications for the HTS include electrically powered seats and overload protection for low cost drives such as electrical and household appliances, including washing machines.



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The HTS 10 provides bipolar current measurements when it is powered by a single +5V supply. It is ratiometric, which means that its sensitivity and offset vary in direct proportion to the power supply. This ratiometric output and single +5V supply make it particularly suitable for use with ratiometric microcontrollers. Microcontrollers are often used in control and protection circuits and the ratiometric output of the transducer allows the microcontroller to work with a lowcost current sensor while removing the impact of power supply variations on output accuracy. A ratiometric microcontroller operating from the same power supply as the transducer can offer 8-bit analogue to digital conversion of the transducer signal. This allows the use of a +5V power supply with a ±10% tolerance for the different devices and the use of a ratiometric current sensor.

This tolerance, as well as the tolerance on the sensitivity and on the initial offset, has an influence on the measuring range. Let's take an example:



With a power supply of  $+5V \pm 0\%$  (it is really 0% in this example), a gain tolerance of ±30% and an offset tolerance of ±12%, the HTS 10-P model can have a maximum initial offset of 2.8V, with a maximum sensitivity of 130mV/A at +25°C.

In these conditions, the sensor provides a measuring range of +13A to -17A. The full scale output is limited at Vdd-0.5V (= 4.5V) for the positive side and Vss+0.5V (= +0.5V) for the negative side.



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Figure 1. Curve for the Linearity

Positive measuring range : (+4.5V-initial offset)/sensitivity = (4.5V-2.8V)/0.13 = +13Apk.

Negative measuring range : (+0.5Vinitial offset)/sensitivity = (+0.5V-2.8V)/0.13 = -17.7 Apk.

The HTS 10-P/SP1 model with better sensitivity and offset tolerance (±20% and ±3% respectively) offers measurements with less fluctuation (thermal drift values are also improved). When the sensor is used with a microcontroller. the device can be calibrated for the application, so that the tolerances can

easily be cancelled or adjusted so that they do not affect the accuracy calculation, ensuring repeatable results. Only linearity errors need then be taken into account.

The HTS 10-P and HTS 10-P/SP1 are specified for 10ARMS nominal (15Apk) measurement and provide a maximum linearity of 1% at +25°C, which suits the detection requirements for these types of applications. The 1% figure is the max linearity error including the hysteresis offset voltage after an excursion to 1 x lp, and is a repeatable value.



Figure 2. Curve for the Bandwidth

The product has been designed for PCB applications, with pins for both primary and secondary connections. However, two methods can be used to connect the primary conductor:

When a track on a PCB represents the primary conductor to measure, the two sensor pins of the HTS sensor can be soldered into that track. These two pins are connected to an internal winding of three turns around the magnetic circuit. In these conditions of use, a permanent nominal primary current of 10 Arms (30 Amperes.turns) can be measured, with peak value up to 15 A (45 Amperes.turns). With this layout, it is necessary to break into the primary conductor.

If a non-contact measurement is needed, without breaking into the primary conductor, the transducer's aperture can be used. This offers a possible nominal current measurement of 30 Arms and 45 Apk when the conductor is passed through the aperture once. In this condition of use, the sensor can be used for different current ranges by changing the number of times the primary conductor passes through the aperture. For example, 10 Arms can be measured with three turns in the aperture, or 6 Arms with five turns. To achieve the same sensitivity at the output as that produced by the internal winding, the goal is to have in all cases 30 Arms.turns generated, whatever the number of turns through the aperture. The transducer should still be mounted and soldered onto the PCB to make the other connections, such as power supply and voltage output.

Based on open-loop Hall effect technology and using an ASIC (Application Specific Integrated Circuit), the HTS transducers provide current measurement from DC up to 16kHz (-3dB as signal attenuation) and up to 10kHz (-1dB).

The HTS also has the advantage over current transformers that it can measure currents that have some DC components in addition to the AC signal.

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### **Advanced Packaging Boosts Power MOSFET** Performance

#### *Higher processor frequencies need faster* response from POL Converters.

Each of the advanced technologies discussed will frequently allow a single-MOSFET to replace two or more traditional MOSFETs in parallel. As well as the potential to reduce cost and component count, a single MOSFET solution also displays greater immunity to circuit stray impedance and device variations.

#### Jason Zhang, International Rectifier

he typical current consumption of ICs such as microprocessors and FPGAs is increasing exponentially, as rapidly shrinking process geometries allow greater functional density while also calling for lower operating voltage. This is challenging power systems design, driving improvements in power devices and also stimulating new architectures based on point of load converters. In fact, power MOSFET silicon has improved to the extent that packaging technology has become the main focus for further gains. The latest packages now entering the market target the established SO-8 footprint but solve the drawbacks associated with the traditional SO-8 package. But there are many options, including CopperStrap SO-8, PowerPak and DirectFET, as well as integrated modules such as iPOWIR. But this abundance of choice can be confusing, especially to an embedded power supply designer who has neither

the time nor the resources to experiment with numerous unfamiliar devices. This article examines popular next generation MOSFET packages, to develop a design guide for creating embedded converters. The small size and low profile of SO-8 have made it a popular power MOSFET package as power density demands have increased steadily. When SO-8 first arrived, its electrical and thermal performance was acceptable compared to contemporary system demands and MOSFET silicon performance. But now that the R(DS)ON of MOSFET silicon is falling to sub-m_ohm levels, the SO-8's wire bonded construction is holding back further progress. In particular, there are four key limitations that emerging packaging technologies must address:

Traditional, 0.05mm-width gold bond wires are preventing die to package resistance falling below 1m ohm.



This represents more than 50% of total MOSFET RDS(on) for the latest devices. Junction-to-PCB thermal impedance (R thj-pcb) is high, because the MOSFET drain is connected to the lead-frame, which is then molded in plastic. The drain leads are therefore the main thermal path to the PCB for heat generated at the junction. The source connection has an even higher thermal resistance path to the PCB. Junction-tocase (top) thermal impedance (Rthjcase top) is also poor, resulting from the low thermal conductivity of the plastic over-molding. The SO-8 leadframe and internal wirebonds introduce parasitic inductance on the gate, source and drain terminals that slow down the switching speed of the MOSFET. Good switching response is increasingly important, as higher processor frequencies demand much shorter response times from POL converters.



Figure 1. Package performance improvement over SO-8 to some extent by addressing part or all of the four major limitations of standard SO-8.

Several enhanced packages are shown in Figure 1. Each improves the package performance over SO-8 to some extent by addressing part or all of the four major limitations of standard SO-8.

#### **CopperStrap Enhances Thermal** Performance

CopperStrap SO-8 was the first significant enhancement to the original wirebonded SO-8 package. The wirebonds connecting the source to the leadframe are replaced with a solid copper strap that covers the surface of the die (source), as shown in figure 1b. This reduces the die to source (leads) electrical resistance from 1 m_ohm to 0.4 m_ohm. It also provides a better thermal path from the die to the leadframe.

CopperStrap SO-8 is now so widely adopted by low RDS(ON) MOSFETs that it is commonly accepted as the standard SO-8 technology. The technology is also branded as PowerConnect.

But although CopperStrap has delivered great improvements in electrical performance, the other important limitations of SO-8 remain; namely, high Rthj-pcb and Rthj-case top, and high source inductance.

#### **PowerPak**

The next natural package evolution is to improve the thermal contact between the die and the PCB, while retaining the electrical improvements achieved through CopperStrap. Good thermal performance is desirable from a reliability standpoint, since every 10 °C reduc-

tion in junction temperature (Tj) delivers a twofold increase in MTBF.

One solution is PowerPak, as shown in figure 1c. This removes the molding compound below the lead frame to bring the metal of the lead frame into direct contact with the PCB. The lower surface of the lead frame becomes a large drain that provides a much greater area of contact to conduct heat away from the die. This is soldered to the PCB. Removing the molding compound below the lead frame also results in a lower profile device. PowerPak retains the SO-8 footprint, but its thickness measures around 1mm. Other packages, such as MLP, LFPAK, SuperSO8, WPAK, PowerFlat and Bottomless SO-8, use similar construction to achieve comparable thermal performance.

	Package Resistance (MΩ)	Source Inductance (nH)	Rth junction_pcb mounted (°C/W)	Rth junction_case top (°C/W)	
SO-8	1.6	1.5	11	18	
CopperStrap	1	0.8	10	15	
PowerPak	0.8	0.8	3	10	
DirectFET	0.15	<0.1	1	1.4	

Table 1. Critical MOSFET package parameters.

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Figure 2. Dual Channel iPOWIR device (iP1202), 15A per channel or up to 30A combined output

PowerPak significantly reduces Rthjpcb, which allows efficient heat transfer to the motherboard. But current (I) demands are continuously increasing, leading to risk of thermal saturation of the motherboard. As a result, there is now a trend toward top-side cooling through a heatsink, in preference to dumping heat into the motherboard.

#### **DirectFET Technology**

International Rectifier's new DirectFET packaging technology uses a MOSFET die with top-layer metal configuration in conjunction with a proprietary passivation system, to create large-area gate and source contacts on the surface of the die. The die is then flipped, bringing the terminals into direct contact with the PCB. A copper "can" is then used to bring the drain connection from the back of the silicon die onto the PCB. The cross section is shown in figure 1d. In this way, DirectFET eliminates not only the conventional lead frame and wirebonds that lead to high package resistance, but also eliminates the plastic packaging that restricts thermal performance of most SMT packages. As such, it virtually removes all four limitations of

SO-8 at once. This configuration maximizes contact area between the source and gate pads and the PCB for best electrical and thermal efficiency. The copper can drain connection also provides an alternate path for heat dissipation and provides a very efficient thermal interface to an external heatsink.

There is virtually no source inductance in DirectFET. And the large gate and source terminals also allow driver circuitry to be connected without including any PCB stray inductance, known as the common source inductance, in the high current path. This results in exceptionally good high frequency switching performance.

In-circuit results show that one DirectFET, without topside cooling, can easily replace two SO-8 in parallel, and sometimes two PowerPAKs in parallel. With a heatsink attached to its can, DirectFET makes paralleling MOSFET less necessary.

DirectFET puts packaging performance back ahead of silicon, which is once again the limiting factor in further MOSFET performance improvement. Table 1 compares the package thermal and electrical performance for the technologies covered in this article.

#### Solutions for Integrated Converters

Alongside the improvements to package and silicon technology necessary to meet modern current demands, power semiconductors must also reduce the design effort involved in building an embedded POL converter. This is highly important, as stringent electrical and thermal performance are now making board layout and component selection so critical that any oversight can create reliability problems. The testability of embedded power supplies is limited to dc parameters only, and also contributes to additional reliability concerns. IPOWIR modules simplify the design of high current power supplies, particularly in relation to board layout, by tightly integrating the power silicon with all critical active and passive components. Only minimal external components are required. An iPOWIR implementation can be tested as a complete power supply in production so that all cumulative dc and ac effects are captured. Reliability levels

match those of full functional power supply modules at lower cost.

Figure 2 shows a dual channel iPOWIR device (iP1202) that outputs up to 15A per channel or up to 30A as a combined output (2-phase solution).

#### Package Selection Guidelines

When building an embedded converter, designers will naturally target the lowest cost components that meet elec trical and thermal requirements. But they can no longer assume that the established SO-8 devices will result in the lowest cost solution overall. For instance, the large package resistance and higher junction temperature (Tj), which can only be compensated by a larger die size, prevent SO-8 devices from exploiting the latest die shrinks to realize ongoing cost savings. In comparison, the DirectFET MOSFET can either reduce component count or reduce power loss to the extent that system level designs are less expensive than many SO-8 implementations.

In fact, each of the advanced technologies discussed will frequently allow a single-MOSFET to replace two or more traditional MOSFETs in parallel. As well as the potential to reduce cost and component count, a single MOS-FET solution also displays greater immunity to circuit stray impedance and device variations.

Multi-phase solutions generally provide lower output voltage ripple and better transient response than a singlephase design. However, extra phases are not necessarily the best approach when resolving thermal or efficiency problems. Using better packages and keeping the number of phases at around two can usually provide the most cost effective solution.

Whenever top-side cooling options are available, the DirectFET package should always be considered first. Adding a heatsink is usually cheaper than adding more MOSFET devices or more phases in parallel.

#### Conclusion

The traditional SO-8 package has served power designers well. But advanced packages such as PowerPak and DirectFET now not only offer greater performance and reliability but also make an increasingly persuasive cost argument. By understanding the relative merits of each of the main emerging technologies, designers can make an informed decision to achieve an optimal solution. When design ease and time to market dominate the designer's objectives, highly integrated solutions such as the iPOWIR series deliver strong performance at a competitive cost.



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### Defining an Intellient Pin-Out for High Amperage

#### Advancing the power curve for DC/DC Converters

As the power voltage for digital circuits falls to the 1.0-1.5V range, and as the power consumed on a load board increases, dc/dc converter modules are being asked to deliver very high output currents. The discussed high amperage half-brick and quarter-brick converters feature an alternative pin-out solution that offers significant performance advantages.

ive years ago a half-brick converter could deliver only 30A, today's highest amperage half-brick converters deliver 100A. Similarly, 5 years ago guarter-brick converters delivered 15A; now they can deliver 60A. To handle this very high level of current, the number of output power pins needs to be doubled. The question remains: where should the extra pins be located? Ideally, the chosen locations should be both optimal for the user and a standard for the converter industry. Unfortunately, several manufacturers have already released products with incompatible extra pin locations. It is therefore up to the consumers to decide which pin location will become the new standard. The purpose of this article is to provide some technical guidance for this decision.

#### Why do I need to double the power pins?

First, it is important to understand that the need to double the number of power pins is not due to the pin's electrical

#### By Dr. Martin Schlecht, SynQor





resistance. An 80 mil diameter copper pin has a resistance of about 20µohm. When this pin carries 100A, its power dissipation is 0.2W. Since the 100A flows out of the V+ pin and back into the Return (or Ground) pin, a total of 0.4W is lost. By doubling the number of power pins, a savings of only 0.2W is realized. To put this in perspective, a 1.2Vout, 100A converter operating at 83% efficiency dissipates about 25W. Instead, the reason to double the power pins is to reduce the dissipation that occurs on the load board as the output current spreads outward from the pin in the board's power plane. To understand this point, consider a load board that is 12 inches on a side. Assume that the board has four loads, each drawing 25A of current, distributed around the board as shown in Figure 1, and that a 100A halfbrick converter is mounted near one edge of the board. Further assume that the power plane connecting the converter to the loads is made from 1 oz. Copper and has a resistance per square of 1mohm (which takes into account the many vias that generally interrupt it).

#### Measuring the Voltage Drop

Figure 2 shows the voltage profile across the power plane when only one power pin is used for each terminal of the converter. Note that in this figure, the converter's pin is the V+ pin (current is flowing out of it), but the nominal dc voltage at this pin (e.g. 1.2V) has been removed from the scale so that we can focus entirely on the voltage drop from the pin to the load. Note also that the simulation includes thermal relief spokes around the pin, although they cannot be seen at this scale. From this simulation we can see an 80 mV drop at a distance of about 6 inches from the pin. This large drop occurs because the current has to first spread out from a small point (the pin) before it can take full advantage of the width of the power plane. The resistance of this "spreading" region is high.

At 100A, the 80 mV results in 8W of dissipation, and that number is again doubled when you take into account the dissipation caused when the current returns to the converter at the Return pin. Both the 16W of dissipation,

and the 160mV of voltage drop (13.3% of 1.2V), are too large. Now consider the voltage profile of Figure 3. in which a second power pin has been added for the V+ terminal. The location of this pin is 0.2 inches inside of (and inline with) the original pin (see Fig. 5a). (Note that with the scale of Figure 3 it is not possible to discern the second pin from the first.) This adjacent pin location may be convenient for the layout of the converter, but it does verv little to correct the problem for the user. The voltage drop at a comparable point 6 inches away from the converter is about 10mV less than the case where only one terminal pin is used. The total power savings is therefore only 2W out of the 16W.

The reason for this marginal improvement can be understood by examining how the current spreads out from the pin. As the simulations show, it takes several inches for the current to spread out enough to take advantage of the width of the power plane. But since the two pins are located only 0.2 inches apart (see Figure 5a). their currents quickly overlap, and it is as though there were just one pin. The advantage of having two pins is limited to the region immediately surrounding the pins, and that region contributes only a small part of the total spreading resistance. However, now look what happens when the extra pin is located on the other side of the half-brick converter. 0.2 inches outside of (and inline with) the pin of the opposite polarity as in the SynQor converter (see Figure 5b). As the voltage profile in Figure 4 shows, the voltage drop at a comparable point 6 inches away from the converter is about 40 mV lower than the case where only one





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Figure 2: The voltage profile across the V+ power plane for the case where the converter has only one pin for each terminal. (The nominal dc voltage has been removed from the scale.



Figure 3: The voltage profile across the V+ power plane for the case where the converter has two pins for each terminal located adjacent to each other. (The nominal dc voltage has been removed from the scale.)

terminal pin is used. The total power savings in this case is 8W out of the 16W This substantial improvement occurs because the two pins, in this case, are 1.6 inches apart instead of 0.2 inches. As such, the current from each pin nearly finishes its spreading before it overlaps with the other current, and the effective spreading resistance is nearly cut in half due to the two parallel paths. Clearly, the extra pin location shown in Figure 5b is superior to the location shown in Figure 5a from the users point of view. A similar statement can be made for the preferred location of the extra pins on a quarter-brick converter.

Figure 6 shows this approach where the extra pins are located 0.15 inches outside of (and inline with) the original pins, with opposite terminals adjacent to each other. Although the distance between the two pins of a given terminal is now only 0.75 inches for this smaller converter, much of the spreading still occurs before the two currents overlap, and the design is therefore superior to one in which the two pins of a given terminal are adjacent and only 0.15 inches or less apart.

As a final point, the preferred extra pin locations shown in Figures 5b and 6 do more than simply reduce power dissipation in the load board. Some of the heat that a converter creates travels down the pins and spreads out onto the load board. How much heat flows this way depends on how hot the load board is from other sources of dissipation. In our half-brick example above, we saw that the power dissipated in the power plane in the vicinity of the converter was reduced by 8Watt by using the preferred pin locations. This reduction makes the load board in the region of the converter that much cooler, and allows more heat to flow down the pins from the converter. This results in a cooler and therefore more reliable converter.



Figure 4: The voltage profile across the V+ power plane for the SynQor solution where the converter has only two pins for each terminal located on opposite sides of the converter. (The nominal dc voltage has been removed from the scale.)



Figure 5a: Extra pin location where the same terminal pins are located adjacent to each other.





Design engineers have much at stake with any new standards that are adopted in the industry. Their voice should be heard as to which pin-out design provides the best overall solution. Since no relevant standards body exits for DC/DC converters, any decision on standardization for the high current brick pin-out will likely be left up to market forces. The user will chose intelligently for the most efficient design to set the standards.

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Figure 5b: SynQor extra pin location where same terminal pins are located on opposite sides of the converter.

Figure 6: The preferred location of the extra pins for a high amperage quarter-brick.

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Dr. Volker Demuth, Dr. Karlheinz Häupl, Dr. Bernhard König, Dr. Arendt Wintrich; Semikron

oday higher power density is in continued demand in power conversion and power distribution technology. Representative for this trend is the IGBT concepts with Trench gate components and the field-stop design. Both concepts provide reduced on-state losses compared to previous non-punch-through (NPT) devices. However, to benefit from this technological step IGBT modules have to include optimal freewheeling diodes to complement the IGBT and to guarantee the overall device performance.

The major demands for freewheeling diodes are a low forward voltage drop, a small recovered charge and a soft switching behavior over a large range of temperatures and currents. Other decisive demands are the ability for paralleling the diode to cover high current applications and a high dynamical ruggedness to prevent destruction of the device during short circuiting.

Our approach uses an innovative design of the well-established controlled



axial lifetime (CAL) technology to reduce the on-state voltage drop. Two key targets were essential to the development of the CAL HD: increase of usable current per chip area and enhanced dynamic performance.

The CAL HD diode is a planar device with a deep n+ cathode zone and p+ doped guard rings as junction termination. The junction termination is optimized with respect to 1700V blocking voltage. The carrier lifetime is controlled by electron irradiation and He2+-ion implant, resulting in an inhomogeneous

defect profile shown schematically in Figure 1. In combination with the anode and cathode diffusion profiles a low recovery peak current and the soft switching behavior of the CAL HD diode is obtained.



Figure 1: Vertical defect density profile of the CAL HD diode produced by electron irradiation and He2+-ion implantation.

The results of our approach are shown using the 75A CAL HD with a chip area of 61 mm2 as representative for the 1700V HD product portfolio. Figure 2 exhibits the on-state characteristic at room temperature (RT) and 125°C.



### looking for solutions...



ELECTRIC



1200 V 10A - 50A

1400 V 35A & 50A

600 V 15A - 30A

1200 V 15A & 25A



75A - 100A

1400 V 75A & 100A

1200 V 50A & 75A

1200 V 75A - 150A

1400 V 75A & 100A

1200 V 75A & 100A

600 V 30A & 50A

Germany

1200 V 10A - 35A

1400 V 10A - 25A



600 V 50A & 100A

1200 V 35A - 75A

1400 V 35A & 50A

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Figure 2: On-state characteristic of the 75 Ampere CAL HD diode (area = 61 mm2) at room temperature (RT) and at 125 °C.

The first eminent feature is the positive temperature coefficient dU/dT at rated current, leading to a balanced current sharing in parallel operation. This allows advanced paralleling of CAL HD diodes in high current devices. The second feature is the distinctly increased current density: in comparison to the standard 61 mm2 1700V CAL diode which is rated at 50A, the CAL HD exhibits a 50% higher current. Benefiting from the increased current density, the surge forward current IFSM could be pushed 14% beyond the value of a standard CAL diode.

The successful adaptation of the CAL HD to Trench IGBT's is proved in Figure 3, by comparing the recovery behavior of the diode when switched with Trench (3a) and with NPT IGBT (3b) under identical conditions. If switched with the Trench IGBT, the initial current drops to a peak reverse recovery current of  $I_{RRM}$  = 55 A. The soft switching behavior is reflected in a gradual reduction of the recovery current into a tail phase. In contrast to that, switching the CAL HD by a conventional NPT-IGBT leads to higher dynamical losses: at similar dl/dt the voltage rises three times faster with the NPT-IGBT (dU/dt=2450 V/µs) as compared to the Trench-IGBT (dU/dt=800 V/µs). The softness of the diode is also improved by using the Trench IGBT: when commutated with the Trench IGBT a smooth tail current is observed leading to 60% larger soft factor  $S=(t_2-t_1)/(t_1-t_0)$  compared to switching with the NPT-IGB





Figure 3: Diode current and voltage waveforms using a Trench- (a) and NPT-IGBT (b) as switches.

The ability of the CAL HD to provide low dynamic losses over a wide range of commutation rates dl/dt is shown in Figure 4. The graph demonstrates the reverse recovery charge Q_{rr}, I_{rm} and the energy dissipation E_{rec}. The solid lines illustrate the results of the Trench IGBT; the dashed lines mark the NPT-IGBT. In the typical operative range of the Trench-IGBT at ~1000 A/µs, the combination Trench IGBT / CAL HD shows 27% smaller switching losses as compared to operation of NPT-IGBT



Figure 4: Dynamical data of the CAL HD diode as a function of commutation speed. Switched with Trench (solid lines) and NPT-IGBT (broken lines).

with CAL HD. At higher frequencies the dynamical losses of the combination trench IGBT / CAL HD pick up and at dI/dt>3000 A/µs the switching losses for both IGBT's nearly coincide. Due to the integrated gate resistance the switching speed of the Trench-IGBT is limited to about 3200 A/µs.

Essential for short-circuit stability is the absence of dynamical avalanche at extreme commutation speeds. Even under these critical conditions the CAL HD shows soft recovery behavior. proving the same high dynamical ruggedness known from the conventional CAL diode, Figure 5.



Figure 5: Dynamical ruggedness of the CAL HD diode for very high dl/dt=6000 A/µs.

To demonstrate the improved performance of power modules achieved by the new CAL HD, simulations of DC/DC converter circuits (e.g. SKM 400 GB 176 D) have been done. Paralleling 4 diodes, the junction temperature was calculated as a function of static and dynamic losses. The maximum load current is defined where the simulated junction temperature of the diode or IGBT is at 125 °C. For the calculation, the thermal and electrical data of table 1 was applied, using a case temperature of Tc=90 °C. The input voltage was set to Vin=1200 V, the output voltage to Vout=600V.

The CAL HD diode shows a significant advantage regarding the output current for switching speeds below 6 kHz, Figure 6. The diode provides optimal device performance in the typical operation range for 1700 V Trench IGBT modules of 2-3 kHz.

Power Systems Design Europe March 2004

	Trench- IGBT	FWD 4 x CAL	FWD 4 x CAL HD
Rthjc (K/W)	0,065	0,125	0,125
Vf @ 300 A (V)	2,2	2,2	1,75
Esw (mJ)	300	38	55

Table 1: Thermal resistance R_{thic}, forward voltage V_f and switching losses E_{sw} of the Trench-IGBT and diodes used for converter simulations.

The improved current rating of the Trench IGBT / CAL HD combination is the result of lower total losses generated in CAL HD diode below 6 kHz. At higher switching frequencies the dynamical losses pick up, compensating for the low static losses and cause higher overall losses compared to standard CAL.

In conclusion, the new CAL HD 1700V is adapted for modern Trench IGBT leading to an excellent performance of

100 e ....... Figure 6: Maximum output current of a

400

300

250



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freewheeling diode and IGBT. In particular, the maximum current density matches the IGBT and the temperature coefficient of the forward characteristic has been pushed to positive values. This makes the CAL HD an ideal solution for parallel operation without thermal overload. In addition,



DC/DC converter using the combination Trench IGBT / CAL (dashed line) and Trench-IGBT/CAL HD diodes (solid line).



Figure 7: Freewheeling diode loss power in a DC/DC. CAL (broken line) and CAL HD (solid line).

the CAL HD diode's soft switching behavior combined with a very high dynamical ruggedness makes this freewheeling diode an ideal choice for modern IGBT power modules: the diode is used in SEMIKRON's new 176 series of SEMITRANS modules, the 2nd generation of SKiiP 3 and in SEMiX.

www.semikron.com

### **Transformers Keep Pace** with DC/DC Technology

#### Acoustic transformers will use Piezoelectric Materials

In recent years, as is the case with many sectors of the electronics industry, companies involved in the design and manufacture of DC/DC converters have been under significant commercial and competitive pressure.

#### Rob Hill, C&D Technologies

he transformer is a key component in a DC/DC converter design in terms of The transformer is a key component in a DC/DC converter design in terms of cost, size and performance, considerable efforts are being made to optimise this component to match the advances in semiconductor and passive component developments. Although conventional wirewound transformers are still in use in many larger form factor power applications, several newer technologies have emerged in recent years that bring significant benefits to DC/DC converter designs, an example being planar wound transformers.



Figure 1. DCDC Converter.

Standalone and embedded planar transformers

Standalone planar transformers fabricated as assemblies, utilise stacks of either flat copper leadframes as windings, or flat copper etched/printed windings of insulating material. This means that they take up a lot less space than traditional transformers that feature round copper wires wound onto bobbins. Precision copper leadframes or printed windings enable design specifications to be met much more precisely than with wire wound transformers, and the level of repeatability from part-to-part also improves.

The etched or stamped copper leadframes or printed windings are stacked in flat, typically high frequency ferrite cores to create the transformer's magnetic circuit. The resultant designs lend themselves to very low profile transformer assemblies. The large cross-sectional area of the copper that can be achieved in planar designs makes high power density, high current designs easier. The high surface-to-volume ratio of planar windings and ferrites allows good heat spreading and dissipation. High efficiency, especially at high operating frequencies, is a further key benefit of planar transformers. In wirewound assemblies.

efficiency can be adversely affected by the 'skin effect' that occurs when high frequency current flowing through a cylindrical conductor forces electron flow away from the center, concentrating it close to the surface of the wire and effectively reducing the conductors cross-sectional area.

From a finishing and assembly point of view, planar transformers also have benefits over wirewound transformers which normally require a manual operation to strip back the enamel on the winding terminations for dip or hand soldering. Stamped or etched copper lead outs on planar transformers can often form surface mount terminations which increases assembly speed and repeatability, thus reducing cost. The advantage is even better with embedded planar transformers where ferrites clamp through apertures in the main DC/DC converter PCB and the windings are spirals on layers of that PCB.

Despite the fact that they take up more space than embedded designs, the popularity of standalone planar transformers has grown in recent years. Because fully embedded transformers use the main DC/DC converter circuit board for their windings, a different



Figure 2. Planar Transformer.

design of circuit board is needed for each input/output voltage combination. Also, in the case of embedded planar designs, the overall system cost is high, due mainly to the need to use a multilayer layer circuit board for the integral etched windings. Some hybrid designs use the main PCB for primary windings which are often common, and then separate small PCBs or stampings for secondaries which vary between output voltages.

Although embedded designs achieve high power density and have very good thermal performance to complement their space saving characteristics, for many applications these benefits are outweighed by the prohibitive cost and lack of flexibility and interchangeability. High production volumes will to a degree offset the higher cost of embedded designs.

#### A technology called 'interleaved' or 'split winding transformers' has been developed by C&D Technologies and implemented on their WPA60 dual-output quarter brick DC/DC converter. This

planar assemblies.

The design interleaves the primary and secondary windings to reduce undesirable leakage inductance. A straightforward 'sandwich' of primarysecondary-primary or, secondary-primary-secondary, can reduce the leakage inductance by a factor of four. High values of leakage inductance can lead to imperfect coupling, losses and voltage transients. Despite the significant benefits of split primary or split secondary transformers there are some important points to consider. For example, there will typically be a larger number of terminations, and isolation of the primary and secondary circuits can be more difficult. Also, in designs that require EMI screens between primary and secondary, an additional number of them will be required.

Future transformer designs

All established transformer designs are based on magnetic technology. In future the large-scale adoption of acoustic coupling techniques offers the potential

#### Standard non-interleaved (split) planar transformers.



#### Interleaved (split) planar transformers.

-	-	Primary 1
-=	-	Secondary
	 -	Screen 2 Primary 2

Winding terminations not shown. One or more windings may be part of a multilayer matherboard.

Figure 3. Planar Transformer Design with Split Winding Design

#### Split winding designs

style of transformer delivers improved efficiency compared to standard

to miniaturize transformer design further. This is already happening to a small degree in some low power DC/DC converter designs with high voltage outputs. Acoustic transformers use the characteristic of piezoelectric materials to acoustically couple power through a vibrating

structure. A transducer excites a resonant mode of the material that is then picked up by a second transducer converting it to a secondary voltage.

Amongst other developments in transformer design is the use of extremely high frequencies of operation that allow efficient air coupling to occur, therefore obviating the need for ferrite. The integration of the transformer with other magnetic parts such as output chokes that feature within the circuit is another advancement that will help reduce the overall form factor of finished DC/DC designs.

Finally, the development of new core materials that allow higher frequencies of operation without high losses, will help to deliver smaller transformers for a given power.

#### Conclusion

It is clear that the suitability of wirewound transformers for DC/DC converter and other applications is diminishing. Their large size and poor efficiency, and the difficulties in achieving repeatability from part to part means that they are rapidly being superseded by newer technologies.

Embedded and standalone planar transformers each have their own benefits and drawbacks, and the selection of one or the other in a design will be largely application driven. Split secondary (or primary) transformers are innovative and offer some useful benefits over conventional designs, once again, the application will determine whether they are the most appropriate choice for a given design. For the future, the move away from magnetic to acoustic based transformers looks set to yield some exciting new products and will broaden further the options open to the DC/DC converter designer.

Product URL: www.cdpoweronline.com Corporate URL: www.cdtechno.com e-mail: info@cdtechno-ncl.com

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### **PCI Bus Systems**

#### On-board power solutions

PCI is an interconnection specification for computer components. It stands for Peripheral Component Interconnect and has been first seen in the marketplace in the early 1990th with Intel's first Pentium CPU Chipsets.

By Ingo Meyer and Dr. Hans-Peter Lüdeke, Tyco

ne of the best aspects of PCI is that it is a vendor and platform independent specification. PCI is basically a 5 volt, 33MHz, 32-bit bus with a basic transfer rate of 133 Mb/s. It also has many design options, which can be combined in any permutation.

- 64-bit bus extension
- 66 MHz extension
- 3.3 volt operation

Hardware developers are faced with huge challenges. While the power density and complexity of circuits are constantly increasing, board space is often tight, development resources are being reduced and there is enormous cost pressure. The fact that the number of supply voltages required has increased is often also counter productive. While the 5 V bus is supplied to the PCI Card voltages of 3.3V, 2.5V, 1.8V, 1.5V or even lower are frequently also necessary, each with several watts of power. The reason for this is constant development by IC manufacturers, who are reducing the voltage level used internally to improve the performance of their components.

For hardware designers, this means that they no longer have to deal just with their actual core competence, the function of the board, they are also increasingly being confronted with issues relating to the power supply concept and realisation. The use of a sophisticated and extremely flexible "modular system" can help to cut costs and development time, reduce the resulting power dissipation and achieve standardisation in terms of the power supplies used.



Figure 1: Modular power supply architecture with non-isolated Tyco Lynx modules

#### **Possible solutions**

With a carefully co-ordinated product range, such as the Lynx range from Tyco Electronics, most applications can be realised with a minimum number of different Point-of-Load converters, without any loss of flexibility. Maximum output currents of 5 A, 10 A and 16 A allow consumers from 3.75 W to 57 W to be supplied. Due to the programmability of the output voltage between 0.75 V and 3.63 V, a maximum of 3 different Lynx converters are necessary to cover this entire power range.

This reduces warehousing and development costs, as new ICs with a changed power demand only necessi-

tate a change of external programming resistor. Maximum heights of 8.3 mm for the SMD version and 12.7 mm for the wired SIP version allow realisation of systems with low circuit board spacing.

#### Product selection

The Lynx product family should be selected with the input voltage based on the Bus supply voltage given by the PCI spec and the output current needed. While both connection options SIP and SMD exists in many cases designers go for the industry SIP standard. All products are approved by CSA, UL and VDE. Table 1 provides recommended Lynx products for PCI card applications.

Product	Vin	Vout	lout	Efficiency**	Interconnection
AXH005A0x	3V 5.5V	0.75V 3.63V programmable	5A	94%	SIP/SMD
AXH010A0	3V 5.5V	0.9V to 3.3V*	10A	95%	SIP/SMD
AXH016A0x	3V 5.5V	0.75V 3.63V programmable	16A	95%	SIP/SMD

* Programmable version in preparation ** At 3.3Vout

Table 1: Recommended Lynx module for PCI card applications.

#### Audio has become more complex

The evolution of the cellular telephone handset is a prime example. To meet these demands, increased functionality is being packed into a smaller number of integrated circuits. To reduce the chip junction temperature space for a heat sink is good design practice.

#### Ken Boyce, National Semiconductor

onsumer demands in the portable electronics market has been towards smaller, lighter, and more feature rich products. Smaller dimension process technologies are used to make more complex, less power consuming, and smaller IC's. Miniaturized IC packaging technologies (micro SMD, BGA, LLP, CSP) have also been a major contributor to meeting product requirements.

Audio requirements are unique. Even if the process technology shrinks, or the phone gets smaller, your ear still requires a certain amount of acoustical energy in order to hear the caller or ringing sounds comfortably.

Also, audio on cellular handsets has become more complex. Features have changed from simple voice communica-







Figure 1. a.) WL-CSP micro SMDs; b.) LLP; c.) 128L dual-row laminate CSP; d.) 192-I/O FBGA with 0.8-mm pitch



tion, to communication with hands free and speakerphone capability, plus MP3 music (stereo) playback. Even simple ring tones are changing to become musical and non-musical mono, stereo, and stereo "3D" ring sounds played from MP3 digital audio files or polyphonic music synthesizer MIDI files, or a combination of both methods.

Each of these "modes" has different power output requirements. As the phones have become smaller, the speakers used have also become smaller. This requires more power to achieve the desired level of output acoustical energy. Over the last 4-5 years, speaker sizes have dropped from about 25mm to 13mm in diameter. Meanwhile, ringer speaker power requirements have gone from about 250mW to nearly 600mW to compensate. In order to get the higher output power, and in response to lower operating voltages in the cell phone, speaker impedances have trended downwards from 8 Ohms to 4 Ohms.

Typically, Class AB amplifiers are used to drive the speaker loads. Because of the output power requirements and typically low operating voltages of portable

electronic devices, the audio amplifiers are operated in the Bridge Tied Load (BTL) configuration, rather than the Single Ended Output mode. This doubles the number of amplifiers on the IC chip.

In the BTL mode, no output coupling capacitors are required between the two amplifier outputs and the speaker. As a result, system low frequency response is improved, and is limited only by the input signal network and the speaker response characteristics. Typical IC audio amplifiers have generally flat amplitude response over the audio frequency band and do not affect the system frequency response. System cost and size are greatly reduced by eliminating the output coupling capacitors.

In the BTL mode, the voltage swing across the load is doubled for any given supply voltage. A key advantage for the BTL mode is that for a fixed load impedance, as the load voltage is doubled, the output power is increased by a factor of 4, according to the equation  $P_{\rm L} = V_{\rm L}^{\,2}/R_{\rm L}.$ 

But, the BTL mode operation also increases the potential power dissipation by a factor of 4.

The power dissipated in a Single Ended Output configuration Class AB amplifier is  $P_D = P_{SUPPLY} - P_{LOAD}$ . The  $P_{LOAD}$  term is the DC equivalent of the AC power in the load when the load is driven with a sine wave signal.

For a Sine wave signal, the maximum power dissipated in a Single Ended Output configuration Class AB amplifier is given as  $P_{D(MAX)} = V_{DD}^2/2\pi^2 R_L$ . For a BTL Output configuration,  $P_{D(MAX)} = 4V_{DD}^2/2\pi^2 R_L = 2V_{DD}^2/\pi^2 R_L$ .

A typical  $P_{D(MAX)}$  vs.  $P_{OUT}$  curve for a BTL amplifier in a micro SMD package is shown below. In some portions of the operating range, the power dissipation actually exceeds the power delivered to the load. Under certain conditions, increasing output power will decrease the power dissipation in the amplifier.



Figure 2. POUT Curve for a BTL Amplifier in a Micro SMD Package.

However, in actual systems, the audio waveform is not usually sinusoidal. There is a mixture of voice and musical waveforms. Therefore, the normal operating power of the amplifier is not the maximum rated power. The actual power dissipation is also less. For such waveforms, the Crest Factor (ratio between the peak power to the average power) is used to calculate average power.

Crest Factor = 10 log (
$$P_{PEAK}/P_{AVE}$$
) = 10 log  $P_{PEAK}$  - 10 log  $P_{AVE}$ 

Crest Factor - 10 log  $P_{PEAK}$  = - 10 log  $P_{AVE}$ 

A Sine wave has a crest factor of 3.01dB (simplified to 3.0). An amplifier rated at 2W peak output power will produce an average 1W output power.

Crest Factor - 10 log  $P_{PEAK}$  = ( - 10 log  $P_{AVE}$  ) 3.01 - 10 log 2 = 3.01 - 3.01 = 0 = ( - 10 log  $P_{AVE}$  ) Therefore,  $P_{AVE}$  must equal 1 (or 1W) since log 1 = 0

Music waveforms typically have crest factors ranging from 12 to 22 dB, with an average of about 15dB. For the amplifier referred to above, similar calculations for a Crest Factor of 15 will show that the average output power (without clipping) will be:  $15 - 10 \log 2 = 15 - 3.01 = 11.99 =$ 

 $(-10 \log P_{AVE});$ 

Therefore, log  $P_{AVE}$  must = (-1.19), and  $P_{AVE}$  = 0.0632, or 63.2 milliwatts.

Voice only waveforms can have higher Crest Factors, and a correspondingly lower average output power. Average power causes heating in the IC, since the "average" is over a period of time. Instantaneous peak power causes relatively little heating, as it is never continuous.

These observations can be used in conjunction with appropriate packages to create complex, high performance, audio sub-systems that contain many different amplifiers properly sized for the loads they will drive.

An example is the LM4857 ITL (See Block Diagram), which contains 2 high power Class AB BTL speaker amplifiers, 2 low power single ended headphone amplifiers, a medium power earpiece speaker amplifier, and a line output buffer amplifier, plus associated volume controls, switching and mixing circuits, and "3D" stereo enhancement for ring sounds and music.

There are 16 output modes, including shutdown. Not all amplifiers are on at the same time. For certain modes, multiple amplifiers are on, and the maximum power dissipation (from the datasheet) is  $1.348W @ V_{DD} = 5V$ , and the maximum junction temperature  $T_{JMAX}$  allowed is  $150^{\circ}$ C.

The industry leading 0.6mm high micro SMD package only utilizes 2.543mm X 2.949mm (7.499mm²) PCB space, making the LM4857 the most space efficient audio sub system available for cellular phones today. The package  $Ø_{JA}$  value is 62°C per watt. To calculate maximum allowable ambient temperature operation, the following formula is used:

#### $T_{JMAX} = P_{DMAX-TOTAL}(\emptyset_{JA}) + T_{AMBIENT}$

Assume sine wave signals, and maximum power dissipation on all amplifiers simultaneously. The allowable ambient temperature operation without violation of the TJMAX value of 150oC would be



Figure 3. LM4857 ITL the Space Efficient Audio Sub System



$$\begin{split} T_{\text{AMBIENT}} &= T_{\text{JMAX}} - P_{\text{DMAX-TOTAL}}(\text{Ø}_{\text{JA}}), \text{ or} \\ T_{\text{AMBIENT}} &= 150 - 1.348(62) = 66.4^{\circ}\text{C}. \end{split}$$

If a higher ambient temperature operation is required, a heat sink would have to be used, or the operating voltage would have to be lowered. In cellular phones, the typical operating voltage is  $3.6V_{DD}$ , not  $5V_{DD}$ . So the ambient operating temperature is easily higher than  $66.4^{\circ}C$ .

If needed, a heat sink can be created by additional copper area on the board around the package, connected to the GND,  $V_{DD}$ , and BTL amplifiers output pins. All National Semiconductor audio amplifiers are specified for the sinusoidal signal condition for power output, and power dissipation calculations. For music and voice signals, the ambient operating temperature can be higher because the average power dissipation (heating effect) is lower. Good design practice would dictate adding a heat sink where space is available to further reduce the chip junction temperature.

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### **Optical-Based Analog Front End**

#### Powerline communications in the home

Low-speed digital communications systems for use over power wiring have been deployed. The common feature of all these systems is that they operate with low- to medium-frequency carriers and narrow transmitting bandwidths.

#### By Patrick Sullivan, Agilent Technologies

he use of high-voltage power lines to carry voice signals has a history dating back to the early 1920s, with low-frequency amplitude-modulation systems operating over lines with voltages as high as 220,000 providing reliable voice links between power generating stations and dispatcher's offices. Later, the power utilities' carrier-current communications systems were refined to use single-sideband (SSB) multiplecarrier technology, and gradually expanded to include telemetry providing continual monitoring of load, voltage, and other power-system characteristics, as well as remote control of switching stations in remote locations.

Carrier-current systems that operate over the 120/240-volt AC electrical wiring in homes and commercial buildings have also been around for many years. Some examples include intercoms and baby monitors; remote controls for lights, switched AC outlets and appliances; and carrier-current AM radio transmitters using power wiring to broadcast programming within limited areas such as building and educational campuses. More recently low-speed digital communications systems for use over power wiring have been deployed. The common feature of all these systems is that they operate with low- to medium-frequency carriers and narrow transmitting bandwidths.

In Europe, the European Committee for Electrotechnical Standardization, CENELEC, produced EN50065, a standard covering the requirements for transmitting and receiving digital signals over 120/240-VAC wiring using carrier frequencies in the 3 kHz to 148.5 kHz range. The U.S. Federal Communications Commission has regulations for similar applications within the 45 kHz to 450 kHz frequency range, and in Japan PLC is permitted in the 10 kHz to 450 kHz range.

Today low-frequency powerline carrier modems can be used for many additional applications in homes and businesses, including:

- Home appliances
- Heating and ventilation Control
- Lighting control
- · Low-speed data communications networks
- Signs and information displays
- Fire and security alarm systems

These applications and frequencies are very different from the Broadband over Powerline (BPL) networking technologies, which are designed to provide networking and Internet access at DSL or cable modem speeds over electrical power wiring. "Home BPL" operates over the 120/240 VAC low-voltage distribution wires, while "Access BPL" operates over the medium-voltage (1 kV - 40 kV) power distribution network, to carry data over longer distances. BPL carrier frequencies are in the 1 MHz to 80 MHz (megahertz), high frequency range.

#### Significance of the Analog Front End (AFE) to powerline modems

The use of digital signal processing techniques has significantly improved communication performance, but the troublesome problem of how to couple the analog-modulated signals from a powerline modem to and from electrical wiring has not seen any significant developments. The analog signal processing circuitry, together with other components required to couple the modulated signal on and off the power line is commonly given the collective name of analog front-end (AFE).

The AFE is called upon to provide voltage and current signal amplification, as well as providing galvanic isolation to protect the user and equipment being interfaced from both the nominal 120/240 volts and the transient voltages, which are common to power wiring. It is traditionally a complex circuit combining many discrete components with bulky isolation transformers.

This article introduces a new approach to the AFE, which uses optical coupling technology to provide significant improvements in the areas of power



Figure 1: Typical frequency-shift keying (FSK) powerline communication modem (PLM) for use in home automation applications.

efficiency, system robustness and overall solution cost.

Figure 1 shows a block diagram of a typical powerline communication modem for use in home automation applications. The modulated signal is generated with a digital look-up table and a digital-toanalog converter (DAC). Demodulation is also carried out digitally, by first converting the received analog signal into the digital domain with an analog-to-digital converter (ADC), and then by applying subsequent digital processing. These two functions are typically integrated into a single modulator/demodulator (modem) IC fabricated using a low-voltage CMOS process.

The use of CMOS IC processes allows the optimization of the die size, cost and power dissipation. However it makes the integration of analog circuitry problematic, which means that some, if not all, of the analog signal processing circuitry must be provided externally.

Although the modulator/demodulator topology used in the digital IC has a significant impact on overall communication performance, it is fair to say that in many cases the performance of the AFE has an equal, if not greater influence on the overall performance of the powerline modem.

#### **AFE Requirements**

The power line communication medium is a difficult environment compared to dedicated STP (shielded twisted pair) or coaxial cables. It places additional

constraints and requirements on the AFE, particularly in the areas of:

- Insulation for voltage safety
- Surge voltage immunity Line attenuation

The 120 or 240 volts on home power wiring are potentially dangerous to the user. International safety norms and equipment regulations require the use of appropriate insulation barriers to protect the end user from the risk of electric shock. The traditional method used in powerline modems to provide safe insulation is an appropriately constructed and certified isolation transformer for coupling the modulated signal to and from the power line.

High voltage transient surges are a frequent occurrence on the power line and are considered to be normal and inevitable. However without sufficient protection all electrical circuitry is at risk from surge voltage-related damage. In particular semiconductor devices are vulnerable, since they can suffer either immediate catastrophic failure or accumulated damage resulting in shortened lifetimes.

In most power line-operated electronic equipment the only coupling mechanism between a power line voltage transient and the sensitive low-voltage circuitry is through the power supply. The low voltage circuits are normally very well protected from power line transients by the inherent low-pass filter characteristics of the power supply itself. Consequently

 Electromagnetic interference (EMI) • Electromagnetic compatibility (EMC) the risk to the low voltage circuits is normally considered insignificant. The powerline modem, though, necessitates a higher-frequency communication path between the power line and the low voltage circuitry. Unfortunately this path not only enables data communications but also opens up the possibility of the transfer of power line surges into the sensitive low voltage circuitry.

To minimize this risk, it is common practice to incorporate supplementary over-voltage protection in the form of clamp diodes, silicon avalanche diodes and MOVs (metal oxide varistor). All of these protection devices have a significant amount of parasitic capacitance, which has the propensity of attenuating received signals. This means that the highest level of protection could also severely attenuate the desired communications.

#### **Electromagnetic Compatibility**

The operation of powerline modems can potentially create objectionable interference to radio-frequency appliances such as radios and televisions, either by interference conducted through the power wiring or radiated over the air from the power wiring.

With respect to conducted interference, manufactures of powerline modems must ensure that the frequencies and amplitudes of the modulated signals meet applicable international conducted emission profiles, and guard against inadvertently transmitting out of band harmonics.

Electromagnetic emissions are similarly regulated. In the case of powerline modems electromagnetic interference (EMI) is of particular concern because most wiring is not shielded in any effective way. Unshielded communication cables subjected to common-mode currents have a very high propensity to propagate electromagnetic interference. Electromagnetic emissions can be minimized by either reducing the commonmode voltage or by increasing the common-mode impedance by minimizing the parasitic capacitance of the coupling device.

#### Attenuation

Communication signals on the power line are subjected to various degrees of attenuation, which vary with time and frequency.

One of the worst culprits for attenuating PLM signals are the capacitors installed to filter out the switching harmonics of switched-mode power supplies and lamp ballasts. On the one hand, implementers of PLM are grateful that these filter capacitors are installed, because they attenuate conducted noise transients. The downside is that the same capacitors can result in a very low power line impedance at the carrier frequencies used by home PLMs. Consequently the first measure taken to minimize attenuation of the transmitted signal is the use of a low impedance coupling circuit and a transmitter output stage with a high output current capability. This ensures minimum attenuation at the signal injection point. To counter inevitable attenuation of the transmitted signal the AFE receiver circuit amplifies the received signal before demodulating.

#### Immunity to Electromagnetic Interference

Electromagnetic interference immunity is the ability of the receiver to reject the interference generated by intentional and unintentional conducted and electromagnetic radiation. The EMI immunity performance of the PLM can be optimized in several ways. The first method is to maximize the signal-to-noise ratio (SNR) by minimizing the noise observed at the receiver. The second is to use noise-tolerant communication methods such as forward error correction (FEC) coding. The third method involves the use of multiple carrier frequencies. In practice, using a combination of these methods provides satisfactory EMI immunity. With respect to the AFE, reducing the amount of noise reaching the receiver enhances EMI immunity.

#### Noise propagates into the PLM receiver circuit in two ways: differential mode and common mode

With differential noise, the noise is injected from the noise source as a voltage between the live and neutral wires of the power wiring. This differential noise signal is subject to the same attenuation effects as the transmitted modem signal. Consequently the amount of differential noise at the receiver will be dependent on the position of the noise injection point relative to the location of the receiving point.

In the case of common-mode noise, unshielded cables act as good antennas for picking up electromagnetic signals from both intentional emitters such as radio stations and unintentional emitters such as universal motors and lamp ballasts. The power line is no exception: since the live and neutral conductors run in close proximity to each other, electromagnetic noise is equally coupled onto both.



Figure 2: The leadframe used for the Agilent HCPL-800J, a bi-directional optical analog front end (AFE) packaged in a 16-pin SOIC (Small Outline IC) package.

The amplitude of the common-mode noise coupled onto the power line will depend on the length of the conductors, and their position relatively to the devices radiating the electromagnetic noise. The power line impedance loads do not attenuate the common-mode noise voltage in the same way as they do to differential-mode noise. The consequence is that the common-mode noise becomes more significant in the case of heavily attenuated communications signals.

The amount of common-mode noise reaching the receiver is dependent on the leakage capacitance of the signal coupling transformer and the noise frequency. Ultimately the receiver circuit is not directly affected by common-mode noise, but is affected by common-mode noise converted to differential-mode noise by unavoidable asymmetry in the cable, transformer and receiver circuitry itself.

To reduce the influence of both differential and common-mode noise, a passive or active filter is used at the front end of the receiver. In this manner noise frequencies outside the communication band can be very effectively removed.

More difficult to filter out are noise sources close to the transmitted carrier frequencies. It is these noise sources and the in band noise frequencies which ultimately cause the residual EMI immunity limitations for PLMs.

#### **Optically coupled AFEs**

A transformer can inherently propagate signals in either direction while optical coupling methods use a unidirectional combination of optical emitter and detector, and can only propagate signals in one direction. To achieve bi-directional Communication in an optical AFE, one transformer has to be replaced with two optical channels. Fortunately optical packaging platforms allow multiple optical channels to be integrated into standard SMD type packages.

Figure 2 illustrates the construction of an integrated optical PLM AFE. Packaged inside the optical AFE are four discrete semiconductor elements: two LEDs (LED1 and LED2) and two BICMOS integrated circuits (IC1 and IC2). IC1 is ground referenced to the low voltage circuitry and IC2 is ground referenced to the power line.

Figure 3 is the block diagram of the AFE. With respect to the transmit optical path, IC1 includes a transconductance amplifier, which drives LED1 with a forward current equal to the sum of a DC biasing current and a current which is directly proportional to the analog input signal. The type of LED used has a very linear current-to-light transfer characteristic to minimize harmonic distortion resulting from the electrical-to-optical conversion.

On the power line side of the isolation boundary, a photodiode and photodetector amplifier are integrated into IC2, with circuit converting captured photons to an output voltage which is linearly related to the light emission of LED1.

The output of the photodetector amplifier is coupled to the output stage via an external AC coupling circuit. The primary function of the coupling circuit is to remove residual DC offset voltage from the output of the photodetector amplifier. This coupling circuit may also include filtering or frequency shaping to remove out-of-band harmonics generated in the modulator or optical channel.

The operation of the receiver optical path is very similar to that of the transmitter path with the optical emitter and detector functions integrated in IC2 and IC1, respectively.

In addition to the basic function of coupling transmitted and received signals other important features are integrated into the optical AFE. The first is the implementation of a highly linear line driver circuit, which is capable of delivering up to 1.0 A peak-to-peak. This high current capability ensures that an adequate transmit signal level is coupled onto the power line even in the case of very low power line impedance. The low distortion specification ensures that the generation of out-of-band harmonics is minimized.



Figure 3: Block diagram showing the two CMOS ICs and the LED emitters used in the optical AFE.

The optical AFE also includes an additional gain stage in the receive function, which may be used to amplify attenuated signals ensuring optimal link integrity even in worst-case signaling environments.

The optical AFE incorporates integrated control functions. To ensure that the line driver does not unnecessarily attenuate received signals, it is important that the line driver be switched to a high impedance state while the PLM is receiving signals. Normally this would require the use of an additional isolated communication channel to couple the transmit-enable signal from the modulator control circuit to the line driver. To minimize packaging complexities the optical AFE allows digital control signals to be simultaneously multiplexed with the analog signals, allowing a single optical channel to simultaneously transmit analog and digital control signals. One of these digital signals is the transmit-enable signal.

Since the output stage of the PLM is totally isolated from the appliance, in some cases the appliance's control circuitry would have no way of determining whether or not the Vcc2 power supply voltage is present and correct. To prevent such a scenario an under-voltage detection circuit is included on IC2, which monitors Vcc2 and transmits an indicator signal across the isolation boundary manner similar to that used for the transmit-enable signal.

#### **Protection features**

To ensure maximum robustness of the modem the line driver circuit includes over-temperature and over-current protection. The over-current signal works in two ways: First it clamps the peak output current to a safe sustainable level; second it transmits an over-current signal back across the isolation boundary. Normally the peak output current is limited by the combined influence of the coupling impedance and the power line load.

Since the worst-case power line load can be very small, in some cases as low as 1_, the resulting peak current levels can potentially reach very high levels. To meet a realistic peak current limit, the coupling impedance has to be sufficiently large. Such high coupling impedance unfortunately will result in some attenuation of the transmit signal at nominal load conditions.

The provision of the isolated overcurrent signal facilitates an alternate peak current limiting strategy. That is to use the over-current signal to signal the microcontroller to progressively reduce the transmit signal amplitude until the overcurrent flag is disabled. Such a control strategy allows the use of a very small coupling impedance maximizing coupling efficiency under all load conditions.

#### Conclusion

One of the first and most obvious advantages of an optical solution is the ability to construct a low profile SMD component that contains not only the isolated coupling mechanism but also much of the analog signal processing components. This results in a large reduction in the number of components required, which in turn reduces the complexity and cost of a PLM. Figure 4 shows a complete powerline modem using an optical AFE.

In addition to these benefits an optical solution offers performance advantages, particularly in the areas of EMC, EMI and surge immunity. With respect to EMC and EMI optimization, reducing the parasitic capacitance of the isolation component increases the common mode impedance, which in turn reduces electromagnetic emissions and sensitivity to common mode noise transients.



Figure 4: A complete powerline modem using the optical analog front-end.

The leakage capacitance of an optical signal-coupling device is directly related to the separation distance and coupling area between the optical emitter and detector. Unlike magnetic transformers, the optical signal coupling devices do not require close physical coupling to achieve satisfactory performance. Theoretically, optically coupled signal paths can operate through an optical fiber at distances of hundreds of kilometers, making the common-mode impedance infinitely high. In practical terms, optically integrated devices in standard SMD packages typically exhibit coupling capacitance on the order of 1.3 pF. This is a very significant improvement over magnetic transformers, which typically exhibit parasitic capacitances in the range of 30 to 100 pF.

Magnetic signal transformers are capable of not just transmitting and receiving communication signals; they are also capable of coupling high voltage surge transients. Conversely optical coupling devices are only inherently capable of coupling low-power optical signals. Transient voltage surges are very effectively blocked from reaching the low voltage appliance circuitry. From a practical point of view this means that the overall robustness of an electrical appliance need not be degraded by the inclusion of a PLM.

#### www.agilent.com



### **How to Choose** the Proper Core for **Power Magnetics**

#### Core material selection is crucial

Durability is an important design aspect that needs careful consideration where devices are exposed to conditions of high vibration, mechanical and thermal shock. Cores with sharp corners or thin dimensions can fracture in these conditions.

#### By Bill Derks, Cooper

roper core choice is critical to successfully designing power magnetics. A design engineer uses experience to move in the right direction early in the design process. Material and manufacturing costs are often preeminent considerations while specified size constraints narrow the choices. Published data on the core dimensions, material limitations and performance are used to determine the design tradeoffs. Each core shape and material has advantages and disadvantages. Several design considerations need to be addressed before the design can be finalized. These include core loss, saturation, permeability, robustness, frequency and temperature response. Some core shapes and materials lend themselves to certain applications better than others.

#### **Core Shapes**

Cores of various shapes are listed in Figure 1 & 2. Each shape has certain advantages and disadvantages. Toroids are low cost, durable and exhibit low EMI unless a mechanical gap is added. The winding labor is greater when compared to other shapes and it often requires the added expense of a header/base for mounting. The EE or EI cores are also low cost industry stan-

dards, which can utilize a bobbin coil form for coils that require high a number of turns. High-speed machine winding is an advantage but for high current applications, where the number of turns is low, the bobbin cost if prohibitive. The EFD cores are similar to the EE and are used when the requirements are low profile SMT. Their long center legs facilitate the use of margins needed to meet creepage and clearance distance requirements. Drum or bobbin cores are also low cost and can be machine wound, yet the high stray flux field often exhibits EMI levels which are unacceptable for some power supplies. When a shield is added, the EMI is greatly reduced. The shielded drum design has high-energy density that makes it an excellent design approach when size constraints are limiting. The UI core lends itself well to high current applications where copper foil conductors are needed. A header for SMT mounting is typically required. The EP. PQ. RM and P cores offer better EMI shielding than the EE or Drum, but the cost is considerably more. Although, when throughhole mounting is acceptable, these often have related bobbins with up to 14 pins. The ER core is a good choice for low profile, high current applications. Even



though the cost is higher than EE cores, these can utilize SMT clips or be selfleaded using flat wire.



Figure 1. Cores of various Shapes



Figure 2. Example of Cores of various Shapes

#### **Core Material**

Core material selection is crucial. Table 1 shows several advantages vs. disadvantages. Table 2 lists some important constraints with a relative cost comparison. Material parameters shown are for typical materials. Most materials are available in multiple formulations. Therefore the specific parameters will vary.

Ferrite MnZn is the material of choice where core loss is important. The lower permeability NiZn ferrite typically offers much higher frequency capabilities than MnZn. It also has low conductivity, which is a benefit for drum core designs. Metallized pads can be incorporated onto a shield for the shielded drum designs. The low permeability of the NiZn is of less concern in the shield drum designs because the mechanical gap has the most effect on the inductance. Powder Iron toroids are a cost-effective choice which should be considered for initial designs. Molvbdenum Permallov. High Flux, and Sendust have several advantages over powder iron. But these come at a cost. The Molybdenum, or MPP, offers the lowest core loss with moderate bias capabilities. Hyflux has the best DC bias characteristics. Sendust offers the lowest cost with the worst bias capabilities of the three. Amorphous is a nanocrystalline material in which the oven firing temperature sets the permeability. A low firing temperature induces a lower number of distributed gaps and therefore provides permeability values as high as 100,000. But core loss is higher and the permeability can be considerably reduced when the inductor in exposed to IR reflow temperatures. Therefore, the moderate permeablity amorphous cores are a good consideration.

#### **Design Considerations**

Permeability vs. Frequency: The inductor operating frequency range is affected by the core material properties. Other parasitic considerations are coupling, skin effect, & proximity. Winding dimensions predominantly affect these. For example, a core structure that can enable a long winding transverse will help to improve coupling and reduce leakage inductance.

	Core Materials				
	Advantages	Disadvantages			
Ferrite ~ MnZn	Low Core Loss, High Penn High Prequency up to low Mhz	Cost, Fast Rolloff Low B-Sat, Temp Stability			
Ferrite – NiZn	Low Condustivity. Wind on core. Very High Freq up to 300Mtz plus	Higher Care Loss than MnZn Low B-Sat. Low permeability.			
Powder Iron	Lowest Cost	High Core Loss, Low Freq			
Molybdenum Permalloy ~ MPP	Good DC Biss Low Core Loss	High Cost Excellent Temp Stability			
High Flux	Best DC Bies, High Bast, Low Core Loss	Average Cost			
Sendust	Good DC bias, Low Cost	Average Care Loss & DC Bias			
Amorphous	High Permerbility	Highest Cost, Poor Temp Stability			

Table 1. Core Materials.

			Frequenc	y Range	Typical	Relative	Relative
Parameter	μο	Bm	(kHz) (	typical)	Temp	Cost	Losses
Material	(perneability)	Gauss	Min	Max	(max, *C)		
Iron Powder							
(Iron)	5-80	10000	0.01	500	105	lowest	high
MPP Cores							
(80% Nickel)	14-550	7000	0.01	1800	140	high	low
Hi-Flux Powder Cores							
(50% Nickel-50% Iron)	14-160	14000	0.01	2000	130	low	moderate
Sendust Cores							
(Iron-Silicon-Aluminum)	26-125	10000	0.01	10000	200	low	low
Tape Wound Cores							
(Amorphous)	3000-20000	5000-16000	0.01	1000	110	high	low
Ferrite Cores							
(MnZn)	750-3000	3000-5000	10	2000	150	low	lowest
Ferrite Cores							
(NiZn)	10-1500	3000-5000	100	100000	175	low	very low

Table 2. Important Constraints of Core Material with a relative Cost Comparison.



Figure 3. Permeability vs. DC Bias.



Figure 4. Inductance vs. Bias.

Permeability vs. DC Bias: The gapped ferrite has a level inductance until it nears saturation. The MPP, Powder Iron, High Flux, & Sendust have distributed gaps, which exhibit a favorable slow rolloff. Power supply designers prefer slow roll-off because the inductor does not saturate as easily during overload conditions and it reduces high peak currents in the IC.

Core Loss: Core loss is an energy drain, which heats the inductor and reduces the allowable current rating for the defined temperature rise. Low loss materials often cost more.

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Core shapes approximating a cube give the best surface area to volume ratio for maximum heat dissipation.

Thermal Characteristics: The core material must maintain its properties above the worst case operating temperature of the inductor or transformer. High permeability materials can have significant reduction near normal operating temperature. The current rating of common mode chokes are limited by this constraint. In addition, elevated temperatures effect low cost, powder iron materials over time. State of the art materials are now addressing this Thermal Aging problem.

Durability is an important design aspect that needs careful consideration where devices are exposed to conditions of high vibration, mechanical and thermal shock. Cores with sharp corners or thin dimensions can fracture in these conditions. Also, a core supplier's firing process can introduce micro-cracks. In an ungapped design, this can reduce the inductance considerably.



Figure 5. Core Loss vs. Frequency.



Figure 6. Thermal Characteristics.

#### Applications

*Common Mode:* The preferred choice is a high permeability ferrite in the shape of a toroid or an ungapped EE core. Core loss is of little concern because the magnetic flux fields nearly cancel resulting in a very low flux density which translates to very little core loss.

*Flyback:* A typical flyback transformer or coupled inductor is designed with a gapped ferrite core wound on bobbin with 4 or more pins. The gapped ferrite may be chosen for low core loss. A high Bsat rating is also advantageous.

*High Current:* As with the flyback, a high current inductor requires a gap, either mechanical or distributed. Ferrite material may be needed to reduce losses in high frequency applications. But these often require a mechanical gap. The lower cost powder iron has a built in distributed gap and offers better DC bias characteristics.

Hyflux, Sendust, and MPP are good alternatives. Ferrite material may be needed for high frequency. Foil or flat wire winding provides best space utilization.

Buck & Boost Inductor: Distributed gap toroid using MPP, High Flux, Powder Iron, or Sendust. Drum Core for lower cost.

*Push-Pull:* The low profile EFD ungapped ferrite cores are good initial consideration due to the need for good coupling afforded by the long winding transverse.

There are no absolute best choices for core shape and material combination. The optimum design is not always low cost. An efficient low loss higher cost design may be needed to achieve the design win. A low cost design is also dependent on several factors including the suppliers manufacturing capabilities.

www.cooperindustries.com



#### Next State of the Art of Circuit Simulation



Ansoft announces Nexxim, a product targeting the next generation of analog/mixed-signal applications, including high-performance RFCMOS, GaAs/SiGe RF ICs and gigabit computer and communication backplanes. Customer benchmarks solved to date include a 1.8GHz PLL (phase-locked loop) in 0.25 micron CMOS with over 2000 BSIM3 transistors, a complete RF/analog frontend for a Bluetooth(r) BiCMOS SOC with over 4000 active devices, a memory cell with over 13,000 BSIM3 transistors, an RF mixer analyzed with more than 1000 harmonics, and a 3 Gsps ADC (analog-to-digital converter) in 0.35

#### **Colour Display and Extra Memory to Analyzer**



ILEM has enhanced its NORMA 4000 power analyser with a colour display and a memory option. No other analyser offers such high performance and accuracy in such a compact box, making it especially suitable for on-site measure-

www.powersystemsdesign.com

ment. The Analyzer measures current and voltage with high accuracy and calculates active, reactive and apparent power and other derived values. Its accuracy is independent of waveform, frequency and phase shift across a wide range. Harmonics are calculated at up to half the sampling rate. Voltages up to 1000V and currents up to 10A can be measured directly due to integrated voltage dividers and shunts. It is also possible to connect external voltage dividers, as well as shunts or probes.

The handy device can easily be carried to the measurement site. This allows parameters of electrical systems, such as heating, harmonics, disturbances and current consumption, to be measured on working systems in the micron GaAs. Each benchmark has driven product development and has proven the added value of Nexxim over competing circuit simulation tools.

With a multitude of algorithmic innovations in transient and harmonic-balance analyses, Nexxim achieves unprecedented robust convergence and simulation speeds while improving accuracy and dynamic range. Nexxim addresses a major industry concern by running frequency - and time-domain analyses using the same circuit netlist and the same library models, thus guaranteeing consistent results from the two different domains. Designers of high-performance ICs and

PCBs will no longer have to spend countless hours reconciling results from two different simulators each running from different netlists and different versions of device models.

www.ansoft.com

field, and not just in the laboratory. The colour display makes it easier to look at every single phase in the representations of the current harmonics, voltage and power with FFT methods (Fast Fourier Transformation) and chart representations. All measured values and charts can also be saved in the device and can be transferred to a PC via an RS-232 interface. With the new memory option, the device has a memory space of 128 MB. The instrument's accuracy of 0.1% and its bandwidth of DC to 3MHz make it particularly suitable for measurements on drive systems, power supply systems and lighting technology.

www.lem.com

#### **High-Voltage SuperFET**



Fairchild announces two high-voltage MOSFETs utilizing Fairchild's SuperFET technology to significantly reduce system power loss, increasing efficiency

and reliability in SMPS and PFC applications. Fairchild's proprietary SuperFET technology implements a compensation region using a multi epitaxy layer to improve on-resistance. The FCP11N60 and the FCPF11N60 SuperFET MOSFETs feature low Figure of Merit  $(FOM = RDS(on) \times Qgd)$ , with the FCP11N60 device offering the best available FOM compared to products of the same RDS(on) level. Both provide best-in-class di/dt (1430 A/us, max) resulting from the devices' wide bodydiode profile to ensure increased ruggedness, ultra-low RDS(on) (0.32

ohm, typical), and low effective output capacitance (Coss=35nC, typical). The FCP11N60 and the FCPF11N60 offer optimized gate charge levels (Qg=40nC, typical) for reduced gate driver power rating and switching power losses.

The devices provide improved power density in the available TO-220 and TO-220F packaging. This lead-free product meets or exceeds the requirements of the joint IPC/JEDEC standard J-STD-020B and is compliant with the European Union requirements, which will take effect in 2005.

www.fairchildsemi.com

#### **Two-Phase DC-DC Power Blocks**



International Rectifier has introduced the dual output, two-phase DC-DC power blocks in single, easy-to-use BGA packages for synchronous buck applications. The devices simplify design, reduce size and streamline computing and telecommunication power system time-to-market. Today's advanced telecom, networking

and server systems have as many as six voltage rails throughout the system board. The iPOWIR iP1201 and iP1202 give computer and telecommunications designers a single device to supply two independent voltage rails, simplifying power supply design and reducing board space by up to 59% compared to equivalent circuits made with discrete components. In addition, the new power blocks have no de-rating requirements up to 90°C circuit board and device case temperature. They are fully optimized for medium current synchronous buck applications requiring up to 15A dual output or 30A single output with an interleaved input. The devices feature built-in, full-function PWM control and

protection circuits with optimized power semiconductors and passive components to achieve high power density. Only an output inductor, input and output capacitors per channel, and a few external components are required to build a complete dual output synchronous buck power supply. The iP1201 covers input bus voltages from 3V to 5.5V and the iP1202 covers from 5.5V to 13.2V, with outputs as low as 0.8V and as high as 5V at full current. They provide over-voltage and over-temperature protection, while independent soft start for each output enables various power sequencing and tracking options.

www.irf.com

#### **Fast Response Gate Drive Transformers**



Datatronic gate drive transformers offer high performance, compact size, high temperature compatibility and economy advantages for a wide range

of equipment. Turns ratios available, depending on model configuration, are: 2:1:1, 1:1.5, 1:1 and 1:1:1.

With an inductance range from 330uH to 2.0mH, they provide excellent drive characteristics for power supplies in PCs. telecommunications. instrumentation and other electronic devices. DCR ranges from 1.0 to 2.0 ohms, depending on the turns ratio of the model.

Some models feature profiles as low as 4.0 mm maximum, flat top design in packages as small as 6.0 x 8.4 mm for compatibility with high-density circuit

designs. Their flat top design makes them ideal for automated pick and place manufacturing, and they are available in tape-and-reel packaging. Designed with materials to withstand temperatures ranging from -40 to 130∞C and meet UL94V-0, they are compatible with reflow soldering techniques. The SM76760, SM76922, SM76924 and SM76925 Gate Drive Transformers delivery time is stock to four weeks on common values.

#### www.datatronics.com

#### **Quad Power over Ethernet Controller**



Building on its industry leading Hot Swap controller technology, Linear Technology is shipping two quad Power over Ethernet (PoE) controllers that are fully compliant with the IEEE 802.3af specification. These controllers provide autonomous operation for Power Sourcing Equipment (PSE), sequencing through all of the required tasks without procesThe recently approved IEEE 802.3af

sor intervention. The devices can operate in either automatic standalone or processor-controlled modes. The LTC4258 implements the 802.3af detection and classification, current limiting for normal and fault operation and DC disconnect detection. The LTC4259 performs the same functions but also adds the ability to implement AC disconnect detection. Both devices can communicate with the host over the two-wire I2C bus, requiring minimal firmware support. The precision measurements for detection, classification and current sensing are performed by dedicated internal circuitry with fully specified accuracy. Power over Ethernet specification defines a method to allow DC power to be delivered simultaneously over

#### **Digital Power Management**



Power-One announced the unprecedented integration of power conversion, control, and communications with the introduction of the Z-One Digital IBATM architecture. This digital power management architecture provides a 50% reduction in Printed Circuit Board (PCB)

space, 20% cost savings, and a 90% decrease in components, number of PCB traces, and power-system development time. The Z-OneTM system provides customers with a totally-integrated solution for board-level power management. This patent-pending architecture incorporates intelligent-power Z-POLTM DC-DC converters, the ZIOSTM operating system, and the Z-One digital bus; all controlled by the Digital Power Manager. The Z-One Digital IBA architecture combines many innovative operating concepts. A multitude of parameters, such as output voltages, sequencing, and protection limits are user-programmed through a Graphical User Interface (GUI) and stored in the

#### **Stepdown Switching Regulator ICs**



Allegro has its SI-8000 Series a family of stepdown switching regulator ICs with output voltage ratings from 1.5 to 12 V and current outputs of 1.5 and 3 A introduced.

Designed to produce a regulated output voltage from a higher-voltage input ranging from 18 to 50 V, the new buckconvertor ICs are available in a variety of package styles including miniature

Ethernet networks. With about 13W of power available from the PSE, small data devices can be powered by their Ethernet connection, free from AC wall outlets. The challenge is more than simply providing power to these new applications; there must also be safeguards to protect Ethernet ports in regular PCs and laptops from potentially destructive 48V common mode signal levels. The quad configuration in the 36-pin SSOP package is optimized for board density in multi-channel systems. The only external components required are the external MOSFETs, sense resistors and passive components required for the chosen detection method.

www.linear.com

Digital Power Manager. This parametric information is used to program the pointof-load converters at system startup. Ongoing communications, between power system components and the host system, support intelligent-power system operation. The advanced Z-One digital bus provides synchronization and data over a single line to support bi-directional communications between the ZIOS GUI, Digital Power Managers, digital PWM controlled Z-POL converters, and host system I2C communications. This patent-pending high-speed bus can address all 32 Z-POL converters in a single communications cycle.

www.power-one.com

DIP8 surface-mount types. The family includes both fixed and adjustable output devices and single- and dual-output versions. Operating frequencies range from 110 kHz to 400 kHz. Features such as output enable, soft start, overcurrent protection and thermal shutdown are included as standard, while efficiency levels are between 80% and 85%.

#### **IMS in High Power Density Applications**



Bergquist's Thermal Clad Insulated Metal Substrate (IMS) technologies will significantly reduce the cost and the complexity of thermal management in high power density surface mount applications. The new T-Clad materials are ideal substrates for power conversion designs, motor drives, solid sate relays, power LED displays, and other applica-

tions where size constraints, die size reductions and high component densities make semiconductor heat dissipation a major design challenge.

T-Clad substrates minimise thermal impedance and conduct heat much more efficiently than standard printed circuit board materials. As a result, cooling with T-Clad can help to extend die life through lower operating temperatures, reduce PCB size, increase power densities, and simplify assembly through the elimination of heat sinks, device clips, cooling fans and other hardware. In addition, T-Clad substrates minimise interconnects and are more robust than the fragile thick-film ceramics and direct bond copper (DBC) constructions often used in modern applications.

Based on a three-layered system, T-Clad boards typically comprise the printed circuit foil layer, the dielectric layer, and the base layer. Circuit layers range in thickness from 35 to 350µm. Base layers are typically 1.0mm thick aluminium, although other thicknesses and other metals-including coppermay be used. Circuit layer and base layer are bonded together by the multiple layer dielectric, which combines electrical isolation with minimum thermal resistance. Furthermore. T-Clad can be used to replace FR-4 in conventional multi-layer assemblies to reduce the thickness of the copper circuit layer.

www.bergquistcompany.com

#### Accurate Readings of Energy



Analog Devices' energy metering ICs, the ADE7753 and ADE7758 now allow utility companies to obtain more accurate energy usage information than ever before. Reactive energy, caused by non-

linear loads, requires energy suppliers to supply more volt-amps to customers than they can measure with a conventional watt-hour (active energy) meter. The ability to measure reactive energy enables utility companies to prevent revenue loss and improve powergeneration capacity management. The ADE7758, which features second-order sigma-delta ADCs, is designed for midrange three-phase energy meters. For each phase, the chip measures reactive, active, and apparent energy; as well as rms voltage and rms current. These

measurements are accessed via a serial interface that allows a fully automated digital calibration. The ADE7758 interfaces with a variety of sensors, including current transformers and di/dt current sensors, such as Rogowski coils. Like other products in the ADE family, the ADE7758 provides accurate active energy measurements with less than 0.1 percent gain error over a current dynamic range of 1000:1. Its reactive energy measurement also surpasses the Class 2 IEC61268 accuracy requirement of VAR-hr meters.

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Power Systems Design Europe March 2004

International Exhibition & Conference for **POWER ELECTRONICS INTELLIGENT MOTION POWER QUALITY** 25 – 27 May 2004 **Exhibition Centre Nuremberg** 



### Europe 2004



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### DirectFET[™] MOSFETS RAISE THE BAR IN CIRCUIT EFFICIENCY

DirectFET Delivers Lowest R_{DS(on)} for Highest Efficiency Synchronous Rectification Circuits



Pate	function	BVD55	Resident Ger 1 Dives	18	19:00 Tana=25°C	Ge typ.	OLD IND.	bayout code per AN-1035
IRF6618	Sync FET	371	22πΩ	±207	1504	46eK	15eC	MT
IRF6612	Sync FET	30V	3.6m2	±201	B9A	28nC	8.8+C	MX

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- Best performance synchronous rectifier in DirectFET package
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