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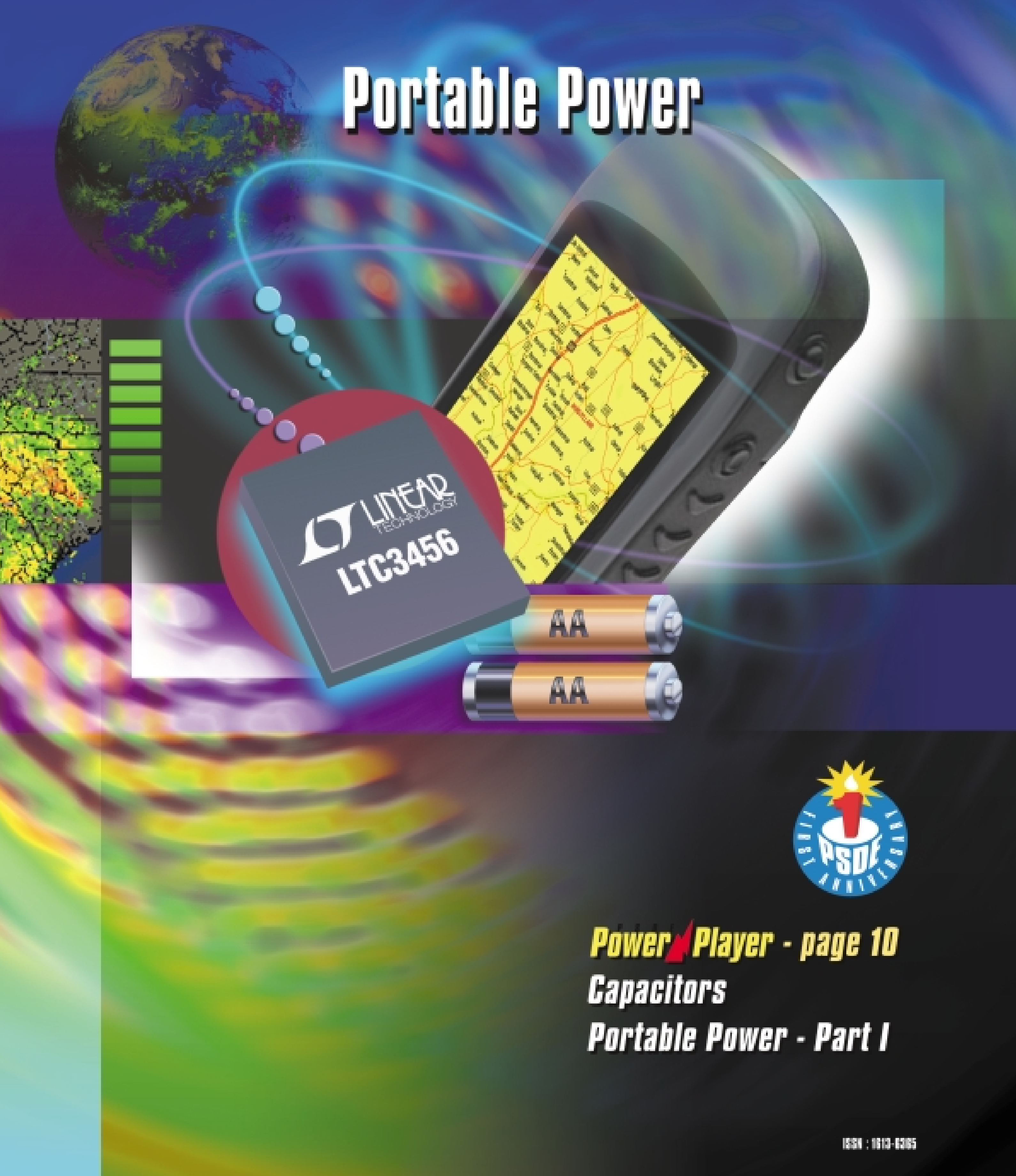
Power Control Intelligent Motion

January/February 2005

Portable Power



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Capacitors

Portable Power - Part I

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Industry News

Cover Story

PSDE Power Player

Features

Portable Power: Part I

New Products

Power Systems Design EUROPE

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Powering Up for 2005!

Our January/February issue celebrates our one year anniversary for Power Systems Design Europe. Looking back over 2004, we published 91 feature technical articles contributed by subject matter experts from the global power electronics and power management engineering community. Additionally our very popular "Power Player" column written each issue by one of our editorial steering committee members and "MarketWatch" written by isuppli Corporation gives you the reader further insight into the minds of those leading the power electronics niche and to insights and trends into different segments of the power industry.

As we began to get our stride, we launched the first of an ongoing Market Focus series with our mid-year Focus on Automotive, a two part series that was extremely popular and drew several request from around the world for article reprints of this series. It is still available for reading on our website: Go to: http://powersystemsdesign.com/automotive_electronics.htm.

This Market Focus continues in 2005, with the first of a two part series on Portable Power included within the pages of this issue. Part two on Portable Power concludes in our March issue. Watch these pages for further announcements on additional 2005 Market editorial.

Meanwhile 9,000 kilometers away from Central Europe the folks at ZM Communications & Messe München International are in the midst of planning the Fourth Annual PCIM China Conference & Exhibition in Shanghai, China to coincide with electronicaChina.

We were also planning—The launch this March of Power Systems Design China, www.powersystemsdesignchina.com, again to coincide with the PCIM China Conference & Exhibition and electronicaChina in Shanghai. Not only will we be exhibiting at the exhibition and distributing copies of the magazine to China's power electronics engineering professionals, we are the "Official Media Sponsor" of PCIM China and will carry their conference program within the pages of Power Systems Design China.

Published quarterly in 2005, and distributed to 10,000 power electronics and power management professionals, Power Systems Design China, joins Power Systems Design Europe as part of our growing circle of influence with the power electronics community, both print and online.

To support our expanding editorial influence on the power community, Liu Hong, former Editor of Electronic Products China Magazine, has joined our team as Chief Editor of Power Systems Design China. Working from Beijing, Liu Hong can be reached at: liu.hong@powersystemsdesignchina.com.

All along, we have had strong editorial contributions from Europe and North America. Now with Liu Hong as part of our team we will now have strong editorial contributions from the three most significant regions of the "electronics world", Europe, North America and China.

If your travels take you to exhibitions and conferences, don't forget to visit our booth at one of these upcoming trade events:

March 6-10, APEC (Applied Power Electronics Conference and Exhibition), Austin, Texas, USA

March 15-17, PCIM China, Shanghai, China

June 7-9, PCIM Europe,Nuremberg, Germany

As you can probably tell we have been very busy this past year making Power Systems Design Europe the market leader in delivering quality editorial to Europe's power electronics community. Our goal is to repeat this in China and bring all our readers an even better editorial package to your desk.

Bodo, Julia and I thank you for your loyal readership and promise to continue to deliver the quality publication you have come to expect from us.

Cheers!

Jim

Jim Graham
Publishing Director
Power Systems Design Europe & China
Jim@powersystemsdesign.com

Company Attains Certification For Wafer Fab Environmental Management System

Micrel announced that its wafer fabrication facility has been certified to ISO14001:1996, the International Environmental Management System Standard. The Company's certification was issued December 14, 2004, after an audit by TUV America. The goal of the environmental management system is to ensure regulatory compliance and to reduce environmental impact through waste reduction and recycling.

As one of the only domestic semiconductor manufacturers to maintain local state-of-the-art fabrication facilities, Micrel has focused on continuously improving its quality, safety and environmental practices. As a result, the Company has significantly reduced water and electrical consumption, saving significant operating funds as well as preserving the environment. Micrel's environmental initiatives have also resulted in the Company being recognized for its Environmental Management System by customers. For example, Micrel was awarded "Green Partner" status by Sony Corporation. To ensure compliance with the European directive on the restriction of use of hazardous substances (ROHS) and other similar regulations, Micrel is committed to providing customers lead-free products. Currently, the vast majority of Micrel products may be ordered in lead-free versions.

www.micrel.com

Dr. Gerald Paul New CEO of Vishay

Dr. Felix Zandman, Chairman of the Board and Chief Executive Officer of Vishay Intertechnology, Inc. (NYSE: VSH) announced that Dr. Gerald Paul, President and Chief Operating Officer (COO) of Vishay, will succeed him as Chief Executive Officer (CEO) of Vishay, effective January 1, 2005. Dr. Paul will also retain the position of COO. The change was approved today by the Vishay Board of Directors. Dr. Gerald Paul has served since 1987 in several management positions in Vishay, and was named President of Vishay in 1998. As President and COO, he has led the experienced management team that has successfully integrated the operations of acquired companies and businesses including, among others, BCcomponents, General Semiconductor, Siliconix and the former Telefunken business.

www.vishay.com

Danaher Buying LEM Instruments

Danaher reports that it has agreed to buy LEM Instruments, a division of Swiss-based LEM Group, for approximately $57 million in cash, including transaction costs and net of cash acquired. The acquisition is subject to applicable regulatory approvals and other closing conditions, it is expected to close in the first quarter of 2005. With its primary operations in Europe, LEM Instruments produces electrical measurement solutions used in commercial and industrial applications. The business generated fiscal 2004 revenues of approximately $45 million.

www.danaher.com

Green Power in Motion

Everyone is talking about "green" and among the hectic bustle the producers of appliances, systems and components affected by the EU guidelines RoHS and WEEE are trying to outdo each other. However, only a few companies are able to offer any lead-free or "green" products just yet – eighteen months ahead of the required start of the guidelines taking effect.

The urge to offer to the customer fast and dependable solutions regarding requirements arising from the EU guidelines RoHS and WEEE further extends the determined course. "Many of our customers are faced with the problem of having to make the guidelines happen within their products until the mid of next year. Thus we were able to present our first lead-free product family "easy" in September last year. With this eupec is way ahead of the date of effectiveness of the EU guideline from 1st July 2006", stresses the project manager for "green product" Dr. Thomas Licht. The products of the "easy" family are mostly applied in low power industrial drives as well as consumer drives such as fans, air conditioners and washing machines, and they have used lead-free solder joints for years.

The majority of the eupec products (high power) is utilized in electrical and electronic plant and systems to which the RoHS / WEEE guidelines do not apply. Notwithstanding, eupec will employ aspects of its "green products" strategy to these products as well. Here too the use of chrome-(VI)-free connection bolts and new plastic housings is planned.

eupec has defined a "green products" standard, which exceeds the requirements of the RoHS/WEEE guidelines.

www.eupec.com

PSMA and CPSS Form Alliance

Arnold Alderman (PSMA) and Zhanshi Li (CPSS) celebrate signing of joint agreement at meeting in Bejiing

The Power Sources Manufacturers Association (PSMA) and the China Power Supply Society (CPSS) announce that they have entered into a Cross Membership Agreement intended to foster collaboration and information exchange between the two organizations. The collaboration, as outlined in the mutual Letters of Invitation, provides each organization the opportunity to participate in the other's activities and committees. CPSS represents members from throughout the People's Republic of China while PSMA brings the international perspective having members in US, Europe and Asia. As part of the alliance, reciprocal Affiliate Membership will be afforded to each organization.

According to Arnold Alderman, Board Chairperson for PSMA, "PSMA believes it is very important to work with CPSS to the benefit of our industry. Our two organizations represent the majority of the power supply industry. We hope this agreement will nurture a better understanding between our members. All members of CPSS and PSMA are urged to participate fully in the opportunities afforded by this important cross membership agreement."

According to Ji Youzhang, Board Chairperson for CPSS, "Our two organizations, CPSS and PSMA are the most important in the power supply industry. This agreement will nurture a better understanding and cooperation between our members. It is very important to development the power supply industry. We hope CPSS and PSMA will have a successful cooperation in the future."

www.wb-power.com

www.psma.com

Direct to Engineers

Intusoft announced expansion to its "Customer Marketing Program," which connects customers and the engineering community to the company's marketing and technology teams. In Q4, 2004, Intusoft announced its ICAP/4 8.x.11 software release for analog, mixed-signal and mixed-systems simulation, which has spawned heightened interactivity between the company and SPICE end users. The unique customer marketing program comprises seven overall modalities:
1) Customer communication channel to marketing 2) Free custom modeling to the engineering community 3) Customer input stream to product requirement documents 4) End-user feedback surve 5) Software trial program 6) Competitive metrics for prospects 7) Technological outreach program.

Importantly, a direct email line to Intusoft's marketing director (rmktg@intusoft.com) has been added to the company's web site. This enables direct communication from the engineering community and Intusoft's customer base, regarding things like product success, feature and operability suggestions, and software applicability to real-world design. Combined with a direct phone number, the communication channel forms a focal point for customers who wish immediate status on a support issue, or insight on future product development. It's also valuable for sales prospects who need in-depth information on Intusoft's ICAP/4 simulation product line, including competitive product comparisons. An updated features matrix from popular SPICE vendors can be accessed from Intusoft's home web page at: http://www.intusoft.com/products/Compare.htm .

Further, Intusoft's outreach to the engineering community has grown to include several technology partners, some who OEM Intusoft's IsSpice4 technology. Sisoft was the latest OEM partner in 2004; SiSoft manufactures leading signal-integrity EDA tools. Other OEM partners include PADS and Mentor Graphics. ON Semiconductor, National Semiconductor, and Dr. Middlebrook (www.rdmiddlebrook.com) are technology partners with Intusoft.

www.intusoft.com

Power Events

- ***APEC 2005****, March 6-10, Austin, TX, www.apec-conf.org*
- ***EMV 2005****, March 15-17, Stuttgart, www.e-emc.com*
- ***PCIM China 2005****, March 15 – 17, Shanghai, www.pcimchina.com*
- ***PCIM 2005****, June 7-9, Nuremberg, www.pcim.de*
- ***SEMICON Europa 2005****, Munich, April 12-14 http://power.ti.com/mr*
- ***Texas Instruments 2005 European Power Supply Design Seminar Series*** *22 cities beginning April 4, information and registretion at http://power.ti.com/mr.*
- ***EPE 2005****, September 11-14 , Dresden, www.epe2005.com*

Three regional UK shows, www.seeds2005.co.uk:

- ***ScotEEDS2005****, March 8, Glasgow Conference Centre*
- ***SEEDS 2005****, March 22, Newbury Racecourse*
- ***NEEDS 2005****, April 5, Bolton Reebok Stadium*

Portable Power needs efficient Power Management

By Bodo Arlt, Power Systems Design Europe, Editor-in-Chief

Portable power has become common to our life. Mobility is what everybody is looking for. We all use portables and expect unlimited operation time with the supply. Modern technology for batteries and capacitors create solutions that match the requests for performance. Super capacitors in combination with batteries extend the energy recovery and therefore the operating time of the equipment. Maxwell and epcos are players that pushes capacitor technology for portable supply.

Power Management by chip and system level is a mandatory subject for electronics today. Sequencing supply voltages is a key element, Potentia Semiconductor is a new name doing simulation support by sequencing of power supplies. Others like TI are starting on chip level for sequencing or putting parts to sleep while not in functional demand. You can go from Linear Technology to National to Fairchild and Micrel, all of them and many others realize solutions where power management is key. In some it is the power supply taken from the LAN (local area network) better known as PoE (power over Ethernet). The control IC design is the basic element that makes it work. Most of the efficiency enhancements have been stimulated by device improvement both ICs and discretes. The electronic switches have become better and better in respect of conduction and switching losses. The most important switch is the MOSFET. It is also substituting the classical rectifiers by performing synchronous rectification.

The power conversion in DC/DC converters, the working horse for Power Management in Portable Power, receive the main contribution from MOSFETs, which in combination with optimized passive components demonstrates better than 90 percent efficiency, in some designs efficiency goes up to 95%. In these applications synchronous rectification with suitable MOSFETs andnecessary control replaces classical rectifiers by reducing the losses. The classic MOSFETs switch, has achieved improvement in silicon resulting into minimized switching - and conduction losses. The low voltage applications are benefiting from trench-gate technology, which has improved conduction characteristics. Parameters like avalanche capability in inductive switching is an important parameter to keep the device within the safe operating area. Active clamping is used to work successfully for a long time. Trench design has replaced the traditional V MOSFETs designs by offering more active area for the current flow per device size.

Automobiles are portables on wheels, you can get in it and get off where you want. MOSFET handling less than 200 volts continues to be the dominant switches in automotive applications. Starter alternator and drive by wire applications, will inspire more custom tailored devices for this volume market. All manufacturers have a full MOSFET product portfolio and future development will continue to support the automotive industry at the required voltage level. These volume markets communication, information and automotive will drive semiconductor innovation. ICs have moved to C-MOS technology for power consumption reasons like discrete MOSFET are cell or stripe structured devices that have moved step by step to more dense production technologies resulting into better device behavior. Bipolar still has some areas of interest, but the majority is MOS design. All of these achievements will guide us to more advanced solutions in the portable power arena of distributed power in systems. In power applications, the elimination of wire bonds is becoming a reality by using a solder process or pressure contact.

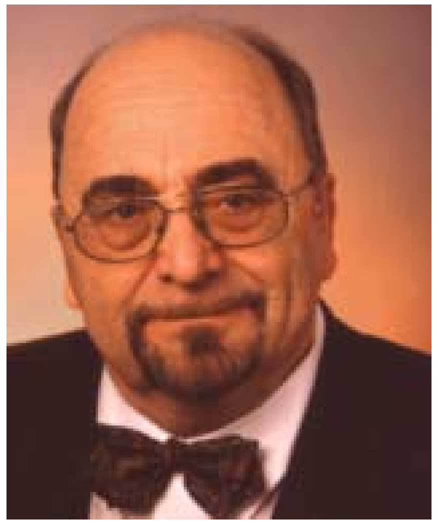
Schottky diodes will still be used in many low voltage applications as a result of their extremely low forward conduction drop. As I said earlier MOSFETs handling synchronous rectification took over a good portion of the Schottky market.

In conclusion for power semiconductors we can say that loss reduction and space minimization is achieved by MOSFETs offering extreme low on resistance. The control ICs to make the switch efficient has become the most important part of design now. These approaches have taken from various manufactures to offer solutions for application oriented specific power management. The solutions start on chip level and continue into systems level. Smart power solutions combining IC and switch on one chip is seen in the market. As the switch reaches a certain current level it is economical better placed as an external one. The total design is challenged to perform efficient. We have to include control ICs, passives like Capacitors and batteries, active switches and rectifiers to optimize the design by simulation tools. Only the total power systems design counts at the end on the test bench for efficiency. Portables are more sensitive as energy is limited by storage options.

Electronics Must be Intelligent and Energy-Efficient

By Rüdiger Bürkel, LEM

In European countries, the commercial sector including the retail and service industries is the largest consumer of energy. In 2000 in the EU, this sector consumed 951 billion kW, which corresponds to 37% of the entire energy consumption within the European Union.1 Consumption continues to increase, despite finite resources. In Germany, about 65% of the industrial energy consumption is converted into mechanical power (through electric motors). Numerous studies have shown that the use of optimised power electronics can significantly lower both energy consumption and costs.



Today, these objectives are achievable with modern electrical and electronic components. When the first silicone semi-conductor transistor was built about fifty years ago in the US, nobody could imagine the meteoric development of the semi-conductor technology in the fields of microelectronics as well as power electronics. Modern power components are designed similar to human beings, insofar as they have senses (in the form of sensors), a brain (in the form of signal electronics and logical components) and muscles (actuators).

The changeover from analogue to digital signalling and control electronics with microprocessors has brought many new possibilities as regards the useful linking of the above functions, which is also the objective of the development efforts in the field of power electronics.

For sensors, the most recent innovative developments concern the use of new materials for the miniaturisation of components and higher temperature resistance, combined with integrated electronic circuits (e.g. ASICs) in sensors and housings.

For four decades, the semi-conductor industry was the driving motor behind the entire industry. The development was sometimes very rapid, with slacker periods in between. After the boom at the end of the last millennium, the industry entered a period of recession, while the latest trend shows a steady growth.

Sustainability is based on sensible use of electric energy. Portable Power is one of the very critical areas. Powered by batteries or capacitors monitoring the status and extend the stand by time is a never ending story in design. We have to watch the primary energy too that charges all these portable tools from the cell-phone to electric vehicle.
The electric car is a portable solution that needs a lot of sense to have optimised performance.

The engineers are sensible in the use of electric energy and increased efficiency. To achieve this, they must reduce the power loss and thus lower the heat generation. These efforts have lead to smaller component parts with effective heat removal and hybrid designs with high packing density. The resulting higher power density leads to lower costs.

Many applications of power electronics require already intelligent components. Such assemblies are capable of measuring and evaluating data and of responding quickly and accurately, without compromising efficiency.

The market demands new products with more precise specs, while the product life cycles are becoming shorter and shorter. To remain competitive in such an environment, companies require highly motivated staff with excellent work efficiency. Companies must be able to identify potential markets in a global environment, and to turn their research achievements into innovative products.

What companies need are people with a vision who think outside the box, and decision-makers who are able to spot profitable innovative solutions without losing sight of what is technically possible.

The focus must be on users, who expect high-tech equipment with excellent support and service.

www.lem.com

Power Management ICs Simplify Designs

Two AA cell battery powered mobile devices

Hundreds of millions of battery-powered handheld devices will be manufactured in 2005. Makers of these products are under increasing pressure to pack more features into an ever-shrinking form factor while simultaneously gaining longer runtimes.

By Tony Armstrong; Product Marketing Manager, Linear Technology Corporation

It is easy to see how this increasing number of features is driving the need for more low voltage output rails at varying power levels. A good example of this is an applications processor for image processing, which needs up to 360mW of power during video capture. It is fairly common for over two watts of peak power to be required by a device's internal systems during full load operation. This type of power consumption can quickly drain a battery's energy. However, other important factors that adversely affect a battery's runtime are power supply efficiency and system power management.

In addition to Li-ion batteries, a variety of mobile handheld devices are being powered from two AA cell batteries (in NiMH or Alkaline chemistries), for both convenience and cost reasons. However, managing the flow of power into a handheld device is an increasingly complex task because of the presence of multiple power sources, multiple supply voltages within the product, demands for optimum efficiency and very limited space. It has been common for these factors to drive the development of highly integrated power management ICs, or an application specific standard product (ASSPs), for such high volume products as cell phones and digital still cameras (DSCs). However, there are also two AA cell battery-powered applications such as palmtop computers, MP3 players, and portable GPS receivers that also need to integrate high levels of power management into their designs.

One of the biggest obstacles when using a handheld device powered by either two AA cells and a 5V AC adapter or a 5V USB port, is being able to deliver both a fixed 3.3V output for the main power rail and a 1.xV output to power a microprocessor or DSP core voltage. Clearly, when the device is powered from either a 5V wall adapter or a 5V USB port, then only a step-down (buck) DC/DC conversion is needed. However, when the device is battery powered, a step-up (boost) DC/DC converter is needed to deliver the 3.3V required by the main power rail; whereas a step-down DC/DC converter is need to supply the 1.xV for the main digital processor. This is due to the fact that the discharge profile of two AA cells is 3.0V down to 1.6V (as seen in Figure 1).

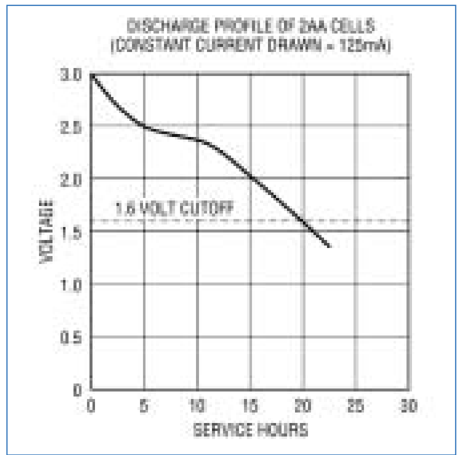


Figure 1. The Discharge Profile of Two AA Cells: 3.0V Down to 1.4V.

In reviewing the discharge profile of two AA cells from the graph in Figure 1, and assuming a constant current draw by the system of 125mA, up to 20 hours of run time is attainable.

Unique Approach

Linear Technology has a simple and effective solution to this issue with its LTC3456 two-cell, multi-output DC/DC converter with USB power manager. The chip brings together several functions that previously required three or more chips. The LTC3456 is a low profile, total power management solution that provides two regulated power supplies from any of three power sources: AC adapter, USB port or two-cell batter-

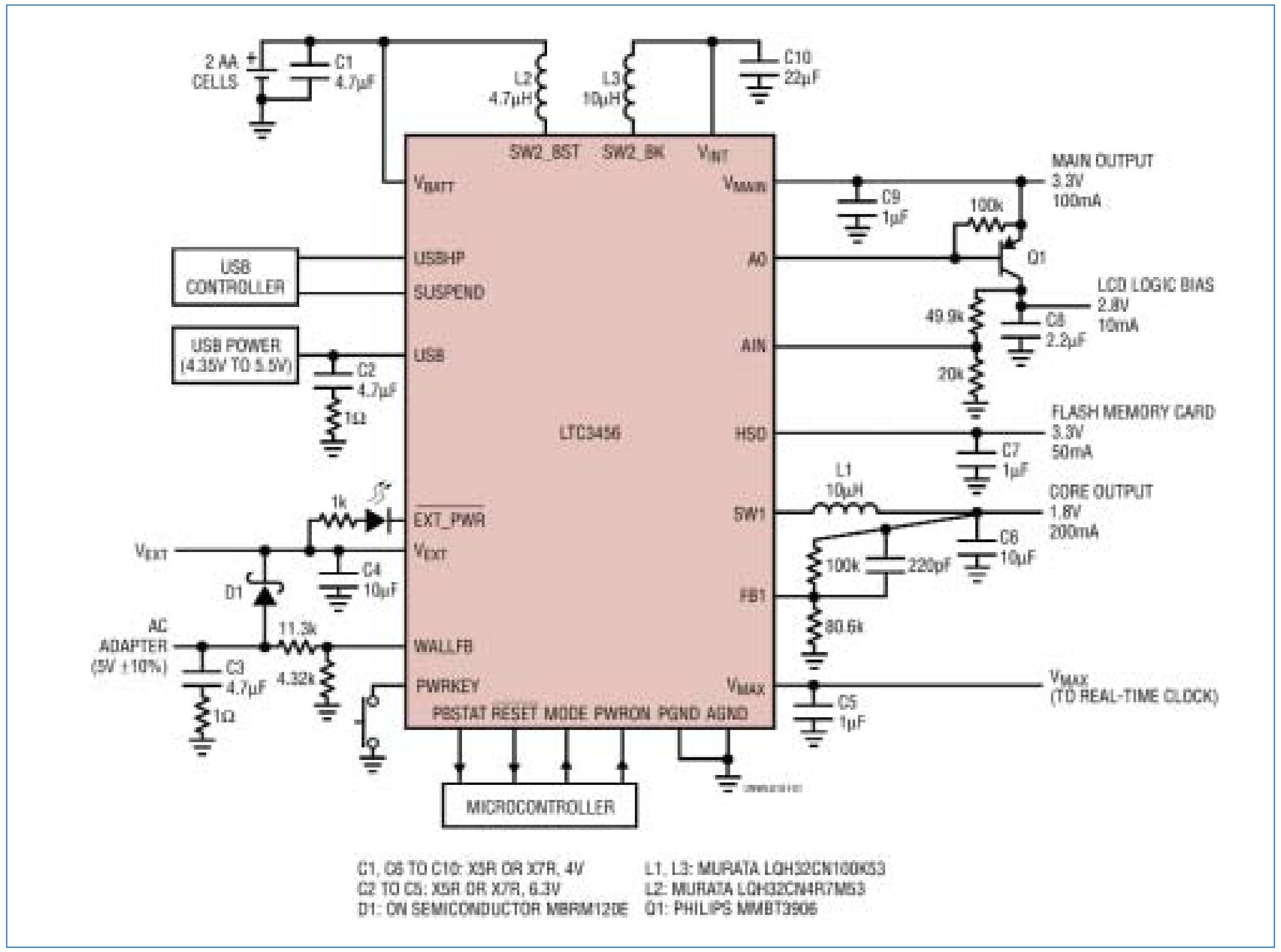


Figure 2. Complete Power Supply for Handheld Devices from Two AA Cells.

ies, in that order of priority. It can supply five outputs without additional devices, as shown in Figure 2.

The LTC3456 generates two separate power supplies: a Core supply for the processor and a Main supply for the peripheral circuitry. The Main supply is a fixed 3.3V output and the Core supply can be adjusted from 0.8V to the minimum battery voltage ($V_{BATT\ (MIN)}$). In addition, the IC provides a Hot Swap™ output which can be used for powering flash memory cards. Furthermore, it also incorporates a low-battery detector (which can also be configured as a low dropout regulator), USB power manager and several protection features that include all outputs being discharged to ground during shutdown. The LTC3456's control scheme allows 100% duty cycle operation for the core output. This provides low dropout operation when the core is powered from the battery source, thereby extending battery run time.

The internal switching regulators operating at a 1MHz constant frequency generate the two regulated supplies. This high switching frequency allows high efficiency and permits the use of tiny, low profile inductors and capacitors. These switchers are current mode PWM types with internal compensation that reduces pin and part counts. Furthermore, all power-path control and DC/DC conversion is squeezed into a single low profile 4mm x 4mm 24-pin QFN package, making the LTC3456 ideal for space sensitive portable devices.

Technical Hurdles and Theory of Operation

One of the key technical challenges in developing the LTC3456 was managing power-path control between the multiple supplies. Until now, system designers have been forced to implement this function with MOSFETs, op-amps and other discrete components. However such designs are plagued by hot plugging problems such as large inrush currents and voltage rail glitches, which can cause big system problems. The LTC3456 provides hot-plug protection for both the USB and wall adapter, while always using the best available input source for power.

When Battery Powered

The LTC3456 is designed to accept an input battery voltage range from 1.8V to 3.2V. This range is ideal for two-cell alkaline or NiMH designs. When enabled, the internal supply voltage V_{INT} (3.3V) is generated via a boost regulator. V_{INT} is used to power the bandgap reference, drivers and other internal circuitry. Core output (1.8V) comes up next via a buck regulator. The Main output (3.3V) and Hot Swap outputs are powered up with a delay of 512µs after the core output is in regulation.

When AC Wall Adapter Powered

The LTC3456 can be powered off an AC wall adapter. This input is usually connected via the V_{EXT} pin via a Schottky diode, D1 (see Figure 2). The status of the AC wall adapter power is monitored through the WALLFB pin. The nominal voltage at this pin is 1.25V. When the pin voltage is higher than 1.25V, the IC will draw power from the AC adapter via the V_{EXT} pin. The WALLFB voltage needs to always be kept below 2V.

When enabled, an onboard voltage detector checks the status of V_{EXT} voltage. If the V_{EXT} pin voltage is greater than 4V, the V_{INT}, Core output, Main output and Hot Swap output are all powered up in that sequence.

When USB Powered

The LTC3456 can also be powered from a USB port. It has an internal current-limited 0.6W (typical) PMOS switch with preset 0.1A and 0.5A current limits. The LTC3456 interfaces with the USB controller bus via logic pins USBHP and SUSPEND, as seen in Figure 2. The USBHP pin is used to set the USB current limit to either 100mA or 500mA. This pin has a weak pull-down current source to ensure that the Low Power mode is in effect during start-up. Pulling the SUSPEND pin logic high disables all USB functionality. In Suspend mode with PWRON low, the device limits the current drawn from the USB pin to 150µA.

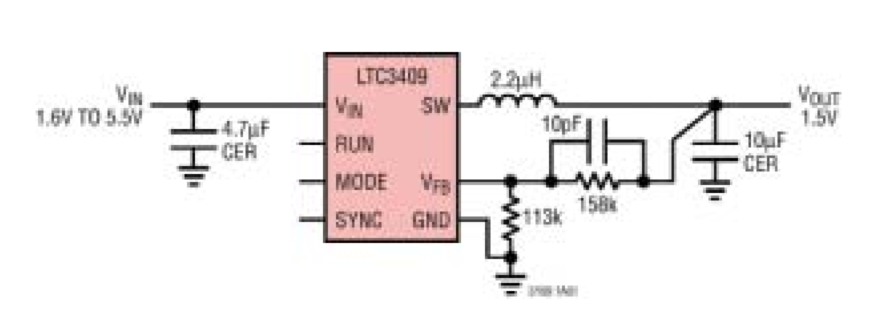


Figure 3. High Efficiency Step-down Converter using the LTC3409.

The minimum voltage to an USB-powered device may drop as low as 4.35V due to cable and connector drops. The LTC3456 has an internal voltage monitor that checks the USB supply voltage and cuts off the USB power if the USB voltage falls below 4.1V. There is 25mV of hysteresis built-in the USB voltage monitor When the IC is enabled, the USB pin is connected to the V_{EXT} pin via the PMOS switch. The V_{EXT} pin gets charged by the preset 0.1A or 05.A current limit determined by the state of the USBHP pin. As the V_{EXT} pin voltage rises above 4V, the V_{INT}, Core output, Main output and Hot Swap outputs power-up in that sequence.

The 'Building Block' approach as an alternative

It is clear that an ASSP approach to power management and conversion within a two cell AA battery powered mobile device, which can also be powered from a wall adapter or an USB port, is a straightforward means to deal with the complexities of selecting between multiple power sources. However, in some products this approach might be considered 'over-kill.' As an example, consider a two cell AA battery powered device that does not use an alternate power source, i.e. once the batteries are dead they are simply replaced with fresh ones. Such products are commonplace in both the medical and consumer markets. In these designs, a synchronous step-down converter to supply a low-voltage rail to deliver power to a digital processor core voltage and an efficient step-up converter to supply memory, I/O and other analog ICs are all that is required.

While this approach to power conversion appears relatively simple, having a synchronous step-down converter that operates down to 1.6V is not. This is due in large part to having sufficient gate drive at this low voltage level to fully enhance the on-chip MOSFETs. Nevertheless, Linear Technology has developed a 1.6V input capable synchronous step-down converter – the LTC3409.

The LTC3409 is a 600mA, high efficiency, monolithic synchronous step-down converter utilizing a constant frequency, current mode architecture. Fixed frequencies of 1.5MHz and 2.25MHz are supported in addition to an internal phase lock loop which will synchronize to an external clock in the frequency range of 1MHz to 3MHz. This range of switching frequencies allows the use of small surface mount inductors and capacitors.

Supply current during Burst Mode™ operation is only 60µA to 80µA, dropping to less than 1µA in shutdown. The 1.6V to 5.5V input voltage range makes the LTC3409 suited for single cell Li-Io, Li-Metal and two AA cell alkaline of NiMH battery powered applications. Figure 3 is an example of a high efficiency converter circuit using the LTC3409 to deliver 1.5V out at up to 600mA of output current with over 90% efficiency.

In addition, the LTC3409 has 100% duty cycle operation to provide low dropout operation which further extends battery run time. Burst Mode operation enables increased efficiency at light loads, further extending battery life. It is offered in a tiny 8-lead DFN package with dimensions of 3mm x 3mm x 0.75mm.

For step-up conversion requirements, Linear Technology offers the LTC3429–a high efficiency synchronous, boost DC/DC converter with true output load disconnect, inrush current limiting and soft-start in a low profile ThinSOT package. This device is capable of supplying 250mA from a two cell AA battery with a 3.3V output. A switching frequency of 500kHz minimizes overall solution footprint by allowing the use of tine, low profile inductors and ceramic capacitors. Current mode PWM control with internal compensation reduces external parts count thereby saving critical board real estate. The LTC3429 shifts automatically to power saving Burst Mode operation at light loads. Antiringing control circuitry reduces EMI concerns by damping the inductor in discontinuous mode.

The true output disconnect feature allows the output to be completely discharged in shutdown. It also limits the inrush current during start-up, minimizing surge currents seen by the input supply. The device also features a low shutdown current of under 1µA. Finally, it is offered in a tiny 6-lead ThinSOT package.

Summary

Despite the overwhelming trend to pack more and more features into mobile battery powered products, high performance ASSPs, from suppliers such as Linear Technology, provide system designers with a simple and cost effective means for the complex power management considerations of operating from multiple power sources. These modestly integrated ASSPs have small package footprints, require few external components and do not need software code. Furthermore, if the design architecture calls for a more simpler 'building block' approach, then Linear Technology also offers the right input voltage range in its converters to enable easy adoption.

tarmstrong@linear.com

www.linear.com

Electrochemical Capacitors as Energy Storage

The devices in automotive applications

To adapt capacitors to a use in power electronics and there, especially, in motor vehicles, both, the used materials and the mechanical construction of the components had to be developed accordingly. In the following article the construction and properties of single double layer capacitors and modules as well as their use in automobiles will be described.

By Dr. Andree Schwake and Dieter Hahn, epcos

Electric double layer capacitors use an effect that was found by the German scientist Helmholtz in the middle of the 19th century.

The electrodes have to be made of an electrochemically inert carbon. It is possible to use either powders that are mixed with a small amount of binding agent and afterwards and in the necessary layer thickness are put onto an aluminium foil with at least 99% aluminium content, or self-bearing carbon tissues which are coated on one side with aluminium and that are put with their covered side onto the aluminium foils that act as current collectors.

The base material that is used to manufacture the carbon is of essential importance for the long-term stability. Basically, you have the choice between synthetic materials as, for example Kynol, or natural materials as, for example, Rayon. Figure 1 shows the behaviour of 120F capacitors with electrodes based on Rayon or Kynol in a long-term test (rated voltage, 60°C).

In spite the fact that, at the same capacitor volume, a higher initial capacitance is achieved with Rayon, this material is not suitable for the use in double layer capacitors, as, after just a few weeks, the capacitance is reduced by more than 20% and the ESR is doubled.

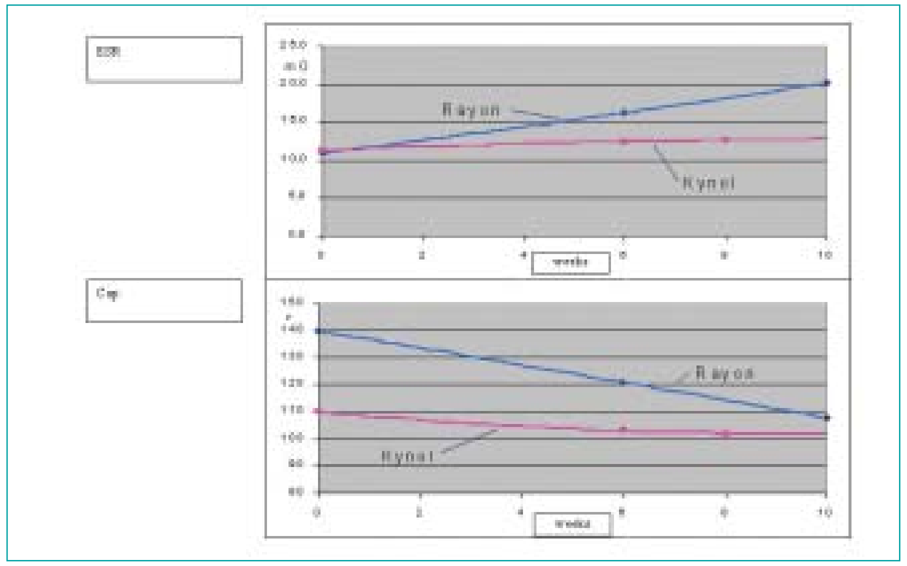


Figure 1. Changes in ESR- and capacitances of 120 F capacitors with different electrodes.

The electrolyte is produced by the use of solvents like Acetonitrile, Propylencarbonate or binary and/or ternary mixtures of carbonates in which conductive salts are solved such as Tetraethylammoniumtetrafluoroborate (TATFB) or Triethylmethylammonium-tetrafluoro-borate (MTATFB). In using

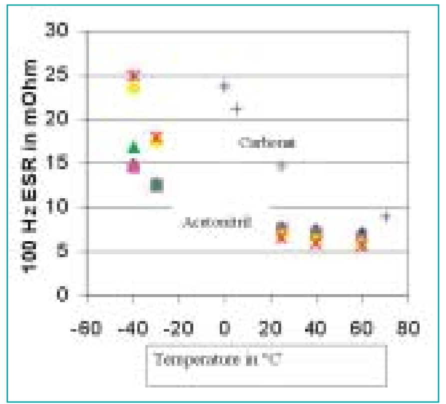


Figure 2. ESR – change as function of the temperature, the solvent and the concentration of the conductive salt γ = 1.6 to ν = 0.8 mol/l TATFB in Acetonitrile.

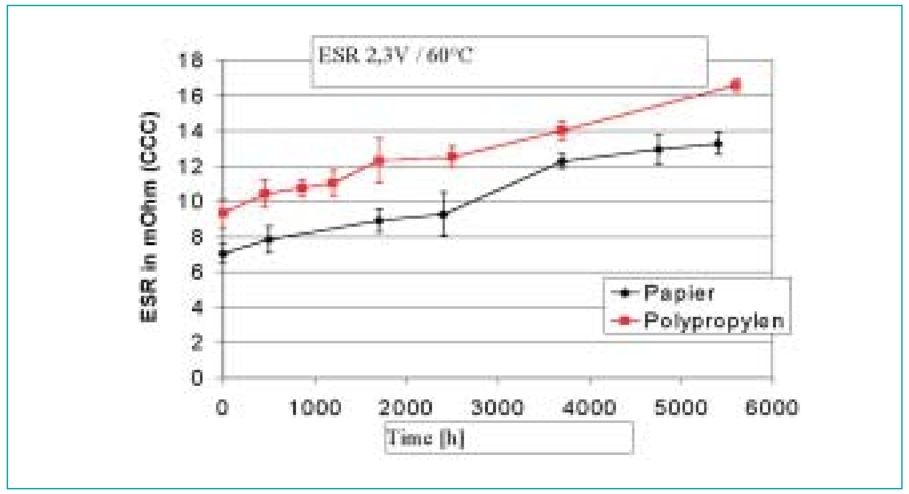


Figure 3. ESR changes of a 120 F capacitor with paper- and Polypropylen – separator.

the solvent Acetonitrile you will get the highest conductivities of up to 60mS/cm. But, on the other hand, in using other solvents, there will be only conductivities of 10 to 20mS/cm. As the carbonate's viscosity increase at lower temperatures is clearly higher than that of Acetonitrile and as, furthermore, the solvability of the salt decreases with decreasing temperatures, in this temperature range, the capacitor's ESR increases sometimes dramatically (see figure 2). We found an optimum temperature behaviour and long-term stability at a conductive salt concentration of 0.9mol/l TATFB in Acetonitrile.

To avoid that microscopically small carbon particles detach from the electrodes and attach to the separator and thus create small conductive paths there, in these capacitors, oriented Polypropylene (PP) films are used as separator. For reasons of cost-effectiveness, we tested the suitability of high-density papers on the basis of synthetic cellulose, too. Figure 3 shows the results of an appropriate long-term test at 60°C and at rated voltage for 120F capacitors. The use of paper separators decreased the ESR by approx. 10% and slowed-down the ESR increase. The higher porosity of paper which allows a larger amount of electrolyte to be stored in each separator volume unit might serve as an explanation for this effect.

A winding made of the above described materials is build into a metal housing made mainly made of Aluminium which is closed hermetically. In the housing, there is an opening for filling-in the electrolyte that is closed afterwards by means of a rivet. In order to minimize the number of parts and to achieve a contacting of the electrodes of lowest possible impedance, the electrode is directly welded to the housing into which the terminal is integrated. The other electrode, too, is welded-on by means of a terminal that is electrically insulated lead out of the lid.

According to the desired voltage, in modules, several single capacitors are circuited in series, for example, 6 for 14V, 12 for 24V, 18 for 42V and 90 for 220V. If, additionally, a high energy content is needed, it is possible to parallel 2 – 4 capacitors.

In accordance with the manufacturing tolerances, the single capacitors show slightly different capacitance-/ ESR values and self-discharging characteristics.

Due to the capacitance values that differ from the average and due to the different self-discharging characteristics of the capacitors circuited in series, single capacitors or even the whole module might be exposed to too high voltages when often charged and discharged. We therefore need measures to avoid this effect. These are either a

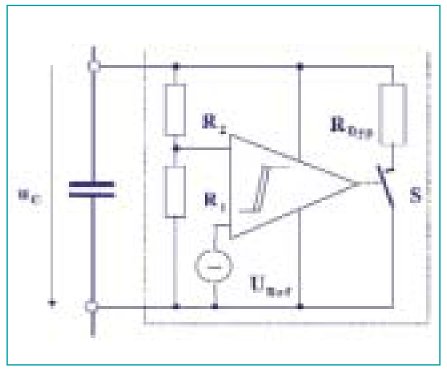


Figure 4. Cell balancing scheme.

net of resistors that are circuited in series parallel to the capacitors or an active unit balancing. Figure 4 schematically shows this balancing. It works like a switch. At, for example, a threshold voltage of 2.35V, a bypass of low impedance is opened. With this bypass, the single unit is discharged down to the threshold voltage.

Both, the module's electrical and thermal properties are of crucial importance for its use in the appropriate appliance. In case of frequent charging and decharging, due to the electric losses within the module, heat is created that has to be emitted to the environment.

The function of the cooling element is described in detail for a 150F/42V module (18x2700F circuited in series). For this module the thermal constant with and without a cooling element was determined. Due to the cooling element's

Figure 5. Module 30F / 220V for electric vehicles.

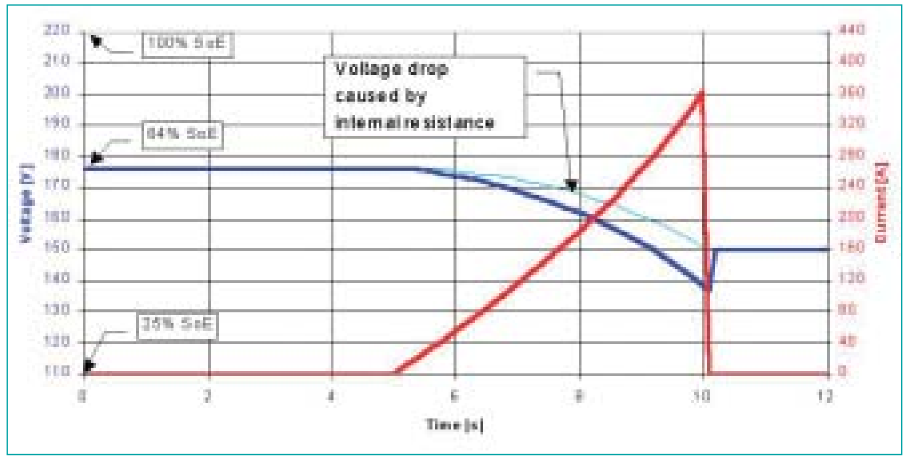


Figure 6. Current-/ voltage curve of the 30 F/220V module under stress.

mass, this module has a higher heat capacitance. This leads to a higher time constant of self-heating of the module.

As part of the EFRB (electric vehicle with extended range and higher acceleration) project promoted by the Federal Department for Economy, a car type Sprinter of the Daimler Chrysler AG was equipped with an electric drive. Here, a zinc-air battery with an energy content of 104kWh was used as energy storage device. This storage can emit a maximum electrical power of 46kW. With this power, the car weighing 3,500kg could just be accelerated very slowly. As the installed asynchronous motor could also be driven with a power of up to 100 kW, with an additional power storage device for acceleration, the car could be driven with much more comfort. Furthermore, the storage build of double-layer capacitors can store brake energy that is converted into electric energy and thus remarkably enlarge the vehicle's range.

The car is constructed as follows: A capacitor module that is operated between 110 and 220V is parallel connected to the battery by means of a DC/DC converter. During acceleration, additional electric power can thus be supplied by the module. In this module (figure 5), 90 capacitors with 2700F are circuited in series. It has got a volume of 86 litres and weighs 77kg. With an energy content of 202Wh, it is able to deliver an average power of 80kW for more than 5sec. Thanks to the materials used it is possible to run this module in a temperature range of –30 up to 70°C.

The module's energy content of 200Wh is by far enough as during acceleration only 35Wh are extracted. When braking the car, the whole electric energy of approx. 60Wh that was gained by changing the kinetic energy has to be stored in the module. So, the module should not be fully charged at the beginning of a ride. The running strategy of the car that sometimes takes energy out of the capacitor module takes this fact into account. This leads to a perceptible increase of the cars range especially when it is run in stop-and-go. This kind of operation is described in detail in figure 6.

The module's clamping voltage corresponds to the stored energy. With a clamping voltage of 175V the module is charged with 65%. During the above described acceleration process, voltage decreases from 175 to 140V while the current increases to 360A. Due to the module's internal resistance of 36m_, the clamping voltage increases by 10V after switching-off the current at the end of acceleration. The clamping voltage of 150V achieved at this moment corresponds to a stored energy of approx. 45%. As it is technically appropriate to run the capacitor-module only in the range between rated voltage and half of the rated voltage, on the one hand, in this example, there would be enough energy left for a second acceleration and, on the other hand, there would be enough free capacitance in the storage device to store the whole braking energy.

MAN reports about similar fuel savings of 15-20% for a diesel-electric bus that was equipped with a module of double-layer capacitors to recuperate the braking energy. Here, 288 capacitors with 2700F were circuited in series.

During the past years, remarkable advances have been achieved in the field of capacitors and construction of modules. Drastic decreases of the capacitor's and the module's inner resistances as well as a more efficient cooling of the modules allow perceptibly higher current impacts. A significant limitation for the use of these modules in automobiles has been overcome by reducing the allowed operation temperature to < -30°C.

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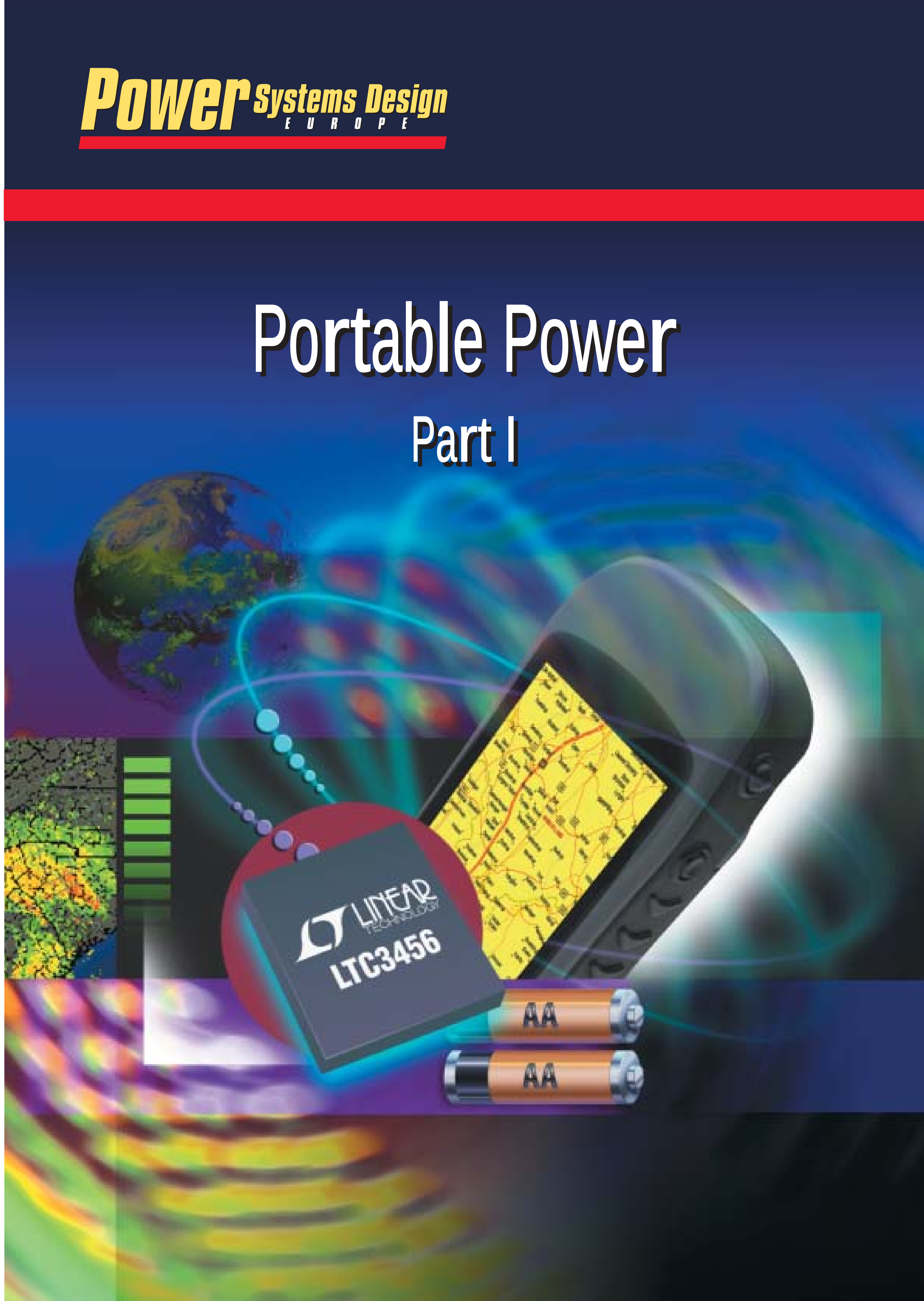

Flexible Dynamic Power Management Solution

Power consumption can be controlled during system operation

A key product differentiator in an embedded system is its power efficiency, because lower power results in lower operating costs, lower fan noise, and lower cooling requirements. Modern embedded systems therefore focus on increased system performance while reducing operating power consumption.

By Shyam Chandra, Analog Marketing Manager, Lattice Semiconductor Corporation

What is Dynamic Power Management?

Increasing the operating frequency, or using more powerful, higher density VLSI ICs—or both—achieves increased system performance, but increasing the performance level inevitably increases power consumption. One option to reduce system-level power consumption is to use low static power devices. Additionally, power consumption can be controlled during system operation depending upon the processing load. This latter approach is called Dynamic Power Management.

Methods Used to Control Power Consumption

Dynamic Power Management identifies low processing requirement periods and reduces operating voltage (voltage scaling) and frequency (frequency scaling), resulting in reduced average operating power consumption. Additionally, during these lean periods, idle sections of the circuit board also can be turned off to further reduce power consumption.

During system operation, the extent of voltage or frequency reduction from its maximum value is determined on-the-fly by software. This article describes a circuit that operates as a peripheral to this power management software.

Issues with Dynamic Power Management Methods:

There are a number of issues that a designer should be aware of when designing a system with dynamic power management capability.

1. Operating voltage & frequency scaling latency—Power supplies require a finite amount of time to ramp to the new operating voltage and this delay is usually a function of load on the power supply bus. But for the Clock generator, the time required to shift between frequencies can be very short. Therefore the operating system has to monitor the operating voltage and determine when the operating frequency should be changed.

2. Processors may not operate reliably during voltage or frequency transition—Many CPUs, capable of operating at different voltages and at corresponding frequencies, may not reliably operate when their power supply voltage or input clock frequency is changing. In such cases, it is advisable to halt the CPU during the voltage and frequency transition. This requires external hardware to monitor the voltage and clock frequency and prevent the CPU from execution during transition.

3. CPUs with integrated PLLs usually generate the required frequency for the integrated peripherals and also provide the clock for the external bus interface. If the CPU clock frequency were changed, the PLL would have to be reprogrammed to maintain operating frequency for the external peripherals, which are not designed to operate at different frequencies. CPUs with on-chip PLL may put the restriction on the range of frequency scaling. An external PLL can easily overcome this restriction and extend the range of power saving while also meeting the clocking requirements of other peripherals used on the circuit board.

Implementing Dynamic Power Management with ispPAC Power Manager and ispClock

Figure 1 shows the block diagram of a circuit board implementing the power management functions. The power management algorithm implemented in the software, and the Voltage Scaling and Frequency scaling unit implemented in hardware, together control overall board power consumption by:

1. Controlling the operating clock frequency of the CPU and the rest of the board circuitry.

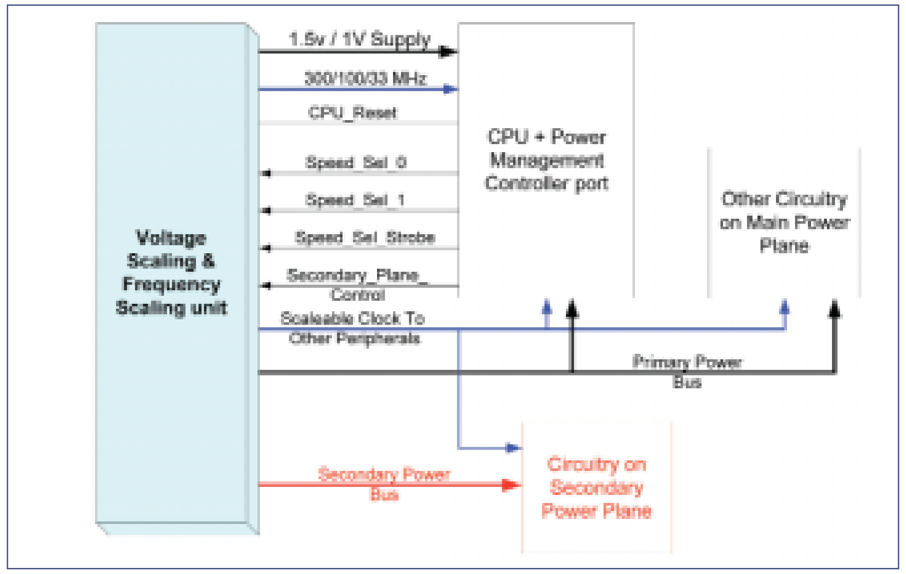

Figure 1. Block Diagram of Dynamic Power Management Implementation.

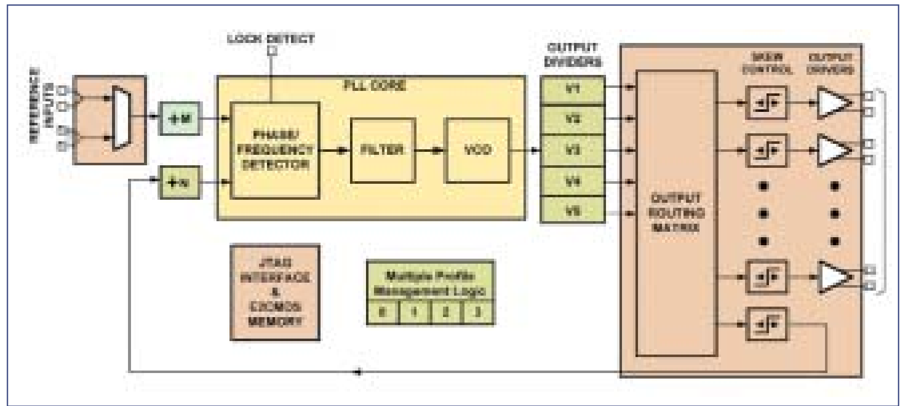

Figure 2. Block diagram of ispClock5520.

Table 1 lists various configuration values under different profiles

Profile	Input Clock	M Divider	N Divider	Vdivider in Feedback	PLL Operating Frequency	Output V-Divider	Output Frequency
00	100 MHz	1	3	2	600 MHz	2	300 MHz
01	100 MHz	1	3	2	600 MHz	6	100 MHz
10	100 MHz	1	3	2	600 MHz	18	33.33 MHz

2. Controlling the core supply voltage to the CPU.
3. Turning the circuit on the secondary power plane off during idle periods.

ispPAC Power Manager and ispClock5520 devices, from Lattice Semiconductor, together provide an extremely convenient mechanism to implement a wide range of Dynamic Power Management functionality.

ispClock5500 features:

The two members of the ispClock5500 family, the 10-output ispClock5510 and 20-output ispClock5520, combine a high- performance clock generator with a flexible, Universal Fan-out Buffer. The on-chip clock generator can provide up to 5 clock frequencies, ranging from 10MHz to 320MHz, using a high-performance PLL and clock multiply and divide facilities. The Universal Fan-out Buffer can drive up to 20 clock nets using either single-ended or differential signaling, with individual output control for improved signal and timing integrity. The devices provide an unprecedented level of performance and flexibility in support of high-performance clock network designs on electronic circuit boards.

Detailed Voltage and Frequency Scaling Circuit description:

Figure 3 shows the Power1208P1 (ispPAC-POWR1208P1) device, which provides all the logic for voltage and frequency scaling functions. It also drives the ispClock5520 device, taking Voltage transition and Frequency transition latencies into consideration and independently controls the secondary power supply plane following the command from the Power Management port. The ispClock5520 device generates the various clock frequencies required for frequency scaling. In total there are 20 clock outputs, which can be programmed to generate different clock frequencies for different sections of the circuit board.

Power1208P1 functions:

- Register and execute Commands from the Power management Control port
- Control Switching B1 supply Voltage between 1.0V and 1.5V
- Monitor all Power Supply Voltages
- Generate Control signals for ispClock to Switch between output frequencies
  - Profile select
  - Reset the ispClock device after Profile switch
  - Control Clock gating during Power Supply voltage variation and clock frequency switch over
- Turn-on primary power bus with tracking
- Secondary power bus control with tracking
- Pulse-stretch the CPU_Reset Signal during power on, and activate CPU_reset in case of power supply fault.

ispClock5520 functions:

Only three of the four profiles of ispClock are configured to generate different clock frequencies. While this article discusses only the change in frequency for the CPU, the same mechanism can also be applied to all the remaining clock outputs.

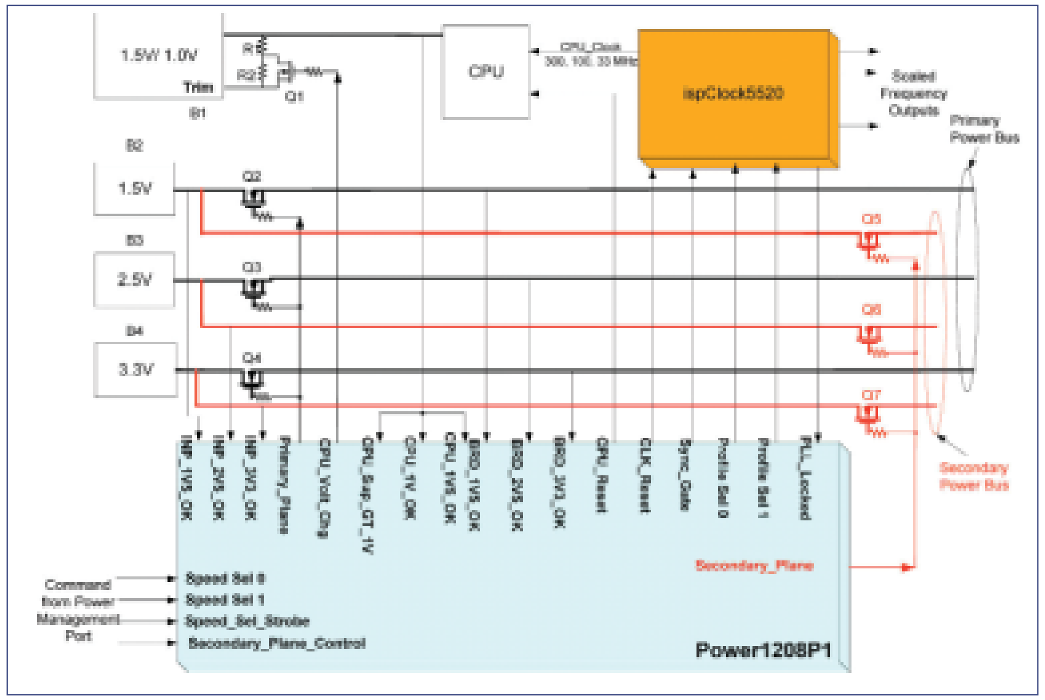

Figure 3. Voltage Scaling and Frequency Scaling Unit.

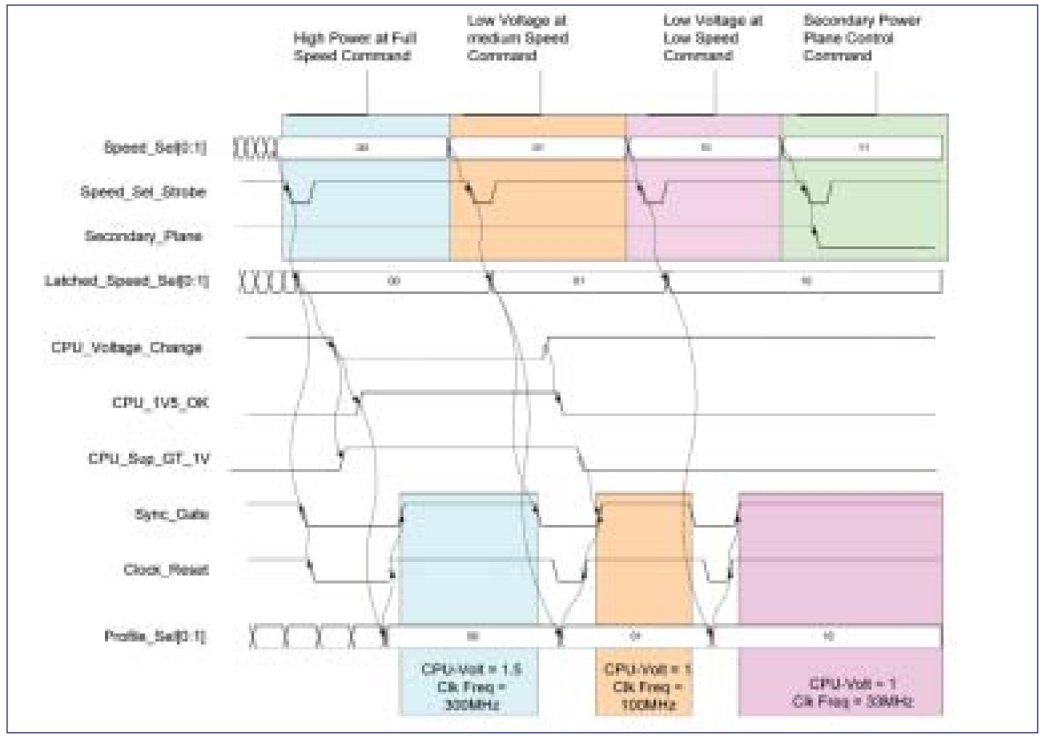

Figure 4. Operation of the circuit.

Circuit operation of power supply B1 - The output voltage of the power supply brick B1 on the top left side of Figure 3 can be set to 1.5 Volts by connecting resistor R1 + R2 between the trim pin and the output voltage pin. If only R1 is connected between the output and trim inputs, the output voltage will be at 1.0V. The MOSFET Q1, when turned on, shorts the resistor R2. This results in output voltage of B1 to transition to 1.0V. However, when the Q1 is turned off, the output voltage of the brick will transition to 1.5V. Controlling the ramp rate of HVOUT pin driving the MOSFET Q1 can limit the current inrush during the voltage transition from 1V to 1.5V and vice versa.

Timing Diagrams

The timing diagram in figure 4 shows the operation of the circuit above. The top section is the command from the Power Management Control Port. The Power1208P1 and the ispClock5520 devices execute the commands and the steady state is reached safely after the power supply voltage and the clock frequencies reach the steady state.

The design described above provides the most flexibility in the smallest circuit board area and can be adapted across a wide variety of designs.

Lattice's ispClock5520 device is ideally suited for the clock frequency scaling function, because it is able to replace four independent clock generator devices and the associated, expensive logic circuit required to multiplex various clock buffers to a single clock net. The resulting solution is flexible and high performance.

Lattice's Power1208P1 device used in this design combines the ability to monitor logic signals as well as power supply voltages. The logic section of this device is able to conveniently integrate all the logic functions required to reliably switch between different operating speeds, while controlling power supply voltages as well as monitoring the CPU voltage rail. The resulting design switches between configurations safely.

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Design Techniques for the Power Conscious

Best power savings by optimising architecture and systems

With electronic equipment mobility firmly embedded in the human psyche, performance at the lowest possible power cost is one of the key design issues facing electronics systems engineers.

By Giuseppe Martino, Accent

Naturally, the earlier in the design cycle power saving opportunities can be addressed, the better as, by the time designers get to the transistor level and can accurately measure power consumption, it is often too late for them to act without incurring huge cost.

With the design focus shifting, power awareness is no longer just a question of choosing the best cell library or supply voltage strategy, it involves more complex issues such as chip package dissipation capabilities and power requirements versus power supply trade-offs.

Essentially, there are three golden rules to follow. Firstly, it is important to ensure the choice of architecture for low power design is based on design exploration at the highest possible level. Secondly, the design team should be properly prepared and trained in terms of the necessary expertise in power sensitive design flows and power-driven synthesis. Thirdly, the choice of silicon vendor should be one with a wide mix of technologies, ASIC libraries and low power embedded memories.

While power-saving opportunities are available at every level of design abstraction from the top down to the physical implementation the best power savings are achieved by optimising architectural and system level strategies (see Fig. 1). Typically the impact at the architectural and system levels can be in the region of 10 to 100 fold (or even more) compared to just a two-fold saving at the circuit and gate level.

A review of potential power saving opportunities should begin at the application level with a detailed analysis of the functions the system is expected to perform and how it is likely to be exercised at the application level. The techniques employed to achieve this will be specific to the application and depend on the product. But once an analytical profile has been obtained, it should be possible to find ways to provide the same target functions at lower energy cost by altering the existing execution modes or by introducing new modes that execute the same job.

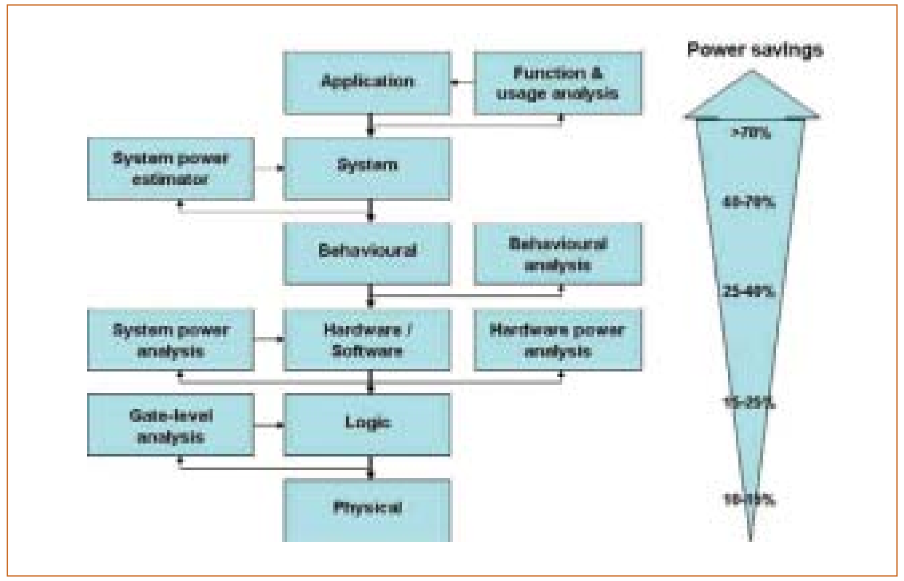
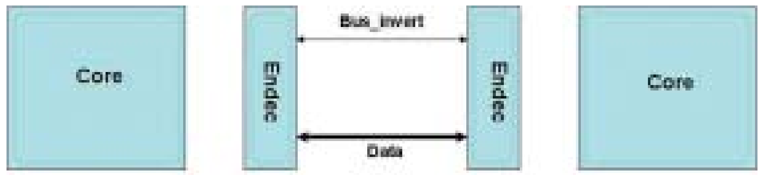


Figure 1. Power savings possible at different levels of abstraction.



Data	Bit transitions	Data plus bus_invert	Bit transitions
0000	-	0000 0	-
1111	4	0000 1	1
0000	4	0000 0	1
1111	4	0000 1	1

Figure 2. Bus-invert signalling and its effect on the number of transitions in a simple data sequence.

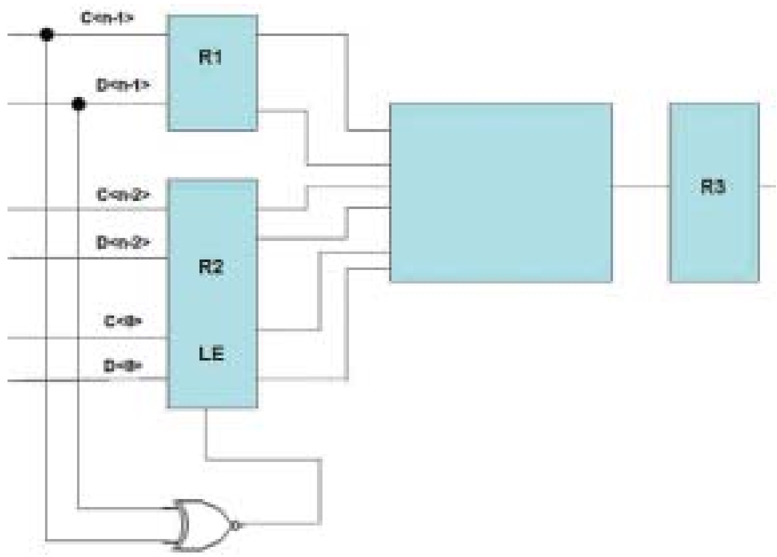


Figure 3. Use of computational kernel extraction to save power in a comparison function.

Significant power reductions can also be achieved by choosing the most appropriate IP and process technology. For example, the active power consumption of a commercial 32bit RISC processor core on a 130nm process can be 70% lower than its 180nm equivalent. But, of course, such a more introduces challenges in relation to complexity and cost that may simply prove great a hurdle to overcome. However, once the system has been partitioned into hardware and software elements, it will be possible to explore different implementations of each to determine the most power-efficient approach.

At the behavioural level, one highly effective power reduction technique is operating system-driven dynamic power and energy management. Circuits are generally designed to deliver peak performance but the systems they drive do not need it most of the time. In such cases, dynamic power management intervenes to cut power by turning off the clocks that feed the system, or even turning the local supply off, thus also eliminating the leakage power.

Today it's common practice to split the system into many independent power domains, to be able to turn off those portions of the system that are not active. A good trade-off between the granularity of such voltage islands and the extra effort and cost needed to implement them, and the savings due to the cut off of the leakage current, allows engineers to manage a variety of sleeping modes in the target device, and to significantly lengthen the battery lifetime.

For active circuits, dynamic energy management goes further by scaling the supply voltage to reduce the energy consumed per task when full-speed performance is not needed. The reduction in supply voltage will slow the circuit down to the point where 'just-in-time' computation is achieved.

This technique, so simple in theory, has a tremendous impact on the design complexity and the effort required, both at implementation level (e.g. technology libraries characterized at several voltage levels, EDA tools to implement the islands, for the cross-domain timing analysis etc), and at system level (software to safely and dynamically manage the voltage scaling).

An analysis of the power saving opportunities at the behavioural level involves the implementation of application specific computational kernels, such as algorithms. For example, the processing kernel of MPEG4, 2D/3D graphics, or of 802.11x technologies can be implemented in a multitude of ways. Some will support very high performance, others better power efficiency. Both software and hardware design play an important part in determining how power efficient an algorithm implementation will be. Optimising hardware for low power consumption at the behavioural level trades off factors such as parallelism against the core size, and the computation precision. Although parallelism increases the overall number of transistors in a core, it allows them to operate at a lower speed so that slower, less power-hungry cells can be used. The overall power saving can be as much as an order of magnitude if voltage scaling can be applied such that the hardware core is supplied with a voltage that is set at the minimum value that allows 'just in- time' computation.

Buses are amongst the most power-hungry elements in any system. This is due primarily to the capacitance effects of long, heavily loaded lines in a large SoC. Different encoding/access schemes will have different effects, so the right choice could help alleviate this. For example, bus-invert encoding is an adaptive technique that minimises the number of transitions needed to transmit two consecutive words on a data bus. An encoder analyses on the fly if it is more convenient to transmit the second word normally or in inverted form. An extra transition line flags the receiver if an inversion has occurred (see Fig. 2).

On a 130nm process, the encoding delay of such scheme for a 32bit bus is about 1.3ns, worst case. The encoding works well where the data appearing on the bus can be treated as effectively random. But there are cases where the data words are correlated, such as samples within a video stream when the colour variation between adjacent pixels in the image is small. By choosing an appropriate data representation it is possible to exploit the correlation and minimise transitions between consecutive samples. Effective encoding techniques for correlated data include two's complement and sign-and-magnitude codes on one side, and Gray, T0, Beach codes representations on another.

Memory accesses are also extremely power hungry. These can be reduced by looking for a perfect match between the data structures handled by the application software code and the memory organisation. Power consumption associated with data storage and data transfers can be addressed by a careful partitioning of the memory into a hierarchy of caches, into smaller physical banks and by optimising the data packet size in terms of burst size and data width.

Beyond the behavioural and architectural levels, both software and hardware design offer opportunities for power reduction.

From a software perspective, optimising the way the algorithm accesses memory make the biggest difference. Many compiler optimisations, for example, trade off processing speed against memory size. Similarly, there are several techniques that can be used at the source-code level to reduce power including the choice of data structures, such as arrays, lists or trees, and the avoidance of memory-to memory data copies.

At the structural hardware design level, power saving techniques typically include the use of resource sharing, glitch minimisation—to prevent the propagation of transitions through combinatorial gates—the extraction of computational kernels and pre-computation of values that will be used multiple times. For example, if downstream logic is driven by a magnitude comparison between two input data values coded on N bits, it is often not necessary to compare the full values. Most of the time, it may be sufficient just to compare the first one or two bits of each word to understand immediately which value is the larger (see Fig. 3). Designing the comparison logic to perform this operation first will yield a lower energy cost for the comparison.

EDA tools can be used to exploit power-driven synthesis when there is a need to handle legacy or third party IP. The behaviour and power consumption of each circuit type is extracted from functional simulations and passed to the synthesis tool. Power is then set as a constraint in addition to area and timing, so that the tool tries to build a circuit with a low power topology and map functions over standard cells with minimum power consumption.

As VDSM comes to the fore, leakage power is becoming a dominant feature designs as it can exceed dynamic power in certain temperature/supply voltage conditions. It can be reduced during synthesis by exploiting the silicon technology and the cell libraries with different transistor threshold voltages that processes at the 130nm node and beyond have introduced. High threshold transistors are slower but leak less than low threshold structures. So, a power-driven methodology should try to use low-leakage cells almost everywhere and isolate the use of high-speed and high-leakage, cells to timing critical paths.

Finally at the physical design level engineers need to be careful during implementation not to destroy all the benefits expected from the choices taken in prior phases. In addition to the challenges posed by the realization of multi voltage domains (operating at statically or dynamically different voltage levels), power-aware floorplanning and place-and- route techniques are essential. They use the placement of blocks such as phase-locked loops, memories and I/O pads to reduce wiring congestion and load capacitance of critical nets. Similarly, logic within the same clock domains needs to be grouped together to stay close to the clock gating and sleep-mode control logic that has been introduced during synthesis. A bottom-up flow, based on 'hard' macros, can help to keep both timing and power under control. Anyway 130nm, 90nm technology nodes and below show new VDSM effects like RC/Xtalk, voltage drop, and electro-migration (even on clock and signal nets) that make the task of engineers and tools (convergence of timing within power and area budget) ever more challenging.

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Programmable Power Management

Meets complex requirements for portable equipment

Portable power systems have become complex as many different devices with a myriad of voltage levels are powered off a single cell battery. In order to keep up with system changes and performance requirements, a programmable multiple output DC-DC PWM controller under digital control allows simple software modification of output voltage levels and sequencing requirements.

ByThomas DeLurio, Director, Applications Engineering and George Hall, Staff Applications Engineer, Summit Microelectronics

The proliferation of multi-voltage DSPs, FPGAs, CCD Imagers, TFT displays and other. applications created a need for a digitally programmable power management control function to meet the increasing stringent supply rail requirements placed on portable equipment (Figure1). In addition, all these devices need to be turned on/off at different times to power up or down for both reliability reasons and to conserve battery life. Device voltage levels for multi-voltage processors, DSPs and ASICs are down to 1.2V and are approaching 0.9V, making system tolerances tighter and necessitating a precise way to keep these voltage levels within specifications. If all these requirements are not followed, performance degradation, fault conditions such as bus contention or device latch-up can arise. Typically, DC-DC converters are specified to meet ±2% setpoint accuracy and ±3% over input voltage, loading and temperature conditions until end of life. A programmable 9-channel power supply PWM controller design is shown in Figure 2 exhibiting ±0.5% total accuracy with flexibility to design any system configuration. An I2C 2-wire serial bus is used for programming voltage levels and monitoring status.

A fully programmable power supply with integrated PWM controllers that monitors, margins, and cascade sequences provides all the power management needed in a portable power system. To provide a complete system, 9 voltage outputs plus reference, consisting of four synchronous PWM "buck" step-down converters, three PWM "boost" step-up converters, one PWM "boost-buck" negative DC/DC converter, and one LDO.

The power system is capable of power-on/off cascade sequencing where each channel can be assigned one of 8 sequence positions. Supplies may also be individually powered on/off through an I2C command or by assertion of one of two enable pins. Cascade sequencing, unlike time based sequencing, uses feedback to ensure that each output is valid before the next channel is enabled.

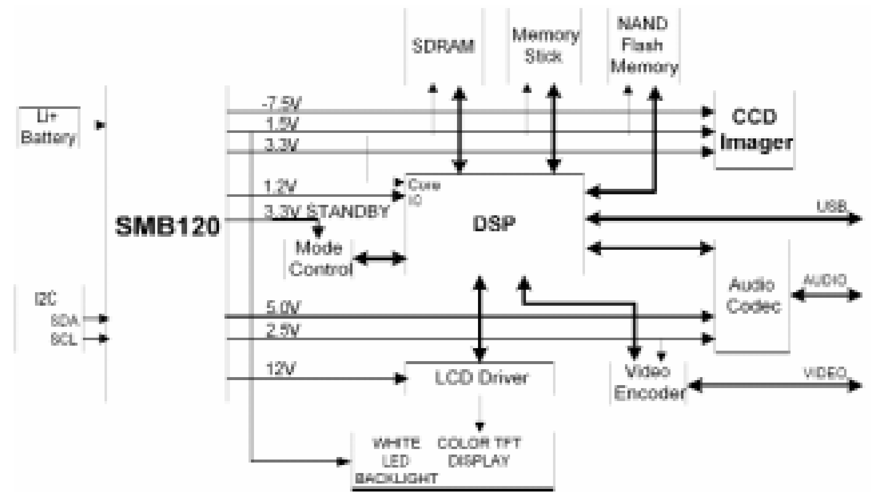

Figure 1. Power management block diagram shows the many different supplies and components in a typical portable system.

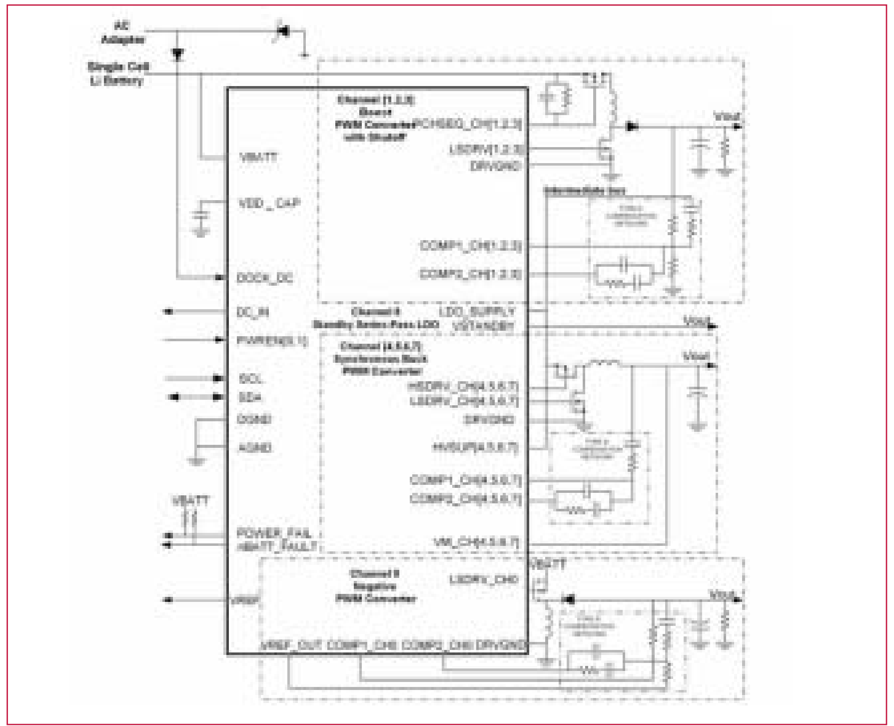

Figure 2. Typical application schematic showing external circuitry necessary to configure the SMB120 channels as: step-up, LDO, step-down, and inverting outputs, from top to bottom respectively. Furthering the concept of power control in a programmable PWM controller for portable embedded systems.

Each output voltage and the battery is monitored for under-voltage and over-voltage conditions. In the event of a fault, all supplies may be sequenced down or immediately disabled. Multiple output status pins are provided to notify host processors or other supervisory circuits of system faults. An Undervoltage Lockout (UVLO) circuit ensures the IC will not power up until the battery voltage has reached a safe operating voltage. The UVLO function exhibits hysteresis, ensuring that noise on the supply rail does not inadvertently cause faults on the internally regulated supply.

In the event of a system fault, all monitored supplies may trigger fault actions such as power-off, or force-shutdown operations. Each supply output may also be turned off individually at any point through an I2C command or by one of two programmable enable pins.

In portable applications powered from the main system battery, the battery voltage is continuously monitored for under-voltage conditions. There are two under-voltage settings for the battery; both are user programmable and have a corresponding status pin. When the first threshold level is reached, the POWER_FAIL pin is asserted and latched. When the second threshold level is reached on the main supply, the nBATT_FAULT pin is asserted.

Margining control over all of its output voltages through an I2C command can be changed by at least ±10% of the nominal output voltage. Margining creates three pre-programmed settings that each channel can be set to via an I2C command. Margining is ideal when used with a channel configured as an LED driver where margining provides three brightness settings. In addition, each output is slew rate limited by digital soft-start circuitry that is user programmable and requires no external capacitors.

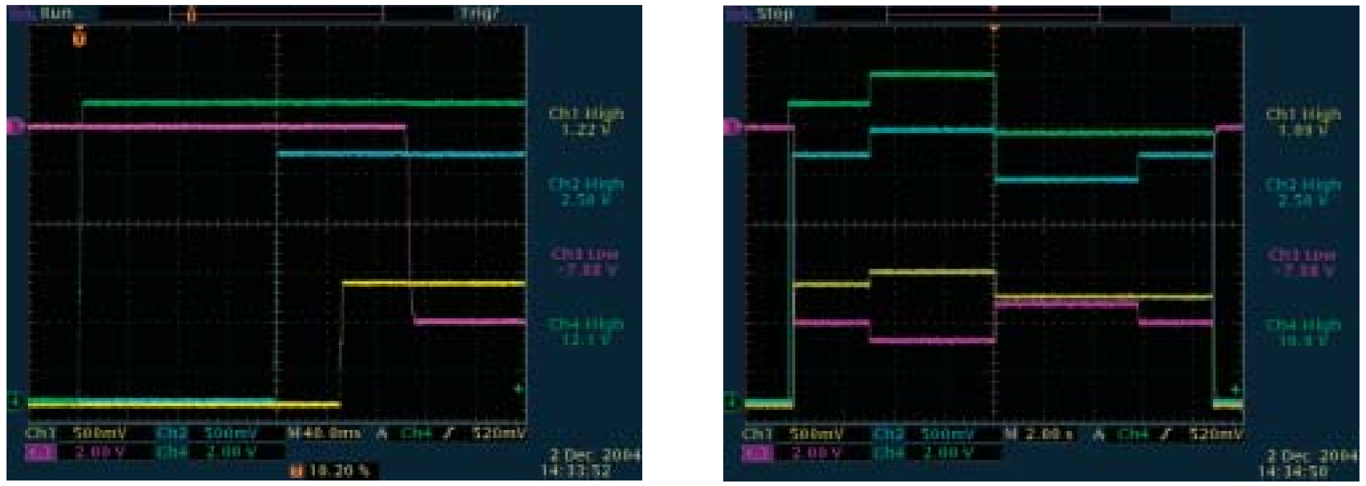

Figure 3. Power-on Cascade sequencing and Margin High/Low Waveforms. The supply channels are cascade sequenced-on to nominal voltage, margined high or low and then cascade sequenced-off. Channels 1, 2, 3, 4 are first margined high and then channels 2 and 3 are margined low. Up to 8 PWM supplies are controlled.
Ch 1 (500mV/D) = 1.25V Buck (Yellow trace) Ch 2 (500mV/D) = 2.5V Buck (Blue trace)
Ch 3 (2V/D) = -7.5V Inverting Buck-Boost (Purple trace) Ch 4 (2V/D) = 12V Boost (Purple trace)

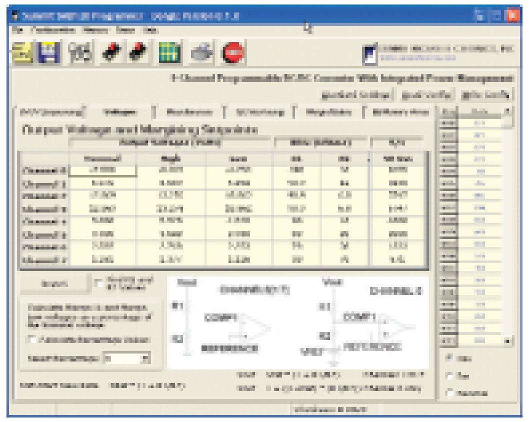

Figure 1. Power management blFigure 4 – Non-volatile Programmable Functions. All voltage, temperature levels and triggers are programmable using a Windows GUI and a PC-compatible parallel port to I2C serial bus programmer.

All programmable settings are stored in non-volatile registers and are easily accessed and modified over an industry standard I2C serial bus.

New digitally programmable power supplies provide I2C programmable output voltages, Power-on and -off sequencing, Individual channel enable control, Battery monitoring, UV and OV monitoring on PWM outputs, Margining, Slew rate control and Programmable power on/off sequencing. Actively controlling DC output voltage levels to within ±0.5% under low to high line/load to meet stringent tolerance requirements of high performance components further extends reliable operation and margining supplies tests system performance goals as well as providing an easy way to make adjustments, such as brightness and volume. The integration of active accuracy control, programmable features and built-in flexibility allows the system designer to create a "platform solution" that can be easily modified via software without major hardware changes. Combined with re-programmability, this facilitates rapid design cycles and the proliferation from a base design to future generations of product.

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The Evolution of Integrated Power Trains

Combining driver and MOSFETs in a single package

Complex electronic products can have a requirement for five or more separate voltage rails (e.g. 3.3V, 2.5V, 1.8V, 1.5, 1.3V, 1V, etc.) and would typically employ what is known as a Distributed Power Architecture (DPA).

By Dr. Phil Rutter, Technical Manager, Business Line Power Management, Philips Semiconductors

Moore's law, which embodies the technological leap that the semiconductor industry takes every 18 to 24 months, has two major consequences on the power delivery requirements of the ICs used in electronic products.

1). A rapidly increasing power requirement driven by the need for greater processing power and larger memory capacity

2). A proliferation of differing voltage requirements as the economics of the semiconductor industry dictate that not all ICs can be manufactured with the latest semiconductor processes.

Moore's law therefore infers an increase in the size and complexity of the power delivery solutions employed in electronic products. This is in direct conflict with the trends of increasing miniaturisation and ever-shorter time to market. The challenge for the power management industry is to combat the effects of Moore's law and provide solutions that are both easy to design with and physically small.

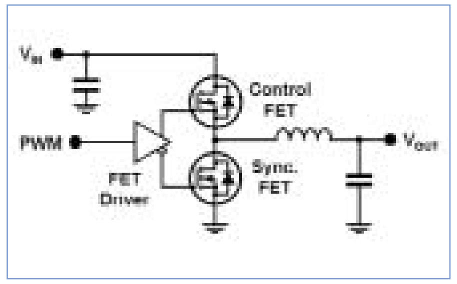

Figure 1. A single phase dc-dc buck converter used in POL applications.

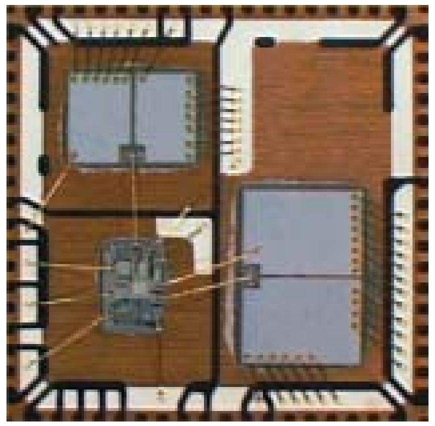

Figure 2. Internal construction of the PIP201, an integrated power train comprising of a driver IC and two MOSFETs in a half bridge configuration for dc-dc conversion.

Complex electronic products can have a requirement for five or more separate voltage rails (e.g. 3.3V, 2.5V, 1.8V, 1.5, 1.3V, 1V, etc.) and would typically employ what is known as a Distributed Power Architecture (DPA). Here, a single voltage (typically 12V) is distributed across the design to a number of Point Of Load (POL) dc-dc converters that convert the bus voltage to the required lower voltage exactly where it is needed. Each POL converter then needs to exhibit high conversion efficiency in order to limit rises in temperature associated with dissipating power in a small area. A POL converter is typically a single or multiphase synchronous buck converter. A single phase is shown in Figure 1 and consists of, a MOSFET driver that controls the switching of two MOSFETs (termed the Sync FET and the Control FET) connected in a half bridge configuration. The mid point of the two MOSFETs, or switch node, is connected to an inductor that provides the output voltage.

Significant improvements in the power MOSFETs have been made with the adoption of advanced silicon processes, such as TrenchMOS, and advanced packages such as LFPak. Consequently, further strides in efficiency require a detailed appreciation of the interaction of the power MOSFETs and the system in which they reside. This has lead to the introduction of a new type of product, commonly known as an integrated power train, that combines the two power MOSFETs and driver IC in a single package. Philips Semiconductor pioneered this type of product with the introduction of the PIP201-12M in 2001. Figure 2 shows the internal construction of the PIP201-12M, which has a footprint of just 10mm x 10mm.

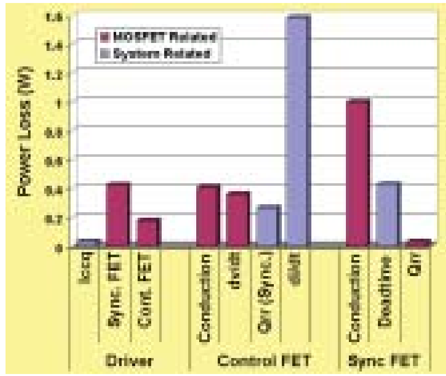

Figure 3. Breakdown of power loss of a discrete dc-dc converter using the PH2625L and PH6325L by Philips Semiconductors (Vin=12V, Vout=1.5V, Iout=20A, freq=500KHz). Half of the total loss is related to the interaction of the MOSFETs with the system rather than the actual MOSFET parameters.

The size and time to market advantages of integrated power trains are self-explanatory. The efficiency advantages however, are best explained by examining the sources of loss in a discrete solution [ref 1]. The Pareto shown in Figure 3 is a breakdown of the power losses of a discrete solution switching at 500KHz and an output current of 20A. The power losses in the Driver, Control FET, and Sync FET have been split into the main loss components and colour coded according to whether the loss is attributable to the power MOSFET silicon or to the system design as a whole.

The surprising aspect of this loss analysis is that the switching loss of the Control FET is not dominated by the fall/rise time of its Vds (referred to here as dv/dt loss and associated with the Qgd of the MOSFET) but by the rise/fall time of the drain current (referred to here as di/dt loss). The speed at which current can ramp up and down as a MOSFET turns on is limited by the package source inductance in the gate drive circuit. This dependence on source inductance on the di/dt of a switching MOSFET is demonstrated in Figure 4. It can be seen that advanced packages such as LFPak have significant advantages over traditional power packages such as DPak and D2Pak but an integrated solution can do much better. The combination of driver and MOSFETs in a single package allows the driver to be connected directly across the Control FET silicon ensuring that the source inductance plays no role in determining di/dt. In the PIP212-12M, the latest this approach doubles the di/dt compared to the best discrete package giving a current ramp rate of 6A/ns.

Combining driver and MOSFETs in a single package opens up many possibilities and degrees of freedom that are not feasible in a discrete implementation, which can either be used to improve conversion efficiency or increase functionality. A new generation of integrated power trains, such as the PIP212-12M from Philips Semiconductors, are exploiting these opportunities. The PIP212-12M includes over temperature protection, a fault flag, power sequencing features, external 5V supply for a PWM controller, and internal regulators to provide the optimum drive voltage for the MOSFETs. PIP212 also includes a novel technique for controlling the timing between switching on and off the two MOSFETs that relies on the accurate sensing of the voltage directly across the Sync FET silicon (which is not possible in a discrete solution). This technique allows for deadtime loss shown in Figure 3 to be virtually eliminated.

The system efficiencies of integrated power trains are far superior to discrete solutions that employ identical silicon

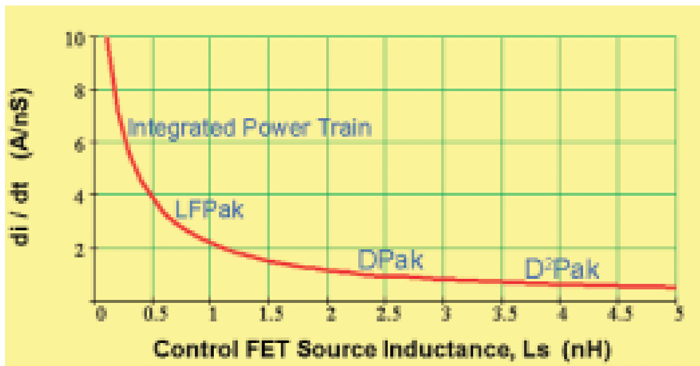

Figure 4. The effect of source inductance on the rate at which current can rise in a MOSFET as it is turned on. Whilst advanced packages, such as LFPak, give significant improvements over traditional power packages, the integration of MOSFETs and driver in a single package enables significant switching improvements by eliminating source inductance from the gate drive circuit.

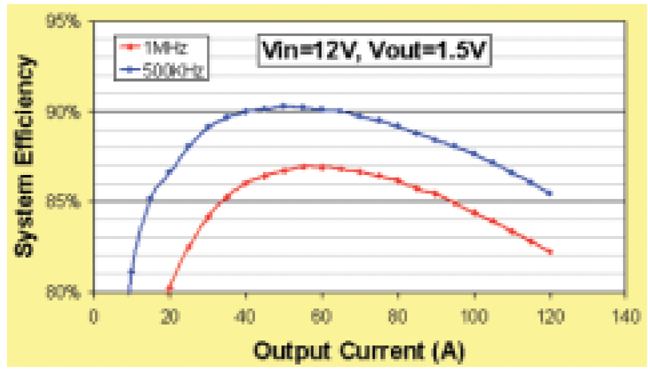

Figure 5. The system efficiency of the PIP212-12M, the latest integrated power train from Philips Semiconductors. Performance at a switching frequency of 1MHz is similar to leading discrete solutions using the same silicon technology but switching at 500KHz.

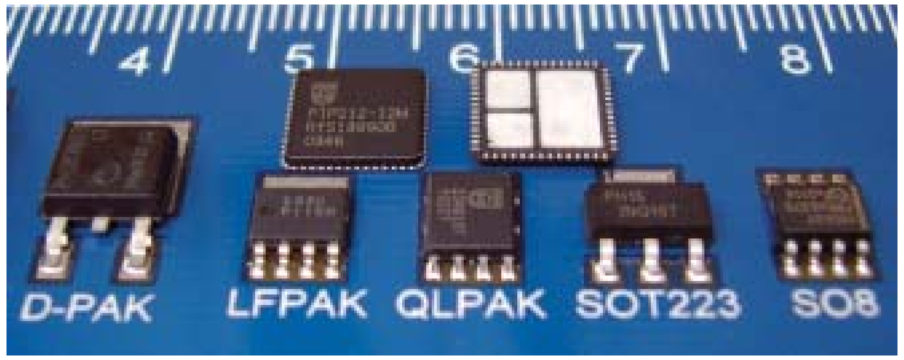

Figure 6: The PIP212-12M that contains two MOSFETs and a driver IC inside a compact 8mm x 8mm package (shown front and back) compared to discrete power packages.

By combining drive IC and power MOSFETs and taking a system approach to power loss a significant gain in performance can be achieved over discrete solutions.

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technology, typically reducing power dissipation by a third. Figure 5 shows the performance of a four phase PIP212-12M design. At 1MHz the performance is similar to leading discrete solutions running at a frequency of just 500KHz. When run at 500KHz system efficiencies of 90 percent can be achieved at an output current of 60A compared to 85 percent for a discrete solution.

This performance is achieved in an extremely compact area due to the small physical size of the PIP212 (8mm x 8mm) as shown in Figure 6. The footprint of the PIP212-12M is equivalent to that of a single DPak and consumes half the area of a comparable discrete LFPak design. The combination of high efficiency and small footprint results in a three fold improvement in power density.

In summary, Moores Law and market trends have created a conflict between complexity of the power demands of products and short time to market. This dilemma is being solved by power semiconductor companies, such as Philips Semiconductors, with the evolution of a class of products, known as Integrated Power Trains.

Bias Power Supply Solutions

Powering modern liquid crystal displays

Modern Liquid Crystal Displays require dedicated power supply circuits to support their specific requirements. Many different display technologies coexist in the market and compete for their market share.

By Oliver Nachbaur and Jeff Falin, Texas Instruments

While the passive matrix TN or STN (Super Twisted Nematic) LCDs require a fairly simple bias supply circuit, the active matrix displays using amorphous (a-Si) or low temperature polysilicon (LTPS) backplanes require a more sophisticated bias supply providing several power rails with power up and down sequencing. Not only the display technology but also the display's targeted end-equipment dictates different power supply requirements. In the past the LCD bias supply circuit was mainly built using discrete components. As the technologies mature, dedicated, fully integrated power supply ICs are available providing all the necessary features reducing overall solution size and cost. The difficulty comes in selecting the most appropriate LCD bias supply IC that supports the LCD technology as well as the end-equipment requirements. This is especially important when the LCD is used in portable equipments like mobile phones, pocket PCs or Laptop computers where efficiency and small solution size is a key feature. This paper discusses different LCD bias supply solutions and how integrated features relate to the specific system requirements for end-equipments like Pocket PCs or monitor LCD panels.

Single Boost converter powers Passive Matrix color STN displays:

Passive matrix displays are very suitable for portable equipment where high resolution and video imaging is not required. The black and white STN or color STN display achieves low total solution cost and requires in most cases only a single positive voltage rail in the 16V to 20V range depending on the display resolution and contrast ration. In order to adjust the display contrast, the LCD bias supply voltage needs to be adjusted to lower or higher values. The TPS61045, a typical inductive boost converter, is shown in Figure 1 and operates with up to 85% efficiency, making it ideal for portable systems.

Since the required output currents are only in the 20mA range, a small 3mm x 3mm QFN package with only a few small external components is usually sufficient.

Compared to other solutions, the converter in Figure 1 has input to output isolation due to a MOSFET switch being incorporated into the IC. Therefore, the input voltage is not connected to the output voltage during shutdown, which minimizes shutdown current and facilitates power-on sequencing. Additionally the TPS61045 has a simple digital interface which allows the output voltage to be programmed for adjusting the LCD contrast.

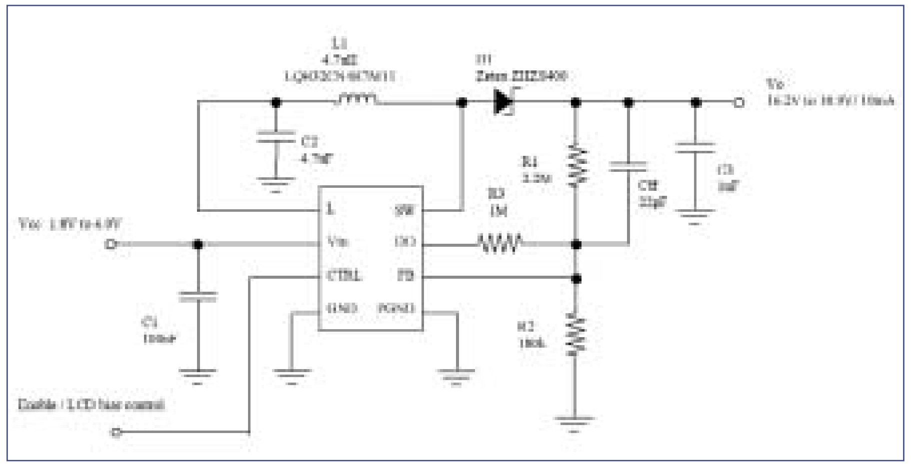

Figure 1. TPS61045 Simple boost converter in SOT23 package for passive matrix LCD.

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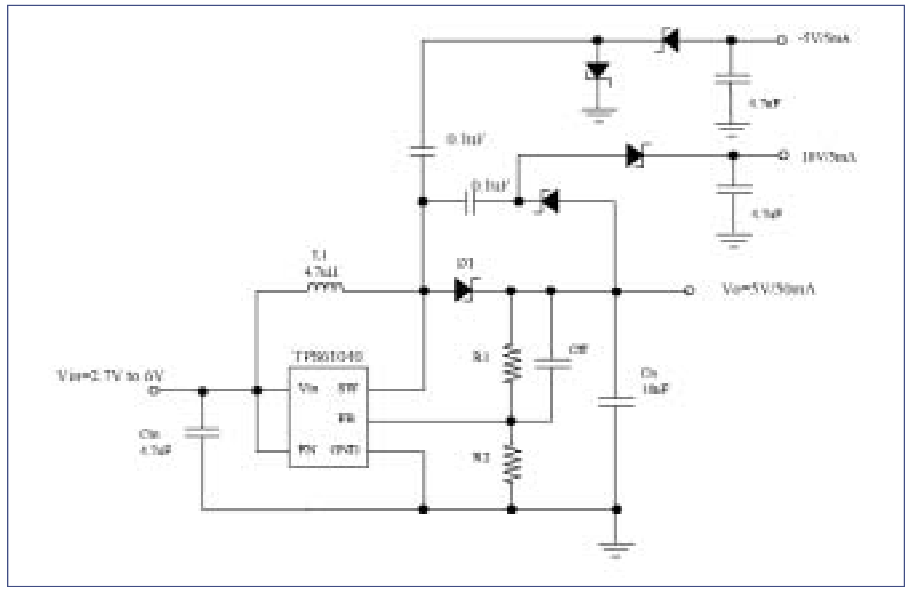

Figure 2. TPS61040 Simple application circuit providing active matrix LCD bias.

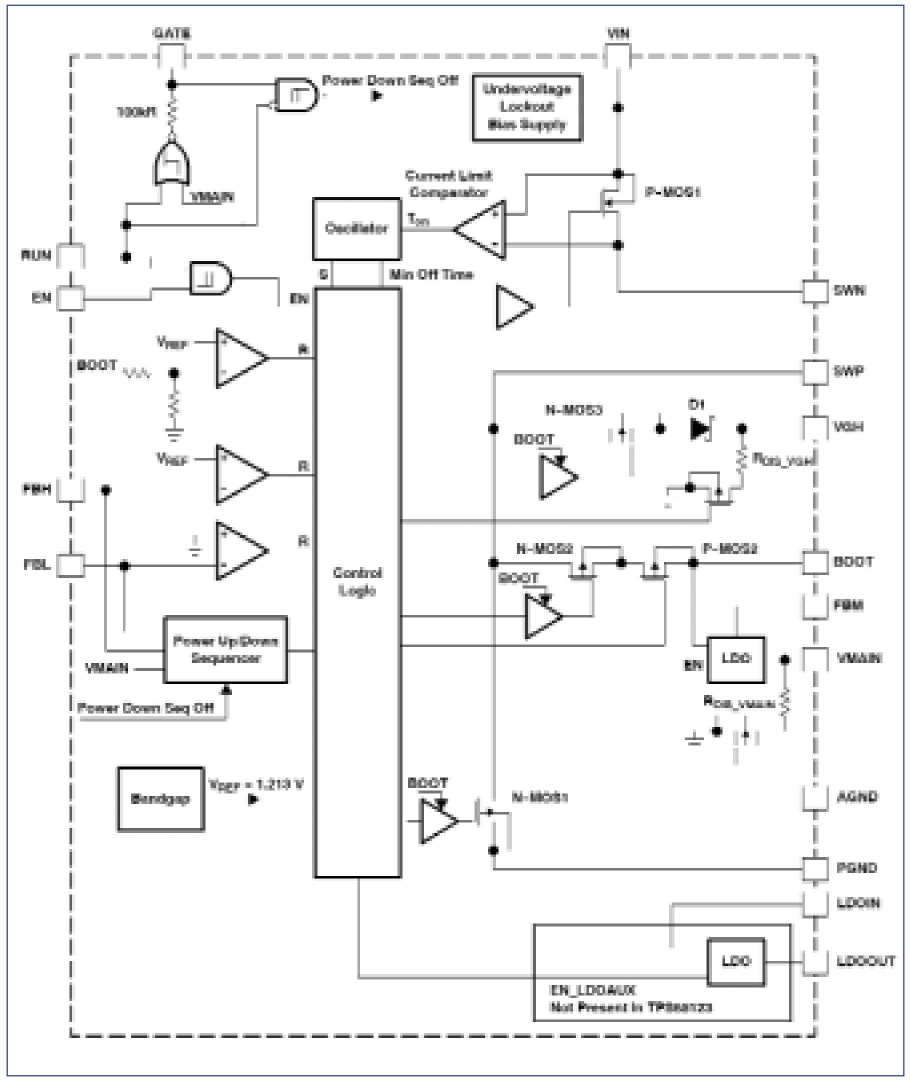

Figure 3. Single inductor solution providing 4 independent voltage rails.

a-Si or LTPS backplane process for active matrix LCDs:

Active matrix displays are used when higher resolution, fast response time and high contrast ratios is required. Therefore, LCD TVs, monitor, notebook and portable DVD application all use active matrix displays. While the mobile phone, pocket PC and PDA market was historically dominated by passive matrix black and white or color STN displays, today's trend consists of using full color active matrix TFT (Thin Film Transistor) displays.

For active matrix display backplanes, two technologies are being used. One technology uses the mature amorphous silicon TFT (a-Si TFT) process and the other technology uses the newer, low temperature polysilicon process (LTPS). The LTPS process with its higher electron mobility, smaller feature size and low power dissipation comes very close to the crystalline silicon process used in semiconductor ICs. Since the LTPS process allows the use of CMOS structures, the row and column drivers as well as other digital circuits are usually integrated on the same substrate as the TFT backplane. This makes the LTPS process ideal for the smaller displays used in mobile phones and PDAs. Since the LTPS process is still more expensive compared to the a-Si process, a LTPS process with integrated support circuits is not currently economical for larger panels above 7 inches. Therefore LCD panels greater than 7 inches usually use the amorphous silicon process with its lower electron mobility. Due to the lower electron mobility the bias supply voltages to turn the TFT gate on and off are much higher compared to the LTPS process.

Single IC provides all LCD bias voltage rails required by Pocket PC or mobile phone displays:

Since today's displays for mobile phones, pocket PCs or PDAs use active matrix TFT displays, the LCD bias supply circuit is more complex compared to that of a passive matrix display. The main difference between the passive matrix LCD bias solution and the active matrix solution is the positive and negative gate voltages that are needed to turn the TFT on and off. Both the LTPS or a-Si TFT backplane technologies require a high positive voltage to fully turn the TFT on and one negative voltage to fully turn the TFT gate off. The third voltage required is a positive voltage for the video signal applied to the column driver. Depending on the system, a logic supply voltage rail between 1.8V and 3.3V is also required for the graphic and timing controller (TCON). Such a LCD bias supply providing 3 or 4 supply rails with display specific power up sequencing can be realized with at least one boost converter and external Schottky diodes to build charge pumps. This barebones application is shown in Figure 2. The circuit of Figure 2 does not provide any application specific features such as sequencing for the voltage rails or an additional 3.3V logic rail. In fact, to provide sequencing or a separate 3.3 V logic rail, which could be disabled when the display is in power save mode, additional external transistors and passive components are required increasing circu it complexity.

In order to address the drawbacks of the circuit in Figure 2 and to optimize the design in terms of overall solution size and efficiency, Texas Instruments provides with the TPS65120, as shown in Figure 3, a fully integrated solution providing both sequencing of the voltage rails and a separate logic supply rail.

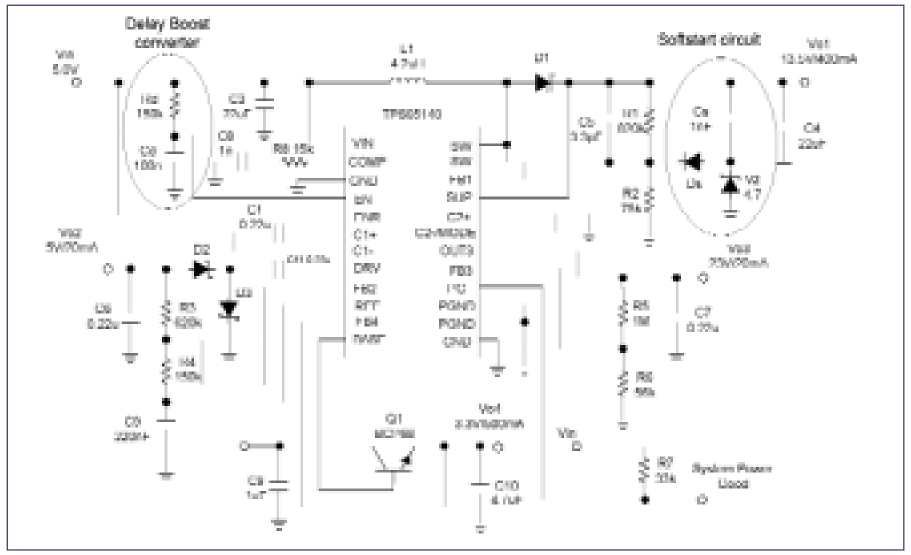

Figure 4. TPS65140 Integrated LCD bias supply increases system reliability and reduces cost.

The solution of Figure 3 operates with an input voltage from 2.5V to 5.5V ideally suited for Li-Ion batteries. The device provides the positive voltage V_{GH} up to 20V/2mA to turn the TFT on, the negative voltage V_{GL} down to –18V/2mA to turn the TFT off and the column driver voltage VMAIN, adjustable between 3.0V to 5.6V with 20mA load current. An integrated LDO derives a 3.3V logic supply rail from VMAIN to power the scaler or timing controller. Since efficiency and small solution size are key, the device comes in a 3mmx3mm QFN package and uses a novel peak current control architecture which time multiplexes the single inductor to serve each output with exactly the right amount of power required by the load. Depending on the different output voltages, efficiencies up to 85% can be achieved. Most of the displays require specific power up sequencing of the different rails to assure a controlled start-up of the LCD and to avoid damages or to avoid an uncontrolled display picture. Small LCDs require different sequencing depending on the display manufacturer used. Therefore the device family has options with automatic sequencing as well as manual sequencing of each output. The solution shown in Figure 3 provides sufficient output power for small displays that are used in mobile phones as well as larger displays used in portable DVD players up to 7 inches. As the panel size gets larger, such as the 14 inch and larger displays used in notebook and now desktop LCD monitors, the required power level increases as well as the LCD bias output voltage rails.

LCD bias supply circuits for notebook and monitor LCDs:

The large display TFT LCD bias solution is very similar to the small display solution presented in Figure 3 except that an inductive boost converter, capable of much larger switch currents, is required to provide the higher output power. Larger output power means a larger power solution but, fortunately, there is more board space available in notebook and monitor LCD panels than in pocket PCs and mobile phones. In addition, since TFT backplanes are dominated by the a-Si process with its lower electron mobility, larger voltage levels to turn the TFT on and off are required. Because the LCD monitor market is fairly cost driven, the benefits of a highly integrated solution, including improved system reliability and a reduction in assembly, placement, re-work and stocking costs to name a few, make a solution as shown in Figure 4 very attractive.

The TPS65140 IC from Figure 4 runs from an input voltage of 2.7-V to 5.8-V and provides the column driver voltage V_{O1} up to 15V, the positive voltage V_{O3} to turn the TFT on and the negative voltage V_{O2} to turn the TFT off plus a 3.3V logic supply voltage for the timing controller. With its typical switch current limit of 2.3A the device can also be used for LCD TV Panels. In the configuration of Figure 4, the 3.3V logic supply comes up first, followed by the column driver voltage V_{O1} set by a delay formed by RD and CD. Then the negative voltage rail V_{O2} and finally the positive voltage rail V_{O3} come up as controlled by the internal sequencing. The positive voltage rail is generated by a fully integrated and regulated charge pump, configurable as a voltage doubler or tripler. The negative voltage rail is generated by a regulated charge pump inverter. Both charge pumps are driven from the inductive boost converter that provides V_{O1}. Usually the LCD bias supply is assembled on the LCD panel and powered from a system rail coming from the notebook or monitor system PCB. To reduce overall system cost, the power supplies on the monitor or notebook system PCB are not over-designed in terms of output power or output current. Therefore high inrush currents caused by the LCD bias supply ICs are not desired. To minimize in-rush currents, an internal softstart circuit limits the inrush current. The device also comes in two current limit versions to allow customization of the solution to meet the exact power requirements as well as minimization of external inductor size. Because of the internally fixed softstart timing of the TPS65140 some applications might require a even longer softstart time for the main boost converter to further reduce in-rush current and to adjust sequencing. For such cases a simple external circuit as shown in Figure 4 can be added to extend the internally set softstart time. With this softstart solution, the feedback is held high during start-up reducing the maximum duty cycle. The diode D_S isolates the softstart circuit during normal operation. The zener diode is used to clamp the voltage on the feedback below its maximum allowable voltage.

In many LCD systems, direct gate drive is used and requires compensation for DC voltage shifts caused by the TFT gate line drivers. This is usually done by introducing a compensation voltage, V_{COM}, driving the LCD backplane. Since this voltage rail needs to sink and source current, a buffer or op-amp is used. Similar to the TPS65140, the TPS65100 family of ICs incorporates a V_{COM} buffer providing the overall smallest solution size in a 4mmx4mm QFN package or TSSOP package.

With the introduced LCD bias supply circuits, the user has the choice between a discrete solution, requiring several external components to implement required features, or highly integrated solutions containing application specific features. The fully integrated solutions not only reduce overall solution size, but they also increase system reliability and reduce overall system and assembly costs. Power IC manufacturers are continuously improving their application specific ICs. In fact, the LCD bias supply ICs currently in development will dramatically improve display quality by providing tighter output voltage accuracy, lower output voltage ripple, and a feature that reduces the effect of capacitive coupling within the LCD display by adjusting the fall time of the positive TFT gate voltage. Ultimately, manufacturers of electronics with LCD displays should be able to realize shorter design cycles when using more dedicated LCD bias supply ICs than discrete solutions.

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Bipolars challenge MOSFETs in Lithium Chargers

Bipolar transistors inherently provide reverse blocking

Today's portable electronics continually present designers with three key challenges—adding functionality, reducing size, and achieving longer operating times through effective power management. Because rechargeable lithium-ion is invariably the battery technology of choice for devices such as mobile phones, digital cameras, and PDAs.

By Simon Ramsdale, Product Marketing Manager, Zetex Semiconductors

The charger must also minimise charge time while maximising battery life. Typically, this system comprises an AC line adapter to supply regulated DC, and an onboard charger that's tuned to the battery characteristics of the mobile device. From a power dissipation and overall design viewpoint, the most critical element in the charger is often the semiconductor device that delivers current to the battery.

Being small and relatively simple, linear regulators often appear in onboard chargers—see figure 1. Their series-pass element must also provide reverse blocking to prevent the charger from discharging the cell in the absence of external power, as well as withstanding the voltage variations that accompany operation from an AC line adapter. This model serves to illustrate some of the key criteria in designing a lithium-ion battery charger, which has four phases to control—pre-charge, constant-current, constant-voltage, and top-up charge. Of these, the crucial maximum power dissipation occurs during the constant-current phase, as the series-pass element has full charging voltage across it while passing maximum current—see figure 2. Although the power level drops to a few hundred milliamps during the constant-voltage phase, this phase is the longest, when the pass element can still dissipate significant power.

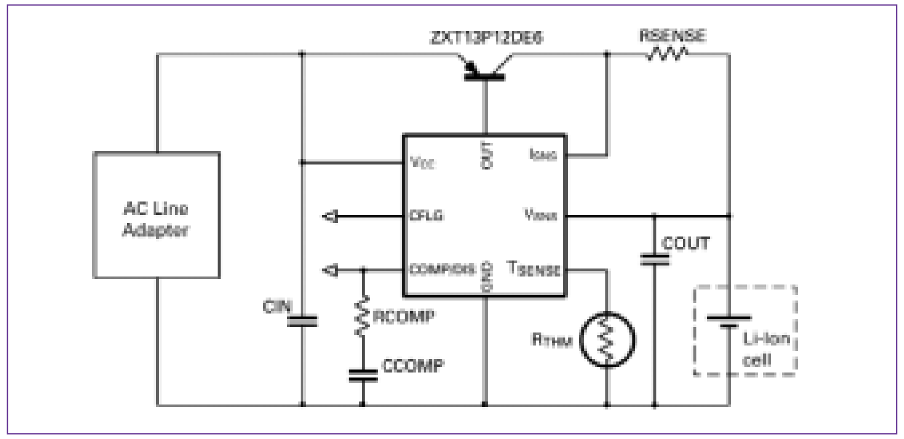

Figure 1. A linear regulator charger.

Here, the pass element could be a PNP bipolar transistor or a P-channel MOSFET (table 1 compares their major characteristics). But when size and cost are critical, high current-gain transistors often shine over the MOSFET competition. This is especially true at the low voltages that typify battery-powered operation, when the low gate-drive voltage inherently compromises a MOSFET's on-resistance performance. Because the series-pass element never saturates in normal linear regulator operation, one of the greatest perceived advantages that MOSFETs offer is not available. The need for additional circuit elements compounds the MOSFET's

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disadvantages in this application. Unlike MOSFETs, bipolar transistors inherently provide reverse blocking, and don't require an external Schottky diode or another device in back-to-back configuration—saving power.

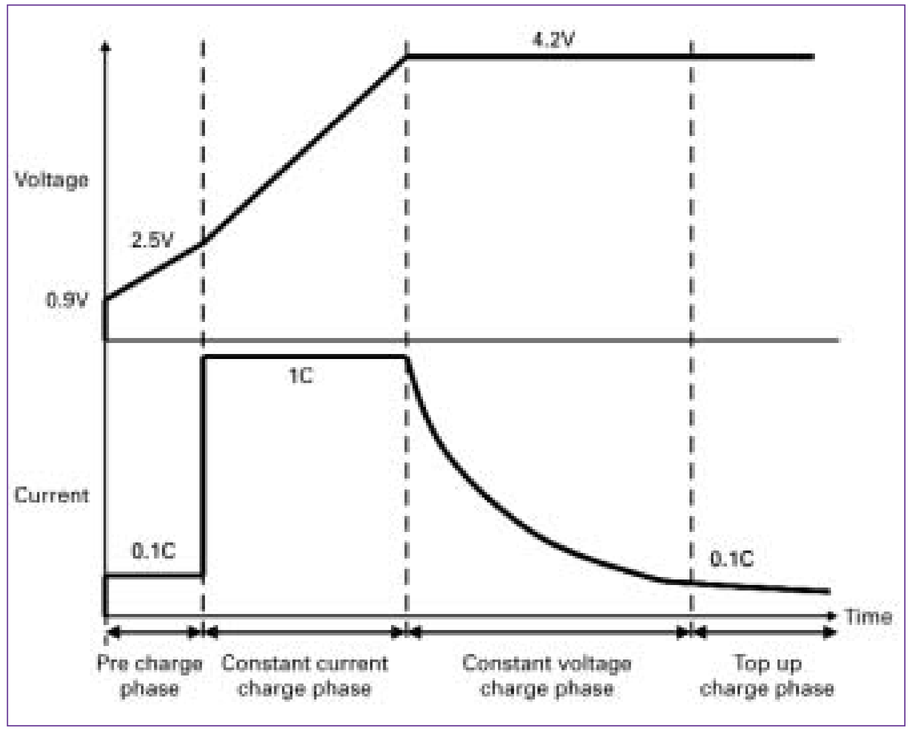

Figure 2. Charging cycle for a lithium ion cell.

Characteristic	Bipolar Transistor	MOSFET
On-resistance	Excellent: can be half that of the best MOSFET, depending on available base drive current	Good at full enhancement, moderate at low gate-drive levels
Blocking voltage	Bidirectional blocking capability, BV_{ces}, BV_{cev} or BV_{cbo} may be appropriate for some applications	Unidirectional, requires series Schottky diode or back-to-back MOSFET pair in some applications
Pulse Current	High	Moderate
Drive voltage	Less than 1V	1.8V to 10V, depending on optimisation
Temperature stability	Excellent: V_{be}: approx. 2mV per °C $R_{ce(sat)}$ approx. 0.4% per °C	Moderate: V_{th}: approx. 4 — 6mV per °C $R_{ds(on)}$ approx. 0.6% per °C
Drive Power	Moderate	DC: excellent; high frequency: moderate
Speed	Linear switch: very fast Saturated switch: moderate	Fast
ESD sensitivity	Very rugged	Sensitive
Price per area of silicon	Comparable	Comparable

Table 1. Comparison of major characteristics.

In practice, the power source must apply at least 4.7V to charge a lithium-ion cell from 3V to 4.2V. This overhead allows for losses in the series-pass element and current-sense resistor. Because a typical AC line adapter has a voltage tolerance of ±5%, the voltage across the pass element may exceed 1.9V at say, 0.6A for a 0.6A/hour cell. This >1W power dissipation remains constant for MOSFETs or bipolar transistors, with a bipolar device such as the ZXT13P12DE6 being able to dissipate 1.1W at 25°C in a SOT23-6 package. A MOSFET's need for a separate Schottky diode increases power dissipation by another 240mW.

In a switch-mode design, the pass elements act as switches and are on, off, or in an ideally negligible transition state. This architecture reduces power dissipation in the pass elements and can increase efficiency beyond 90% but increases complexity, size, and cost—see figure 3. Switch-mode operation significantly reduces the charger's dissipation variation with changes in source voltage, cell voltage, and charging current. It's then possible to increase the source voltage to >10V to minimise on-resistance in MOSFET switches due to better gate-enhancement. Most switch-mode charger ICs are intended to drive MOSFETs, with some using synchronous switching techniques to further increase efficiency. A separate reverse-blocking Schottky diode is still essential for the MOSFET circuit.

Pulse chargers substitute a fixed output current AC line adapter for the normal fixed-voltage supply. During the constant-current charging phase, the pass element applies the full source current to the cell. Because the line adapter adjusts its output voltage to match the load current and the pass element is saturated during this peak power phase, the pass element dissipates minimal power. This enables pulse chargers to deliver more current to a cell, charge larger capacity cells, or reduce the size of the pass element. With its intrinsic reverse-blocking capability and low collector-emitter (VCE) saturation, a bipolar transistor is optimal for this

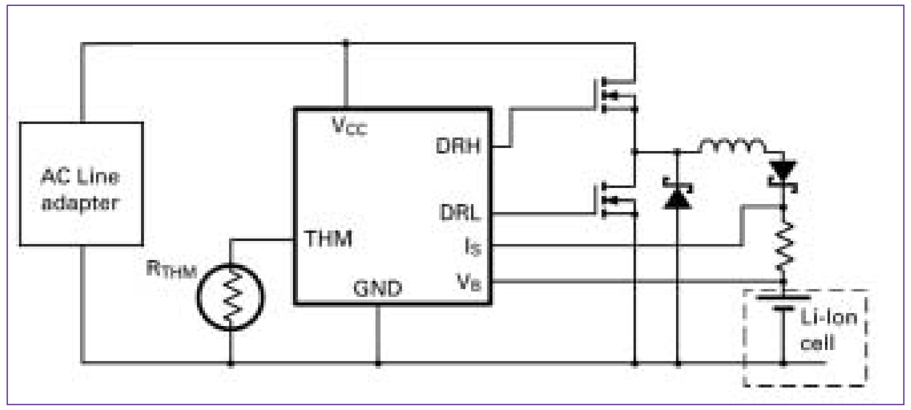

Figure 3. Switch mode charger.

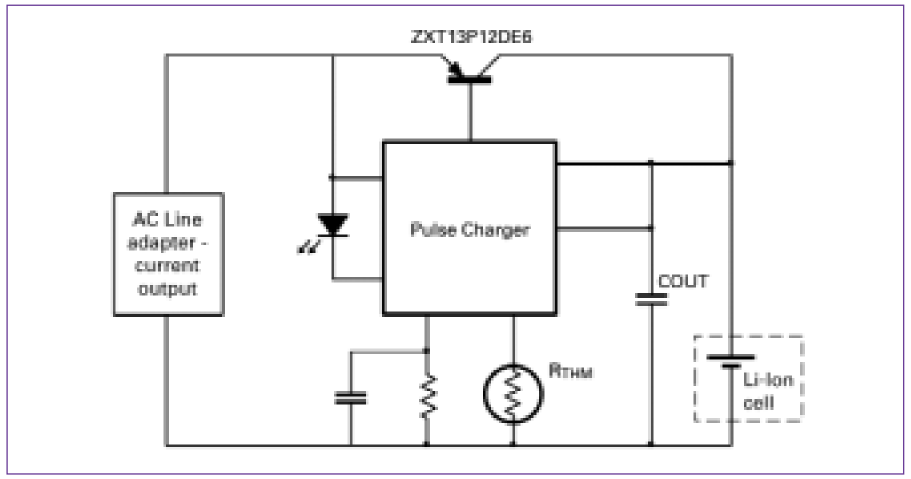

Figure 4. Pulse charger.

application—see figure 4. Here, the ZXT13P12DE6 has a typical VCE of 50mV at 600mA that constrains peak power dissipation to 30mW; a MOSFET design would dissipate another 200mW in the reverse-blocking Schottky diode.

Charging current accuracy is much less important for cell lifetime than the accuracy of final charging voltage during the constant-current phase. The circuit senses cell voltage and temperature during this phase and when the cell voltage reaches 4.2V, the charger switches to pulse mode. Now in the constant-voltage phase, the circuit applies current pulses that result in an exponential decay in the average current that the cell receives. The pass element is either on or off, greatly reducing its power dissipation. It's essential to monitor the cell voltage during and after the current pulses to ensure that the final value lies within 1% of its target. This phase continues until the charging current decays to a predetermined level, or a fixed time elapses. Charging then either ceases, or switches to an extended cycle-skipping top-up mode.

The greatest challenge that linear chargers present is the handling the peak power dissipation in the pass element while minimising PCB area. Here, bipolar transistors with their inherent reverse-blocking abilities provide cost and power savings over MOSFET-based solutions.

Switch-mode chargers greatly reduce the overall power dissipation but increase cost and PCB area. Driver ICs typically specify MOSFETs as the pass element. The increase in cost, PCB area, and complexity lends switch-mode designs to high-power, less cost-sensitive applications.

Pulse chargers also constrain overall power dissipation, but without incurring a switch-mode design's complexity. These characteristics suit use in portable electronics that need to handle significant current levels within ever decreasing PCB areas. Pass-element saturation losses dominate power dissipation, which the series Schottky diode that MOSFET-based solutions require can swamp. As a result, bipolar transistors are clearly the devices of choice for this application.

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NEW PRODUCTS

Mini but mighty

Packing maximum performance into a mini package is something NEC Electronics excels at. The recently launched series of new PowerMOSFET devices is yet another example. Based on the outstanding UMOS-4 technology with 0.25 µm design rule, these devices come in the new 6pinWSOF package and are targeted especially at portable power applications where size and performance are both critical.

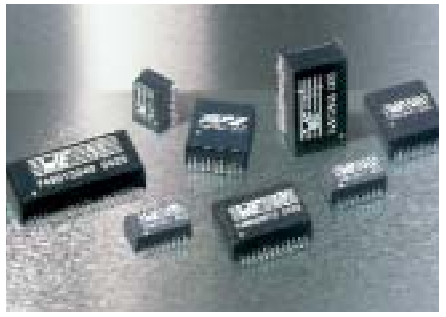
The 6pinWSOF package takes up just half the board area of the earlier SC-95 and SOT-6 packages. The RDS(on) value is down to typically 30 m_, while current and power dissipation ratings are up to 5 A and 1.5 W respectively. An ESD gate-source Zener protection diode provides increased protection against electrical discharge damage.

The new WSOF family comprises 3 N-channel and 4 P-channel devices covering VDS ratings from -12 V to +30 V.

These new devices are added to NEC Electronics' wide range of solutions for power management in portable equipment – from notebook PCs and PDAs to mobile phones.

www.ee.nec.de/mosfet

LAN Transformers for PoE



News from the Würth Elektronik product range: The WE-LAN Ethernet transformers are specially designed for Ethernet applications. Besides transformers for 100 BaseT Ethernet and 1000 BaseT Ethernet, the Würth Elektronik range also includes transformers for Power-over-Ethernet (PoE) applications. The WE-LAN series is compliant with the relevant Ethernet standards IEEE 802.3u, IEEE 802.ab and IEEE 802.3af. Furthermore, the transformers also boast an insulation voltage of 1.5KVAC compliant with IEEE 802.3. The WE-LAN transformers are available for 1,2 and 4 ports.

The LAN transformers may be used with common Ethernet ICs, for example from INTEL, ADM, Globespan and Realtek etc. The application areas for WE-LANs cover servers, network cards, motor controllers, hubs and switches. The operating temperature is in the range 0°C to 70°C. An extended temperature range between -40°C and 85°C, as well as customised solutions are available on request.

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Dual Positive Regulator

Torex Semiconductor, the Japanese manufacturer of power management ICs for battery-powered hand-held equipment, has strengthened its portfolio of regulators with the launch of the XC6406 series of regulators. Fabricated using a CMOS process, the XC6406 series are highly precise, low power consumption, dual positive regulators, offering a combined dual output of up to 600mA. The output voltage is set by laser-trimming at the factory and customers can specify voltages for each output in 100mV increments in the range of 1.8 to 6V.

The XC6406 series is designed to operate in battery-driven or point-of-load circuits such as those found in CD-ROMs, DVDs, PDAs, cameras and video recorders, and can accept an input voltage up to 8V. Power consumption of the IC is typically 20µA (40µA maximum) with a dropout voltage of 150mV at 100mA and 300mV at 200mA. The XC6406 also features an error amplifier, a current limiter and a phase compensation circuit.

Available in the SOP-8 package, the operating temperature range is -40°C to 85°C. A SOP-8FD package is currently under development.

www.torex.co.jp

Fixed Frequency Charge Pump

Optimized for battery-powered portable applications, a fixed frequency, high efficiency charge pump from developer of innovative power management solutions AnalogicTech can be used with ultra-small 1 microfarad capacitors at VIN and VOUT. Conserving valuable board space, the AAT3119 eliminates the need for an inductor, requires only three small external capacitors, and is available in a compact 8-pin SC70JW package.

Representing the company's next generation of regulated voltage doublers, the AAT3119 produces current levels up to 150mA and delivers 300mA of pulsed current. Operating from a 2.7V to 5.5V input range, the device is ideal for RGB and white LED backlighting applications in cellular phones, MP3 players, PDAs, and other hand-held devices.

The AAT3119 delivers a fixed switching frequency that does not change with output current. This is a very important design consideration for noise-sensitive wireless applications like cell phones, where pinpointing a specific switching frequency simplifies the system design.

AnalogicTech's AAT3119 offers significantly higher operating frequencies and lower output ripple than its predecessors. A thermal management system protects the IC during any short-circuit condition at the output pin by sensing die temperature and shutting down the device. Integrated soft-start circuitry prevents excessive in-rush current during startup. A low current shutdown feature reduces quiescent current to less than 1uA.

Rated over the –40oC to 85oC industrial temperature range, samples and production quantities of the AAT3119 are available now.

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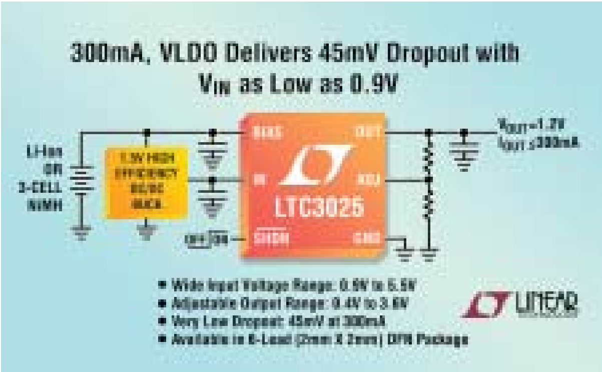
2A Step-Up DC/DC



Linear Technology Corporation announces the LTC3426, a 2 Amp, 6V, 1.2MHz step-up DC/DC converter in a ThinSOT package. Its wide 1.6V to 4.2V input voltage range enables the LTC3426 to operate from dual cell Alkaline/NiMH/NiCd to single cell Li-Ion batteries, delivering outputs up to 5.5V with efficiencies over 90%. Its constant 1.2MHz switching frequency allows designers to keep switching noise out of noise-sensitive circuitry and enables the use of tiny capacitors and inductors. The combination of the LTC3426's high efficiency switch and tiny ThinSOT package provides high current boost capability in a very compact form factor, making it ideal for space-constrained applications.

The LTC3426's 100mOhm switch provides high efficiency at heavy loads. It can generate up to 800mA of output current at 5V from a 3.3V supply. Antiringing circuitry reduces EMI concerns by damping the inductor while in discontinuous mode, and internal soft-start eases inrush current concerns.

The LTC3426ES6 is available from stock in a ThinSOT package.

www.linear.com

Longer Battery Life with Class-D Audio

An amplifier as small as 2 mm x 2 mm is ideal for a variety of portable devices.

DALLAS (January 6, 2005)—Texas Instruments Incorporated (TI) (NYSE: TXN) introduced today a high-performance, filter-free stereo Class-D audio power amplifier that enables designers of cell phones to develop audio-rich products, while maximizing talk time and audio quality. With about two-thirds lower quiescent current and 80 percent lower noise floor than its nearest competitor, the TPA2012D2 packs high efficiency and audio quality in a tiny package, enabling the features and form factors consumers demand. The device is also ideal for personal digital assistants (PDA), notebook computers, portable DVD players and other types of portable audio equipment.

www.ti.com/sc05007

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