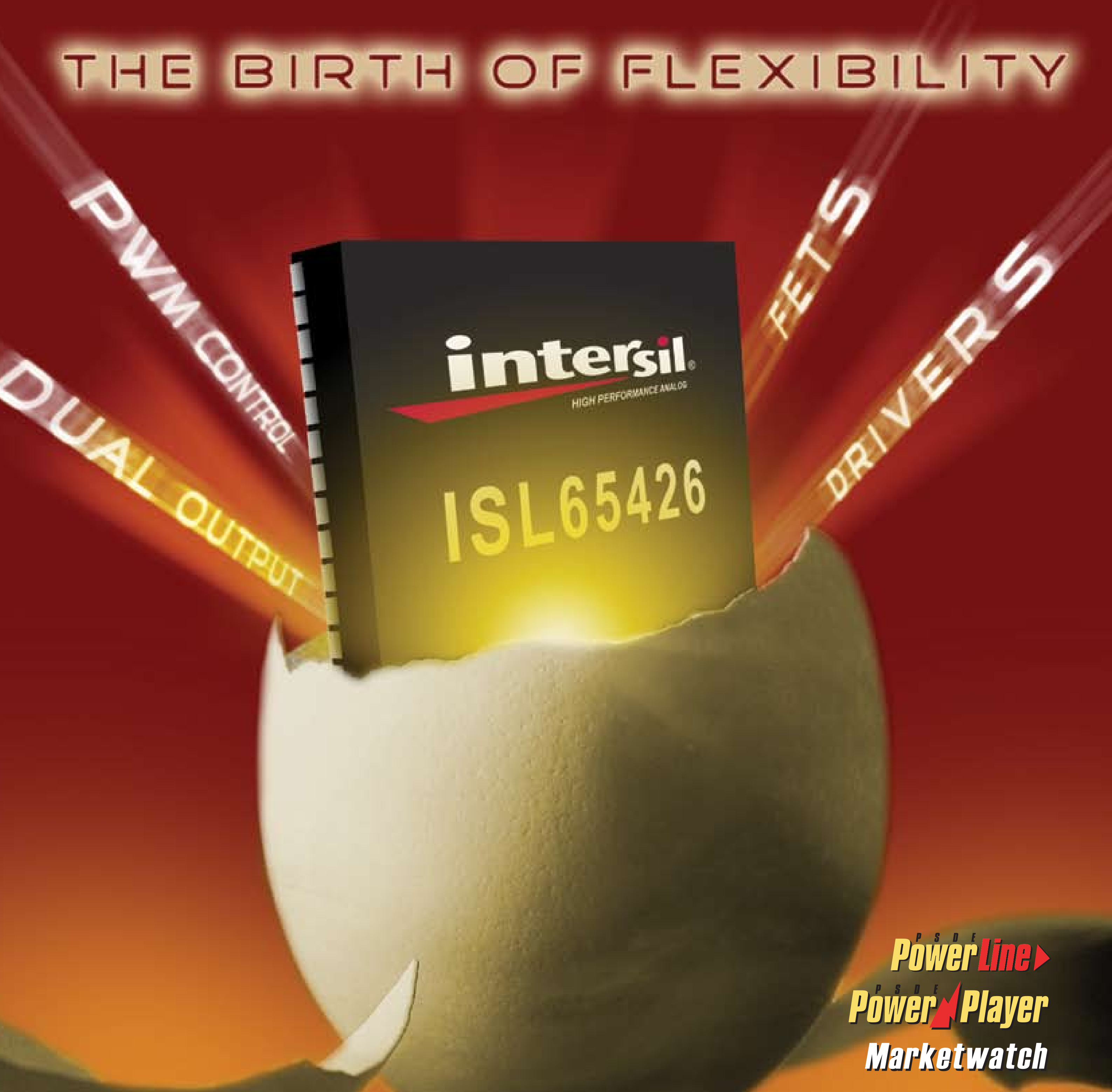
Power Systems Design EUROPE

Power Control Intelligent Motion

July/August 2006



PowerLine
PowerPlayer
Marketwatch

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Power Systems Design EUROPE

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Power Sources Manufacturers Association
The Multinational Power Electronics Association

Powering Progression

Now in the editorial hot seat after years of being on the "other side" of the PR business in the semiconductor Industry, feels kind of strange. After entering engineering more years ago than I care to remember, I quickly got into the communication and reporting of semiconductors working over the past twenty years at Texas Instruments, Hitachi/ Renesas and National Semiconductor. My last role with National took me extensively into the field of power management and is proving to be a good foundation for my new role.

Getting along to see everyone in this vast business will certainly be a challenge but one that I look forward to in order to get a broader take on one of the industry's most fascinating areas, power.

Since joining the PSDE team, I've made a start in traveling around our region to get to see our clients and engineers who have all been extremely positive in voicing their support and giving guidance and feedback on where they would like to see the magazine develop. For me personally, this is the best experience I can get in my goal to deliver the most valuable and relevant content to you.

The enthusiasm demonstrated, both for the industry and the magazine, by the engineers I talked with was a great boost for me. It shows the passion for our industry still lives and flourishes in Europe. I would like to thank this snapshot group for their candid and direct feedback and for their support and endorsement of our continuing efforts at PSDE.

I don't need to stress the importance of power for the future, we all know it and are either working on it or, as in my case, reporting the strides forward companies are making. As I get around more, something I feel is vital to get the direct news, I'll be bringing back reports from the field, from engineers and executives alike.

One thing that struck me upon joining the global PSDE team, was the rich resource we have in our steering committee. You can see the list at the front of the magazine.

These are great people from our industry, many of whom I have worked with before. They have proven track records and will help me to enrich the content and flavour of our publication with their experience and insight. Whilst on the topic, I'd like to extend a warm welcome to two new committee members whom I know will bring value to the team and in turn to you our readers and contributors.

Hans D. Huber, V.P. Industrial, LEM and Kevin Parmenter, Director Field Applications Engineering, Fairchild Semiconductor

I look forward with much enthusiasm to working amongst you all to bring the latest in those progressive steps forward in our vitally important industry. A brief overview on what's upcoming:

We have the 12th International Power Electronics and Motion Control Conference, EPE-PEMC 2006, August 30 - September 1, 2006, scheduled in Portoroz, Slovenia. It brings together participants from existing and future member states of the EU and should provide an inspiring forum for the latest in Power Electronics, Motion Control and related areas. Special attention is to be devoted to sustainable energy systems, clean surface transport, and component technologies and converter topologies.

In this issue we hear from XP Power who discuss the viability and the growing attractiveness of commercial converters in military DC/DC applications and the factors affecting their selection.

From On Semiconductor we have an article to guide the designer in the choice of the right power architecture to choose for today's and tomorrow's designs.

This is just a snapshot of the contributed articles in this issue that I hope you will find useful in your work and info base. I would like to hear feedback so that I can work to maintain the high standards achieved by Bodo Arlt and keep the content relevant and presented in the right format for you.

As the new guy I want our content to be in line with what you need to see. Tell me about your views and, in addition, tell me about your new applications.

Cliff Keys
Editor-in-Chief, PSDE
cliff.keys@powersystemsdesign.com

Samsung and Sony Sign Final Contract on Production Line for World's Most Advanced Generation LCD Panel

Samsung Electronics Co., Ltd. and Sony Corporation have signed the final contract for constructing an 8th generation amorphous TFT-LCD panel manufacturing line at their joint venture, S-LCD Corporation.

The venture plans to establish an 8th generation amorphous TFT-LCD panel production line (glass substrate size: approximately 2,200mm×2,500mm), in addition to the current 7th generation amorphous TFT-LCD panel production line, at S-LCD (Tangjeong, ChungCheongNam-Do, Korea).

The venture plans to invest approximately $1.9 billion with each company providing half.

Actual production is targeted to start in autumn 2007 with a production capacity of 50,000 panels per month.

Together with the current 7th generation line, the start of the world's most advanced (8th generation) line will enable both companies to expand production of large screen LCD panels for 50 inch class LCD TVs, of which demand is expected see a significant increase, as well as to acquire a stable supply to meet demands.

www.sony.net

www.eu.samsungsemi.com

Cree to Acquire INTRINSIC Semiconductor

Cree, Inc., world leader in the development and manufacture of semiconductor materials and electronic devices made from silicon carbide (SiC), today announced it has signed a definitive agreement to acquire privately held INTRINSIC Semiconductor Corporation, a leader in research and development of low defect density SiC substrates. Under the terms of the agreement, Cree will acquire all of the outstanding INTRINSIC capital stock and options based on a valuation of $46 million, with approximately $43.5 million to be paid in cash for the outstanding stock and the remainder to be paid through the assumption of outstanding INTRINSIC stock options. Integration of INTRINSIC's technology into Cree's materials product line should accelerate development of larger-diameter, high-quality SiC wafers, which should enable new high-power semiconductor devices and lower-cost LEDs.

"INTRINSIC has developed the first commercially available, zero micropipe SiC substrates using their ZMP™ technology. We believe the combination of Cree's technology and manufacturing expertise with INTRINSIC's ZMP technology will accelerate the commercialization of low-defect 100mm and 150mm substrates. These substrates should not only support our cost roadmap for LEDs, but more importantly, they should also enable us to more rapidly commercialize higher-power devices for motor-control applications and hybrid vehicles," stated Chuck Swoboda, Cree's chairman and CEO.

"We are extremely pleased to be joining the Cree team," said Dr. Cengiz Balkas, president & CEO of INTRINSIC. "The contribution of INTRINSIC's ZMP process to Cree's existing world-class SiC technology and high-volume manufacturing capability represents a unique opportunity to make a new generation of cost-effective SiC devices available sooner than had previously been envisioned."

The transaction is expected to be completed during July 2006 and should not have a material impact to Cree's fiscal 2007 earnings. Cree expects to incur approximately $325,000 of nonrecurring costs in completing the acquisition.

www.cree.com

Maxwell Technologies' BOOSTCAP® Ultracapacitor Wins Prestigious 'Electron D'or' Award

Maxwell Technologies announces it has won the prestigious 'Electron d'Or' award. Maxwell's MC2600 ultracapacitors were selected as the most innovative product for the previous twelve months in the category of power conversion.

The recipients of the Electron d'Or awards are chosen by a jury of industry experts, in conjunction with the editors of 'Electronique', the leading French electronics monthly magazine. This year is the ninth annual awards, and there are prizes in twelve categories.

The MC2600 is a family of ultracapacitor cells and multicell modules aimed at transportation, automotive, telecoms and industrial applications, offering excellent performance and a lifetime of over 1 million cycles. It is available in two distinct types, the affordable Energy Line, and the high performance Power Line that provides the lowest possible internal resistance. This means an optimal solution can be chosen for virtually any application.

The 2600F cell is engineered for operation at 2.7V rather than the typical 2.5V. The BMOD2600-16 module combines six of the MC2600 cells to provide 16-V operation. The MC2600 achieves a power density of 10.4 kW/kg and an energy density of 5.6 Wh/kg.

BOOSTCAP ultracapacitors deliver up to 10 times the power and longevity of batteries, require no maintenance and operate reliably in extreme temperatures. In transportation applications, they efficiently recapture energy from braking for reuse in hybrid drive trains, reducing fuel consumption and emissions. They also provide compact, lightweight, "life-of-the-vehicle" solutions to stabilize automotive power networks and power new, all-electric subsystems, such as drive-by-wire steering. In mission critical industrial applications, where backup power is critical for continued operation or a soft shutdown in the event of power interruptions, they provide reliable, cost-effective, maintenance-free energy storage. In wind turbine blade pitch and braking systems and other industrial applications, they provide a simple, solid state, highly reliable, solution to buffer short-term mismatches between the power available and the power required.

www.maxwell.com

RUTRONIK appoints key position in European distribution

RUTRONIK Elektronische Bauelemente GmbH is consolidating the management of its international distribution activities into one key pan-European position. Frank Rotthoff, an experienced industry insider has been appointed to the post of Sales Director Europe. He is responsible for the entire distribution region spanning 23 European countries outside Germany and reports directly to Thomas Rudel, Managing Director of Sales and Marketing. The management of the distribution activities within Germany remains unchanged in the hands of Manfred Machner. Rotthoff. In his career to date, Frank Rotthoff has focused on international and worldwide activities, initially in the field of machine, plant and process technology and since 1989 in the semiconductor business.

Rotthoff has many years of international management experience and responsibility in marketing with strong emphasis on distribution with leading manufacturers of semiconductors.

www.rutronic.com

China's Technology Imports Up 60% in First Half 2006?

China has signed 5,461 technology import contracts valued at 13.2 billion U.S. dollars in the first half of 2006, an increase of 62.2 percent on the previous year, according to the Ministry of Commerce.

A report of the ministry published this week said the railway transport industry signed contracts worth 3.93 billion U.S. dollars from January to June, eight times that of the same period of last year.

The electronics and telecommunications industry signed 782 technology import contracts, with the contractual value reaching 2.79 billion U.S dollars, up 150 percent.

The European Union is still the number one technology exporter to China. In the first six months, China signed 5.62 billion U.S. dollars worth of technology import contracts with the EU, a rise of 45.7 percent.

Japan and the United States ranked second and third, with technology contracts signed with China standing at 3.36 billion and 2.08 billion U.S dollars, up 25.4 and 15.7 percent respectively.

www.chinadaily.com.cn

Legislation Passed by US Congress Promotes Purchasing Energy-Efficient Servers

The US House of Representatives passed legislation recently imploring Americans to give high priority to energy as a factor in determining best value and performance for purchases of computer servers.

The bill was sponsored by Rep. Mike Rogers, who has made energy issues a focus of his legislative activities. The new bill directs the Environmental Protection Agency to conduct a three-month study "of the growth trends associated with data centers and the utilization of servers in the federal government and private sector."

Technology companies have been striving to increase energy efficiency in servers for the last few years. These efforts include Sun Microsystems' CoolThreads® microprocessor, which uses less power than the average light bulb and Intel' Woodcrest® and Montecito® processors, which both consume approximately 30W less than their previous models. An association of technology companies (including Advanced Micro Devices, Dell, Hewlett-Packard, IBM, and Sun) has also been formed to promote efficient power production and consumption.

The 2006 Digital Power Forum (DPF 06) will include representatives who will be giving papers and making presentations that directly address the issues and concerns brought into focus by the recent legislation. The DPF 06 will be held in Dallas, Texas, September 18-20.

www.darnell.com/digitalpower/

Texas Instruments Executive Meets with India Government Official to Outline Benefits of Open Standards to Drive Mobile Phone Penetration

TI Reinforces 20-year Commitment to India and announces a new R&D Centre in Chennai.

At a meeting with press today hosted by Thiru Dayanidhi Maran, the Honorable Minister of Communications & IT for India, Texas Instruments Incorporated outlined how continued support of open technology standards will enable India to reach its goal of 500 million mobile phone subscribers by 2010. Gilles Delfassy, TI's senior vice president of its Wireless Terminals Business Unit, also announced that TI is increasing its wireless design presence in India with a new research and development (R&D) centre in Chennai. TI's history in India began with a research and development centre in Bangalore more than 20 years ago and has now expanded with this new centre in Chennai dedicated to a platform of technologies that will span across TI's product portfolio.

"Mobile phone growth in India is nothing short of a phenomenon, and the wireless industry waits for India's next move because of the impact it will have on the future of mobile phones," said Delfassy. "Today, there is a huge opportunity to connect the unconnected as the majority of India's population does not have access to communications services. TI has been committed to India for over 20 years, and I'm pleased to say that we are escalating our existing wireless design presence in recognition of the importance of India to the global wireless market."

www.ti.com

Power Events

- ***EPE-PEMC 2006,*** *Aug 30 - Sep 1, Portoroz, Slovenia, www.ro.feri.uni-mb.si/epe-pemc2006*
- ***H2Expo,*** *October 25-26, Hamburg, www.h2expo.com*
- ***ELECTRONICA 2006,*** *Nov. 14 - 17, Munich, www.electronica.de*
- ***SPS/IPC/DRIVES 2006,*** *Nov. 28 - 30, Nuremberg, www.mesago.de/de/SPS/main.htm*

New Low Power 4.3 Inch LCD in 16:9 Format

Sharp announces its new line-up of small-format widescreen displays with ASV technology for demanding mobile A/V and industrial applications With the new 4.3 inch LCD product line, Sharp is launching three small-format TFT displays, offering real 16:9 widescreen viewing. These displays feature developments such as ASV technology providing excellent clarity from different viewing angles. In addition the contrast ratio of 400:1, 16.7 million colours and 480 x RGB x 272 pixels provide outstanding picture quality. These qualities make the new TFTs ideal for use in mobile high-end multimedia and industrial applications.

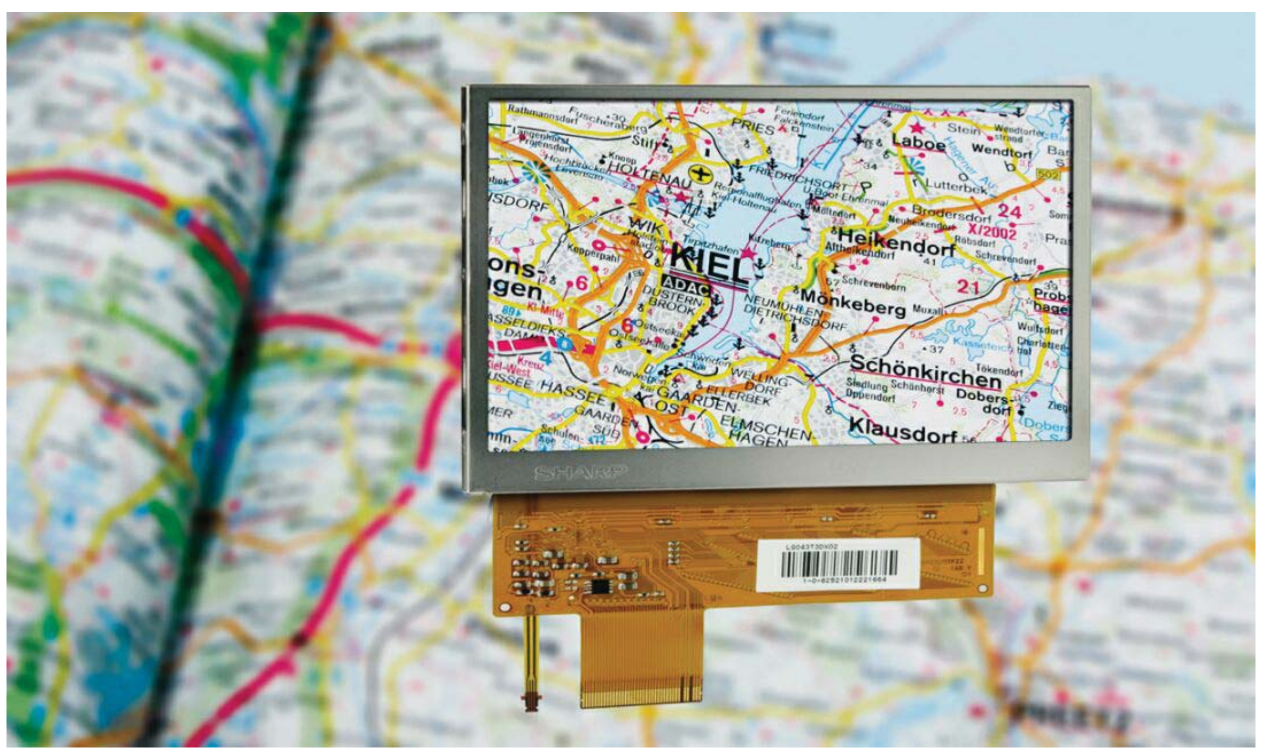
The high performance and low power consumption are an ideal fit for consumer, medical and industrial applications These new displays integrate ASV technology, which extends the viewing angle to 160 degrees. In addition, the panels and the LED background lighting have low thermal power loss-important for mobile applications such as handhelds with audio-visual features such as games consoles, portable media and DVD players. With these multimedia features, these products demand high standards in terms of the display picture quality. Additionally, there is a growing trend towards producing videos and films in 16:9 – another advantage of the widescreen format.

As well consumer applications the modules are also suitable for industry and medicine applications. Here, it is essential to display clearly vital images in full such as oscillator or ECG curves in the widest possible picture format. For excellent clarity and perfect functioning even under difficult operating environments, the LQ043T3DX04 module also offers an extended temperature range from -20 to +60 °C and a luminance of up to 230 cd/m². A further model featuring a touch screen is also planned.

This new device can be controlled by an ARM based processor BlueStreak series, e.g. the ARM9-based 32-bit MCU LH7A404 with 266 MHZ, which is particularly suitable for multimedia applications.

Samples of the LQ043T3DX04 module will be available worldwide from September via Sharp distribution offices and distribution partners. Series production is scheduled to start in Q4 2006. The LQ043T3DX02 is already in mass production.

www.sharpsme.com



POWERpuzzler #12

sponsored by POWER INTEGRATIONS

Laying it All Out

by Peter Vaughan
Manager of Product Applications
Power Integrations

Test your power supply design knowledge as it pertains to printed circuit board layout by trying your hand at answering the three questions below. Check your answers at www.powerint.com/puzzler12 and enter for a chance to win a new Apple iPod nano.

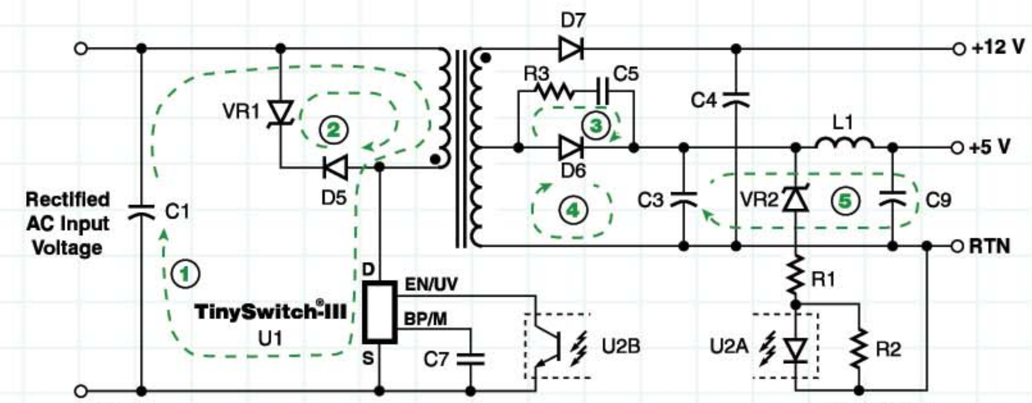


Figure 1.

Question 1: beginner

Match each of the current waveforms shown in Figure 2 to the five current loops shown in Figure 1. The X-axis represents time, where t=0 is the start of a switching cycle (U1 internal MOSFET turns on). The Y-axis represents current, with the peak current values indicated on each waveform.

A. ____ B. ____ C. ____ D. ____ E. ____

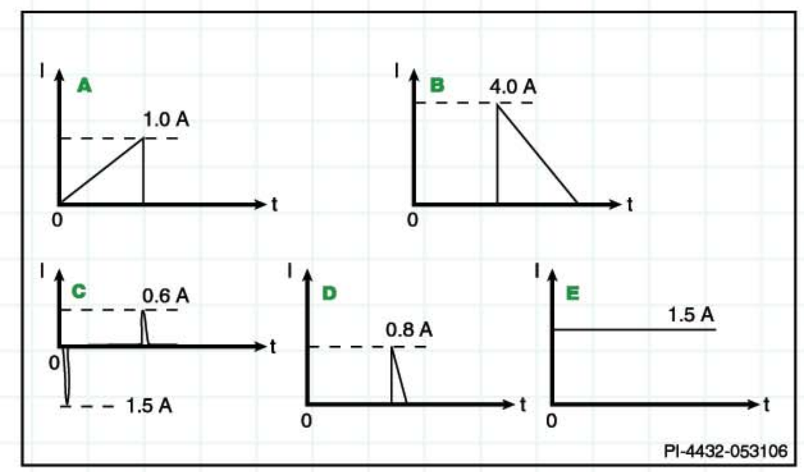


Figure 2.

Question 2 : advanced

Layout is a crucial step in addressing EMI, specifically making sure loop areas are as small as possible. Figure 1 shows five different loops in a typical Flyback power supply. Arrange these loops according to which loop area is most critical to shrink.

1st ____ 2nd ____ 3rd ____ 4th ____ 5th ____

Question 3 : expert

Figure 3 shows a partial layout for the two output power supply shown in Figure 1. Can you spot five areas where the layout could be improved? While you are not permitted to add or subtract components, you may reposition them. Black dashed lines indicate the important primary and secondary side loops.

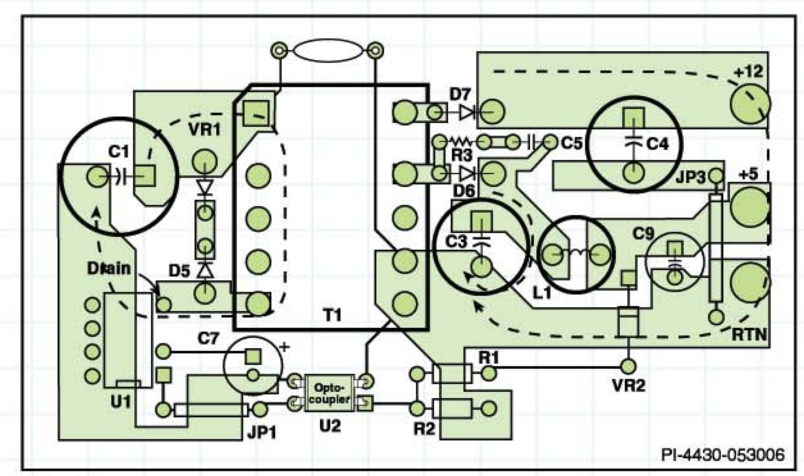


Figure 3.

*The answers to these questions can be found at **www.powerint.com/puzzler12**. Check out how well you did and enter to win an Apple iPod nano!*

Power Player

Power Supply on the Chip, a New Reality

By Paul Greenland, Vice President Marketing, Enpirion

The rationale for putting the power supply in the same package as a system chip is very compelling. The system chip in question could be a microprocessor, an FPGA, DSP, network or applications processor with dedicated power requirements. If the power supply is "in-board" the system chip manufacturer does not carry the burden of power management applications engineering as the power supply is "tuned to its load", and a standard power rail can be applied externally. Another significant advantage is that of electromagnetic compatibility; high-frequency power supplies require careful layout, ensuring that connections carrying pulsating currents are short, direct and that current loops encompass the minimum area. This is far easier inside the package, or on the die. Unfortunately there are practical limitations to putting the power supply in the same monolithic integrated circuit as the system. State-of-the-art system integrated circuits are manufactured in deep submicron CMOS technologies. These technologies can only withstand a low voltage and have limited isolation between adjacent circuits. These two aspects of system chip technology make it difficult to put a switching converter on the same die as the rest of the system. The options left to the system IC manufacturer wishing to embody the power supply are to employ a stacked structure, where the DC-DC converter is mounted on top of the system IC or a side-by-side approach where the DC-DC converter is mounted on the same lead frame as the system IC. The stacked approach has the smallest footprint, at the expense of profile. Many system IC manufacturers have restrictive packaging rules, set up from the stacking of flash memory, which limit the efficacy of stacked power supply implementation.

Once we have decided to place the DC-DC converter inside the system IC package, either in a stacked or side-by-side configuration, power management technology aspects such as: power switch characteristics, IC process, packaging and magnetics should be considered. Miniaturized chip-scale DC-DC converters must switch at high frequency to reduce the size of built-in filter components. The power switch should be "tuned" to its high-frequency application in the same way as the DC-DC converter is tuned to its load. A common figure of merit for matching MOS switches to their high frequency power switching task the product: $r_{DS\,(on)} \cdot (C_{iss} + C_{oss})$, this figure of merit sets the efficiency of switching over a given frequency range. The driver for the power switches must also be matched to its load, to minimize dead time and noise susceptibility. IC process technology should have a high logic density, sufficient to implement sophisticated non-linear and adaptive control without consuming too much die area. Thermally enhanced packaging, which reduces parasitic resistance and inductance, is essential as switching frequency increases. Strict PCB layout guidelines with thermal vias placed under areas of high current density are the norm. Encapsulated magnetic components are particularly tricky to implement. First the magnetic material should be carefully selected to have the appropriate properties at high frequency. Next, the shielding of the magnetic component, in this case an inductor is important to prevent stray magnetic fields and losses from eddy currents induced in adjacent metal (lead frame, PCB tracks, current redistribution layers or integrated circuit metal runs). Furthermore, the process of encapsulation can change the magnetic properties of the inductor, particularly if it has a discrete gap to support direct current, so a low-stress encapsulation method is desirable. A further element in making power supply on a chip a reality is close cooperation with the system IC manufacturer during design so that the tuning of the power supply to its IC load is optimal. This is best achieved with a direct IC designer to IC designer interface, brokered by internal applications and systems engineering. Full system level behavioral simulations are particularly useful in predicting and curing anomalous operation before the IC design phase commences.

In summary, the decision to place the power supply inside the system IC has a number of persuasive advantages. The efficiency of the fully integrated assembly is higher as the power supply is tuned to its load. The ultimate customer finds the assembly easier to use with a standard power supply, bad news for those manufacturers who promulgate the myth that power management is a "black art" which makes expensive applications support a necessity. From the user's perspective, a system implemented with standard power rails has the best cost-performance trade-off as standardized power supplies are readily available and simple to apply, leaving the system designer to concentrate on aspects of the design which bring differentiation and added value to the end-product.

www.enpirion.com

Efficiency and Harmonics Regulations Drive the Efficiency Challenge in Power Supplies

By Chris Ambarian, formally of iSuppli, recently joined Qspeed

Before we can discuss what's driving the efficiency challenge, it probably makes sense to define: What is the efficiency challenge? As I see it, it is the drive to increase power supply efficiency and density even in the face of factors that make it exceedingly difficult to do so.

On one side, we have the US pushing the 80 Plus program (www.80plus.org), that requires computer power supplies to be at least 80% efficient at 20%, 50%, and 100% of rated load, with a true power factor of at least 0.9 to gain program certification. The effort is driven by the US Environmental Protection Agency's EnergyStar® program (www.energystar.gov). Compliance with the program spec represents a significant improvement in power supply performance over typical supplies, which last year had efficiencies in the range of 70-75%. The spec also essentially mandates active PFC (power factor correction) in every unit. Sponsors of 80 plus include several North American utilities companies who are among those who stand to benefit from the reduction in power demand and the increase in power quality.

Now we have the European Union (followed quickly by China) responding to their grid challenges in requiring all loads of greater than 75W (IEC 61000-3-2, which also applies to a wide range of electrical and electronic equipment) to meet stringent harmonic content limits – again, effectively a requirement for active PFC. Meeting these new mandates will not be easy, cost is everything. Anyone who's been in the power supply industry for a while knows it. So there's the challenge: meeting what you must, but at a rock-bottom cost. This balancing act is no accident.

If we had a "90 plus" mandate instead of 80 plus, at this point it would certainly add astronomically to the cost of a supply, and would take us to the absolute limits of current technology. Therefore more reasonable, achievable targets have been set ¨C but even getting to 80% efficiency with 0.9 power factor at various operating points is likely to add something to the cost of a power supply. As energy prices increase and the world becomes more aware of the need for efficiency, the job of merely keeping up with the specs at the traditional "same or lower cost" is a challenge. Add to this the fact that in the last year, component suppliers have been using a favorable pricing environment and rising raw materials costs to justify substantial price increases.

The power supply industry is now pressed in the middle of all these factors yet manufacturers are responding with ever more creative ways to meet the evolving regulatory environment, while being cost-competitive. The opportunity for semiconductor suppliers and power suppliers alike is to help each other to meet the stringent requirements of the market trend toward greater efficiency. But that's of course not as easy as it sounds.

There are already many techniques for increasing the efficiency of the power conversion function available to power supply R&D managers. We may think the question is, "Which one of those techniques provides the ***highest*** efficiency increase for the least amount of money?" But in reality, the question for most R&D managers turns out to be which approach will provide them ***adequate*** efficiency to meet the market requirement, for the lowest amount of money. The challenge for semiconductor and passives suppliers will be in creating devices that will enable power supply manufacturers meet their efficiency and power quality requirements, at the lowest cost.

I have until recently been an industry analyst and it has not been possible to discuss confidential details of how R&D people in the semiconductor and power supply industries are planning to meet these challenges. But as I now transition back into the position of component supplier, these challenges will be at the forefront of my thoughts. I'm confident that we'll be talking again soon about the types of components that will provide the best solutions.

www.isuppli.com
www.qspeed.com

Configurable 6A Dual Synchronous Buck Regulator with Integrated MOSFETs

Flexible and Compact DC-DC Converter Design

Power supply design for an FPGA or CPLD in an embedded system is a complex task. Choosing the appropriate control IC and power MOSFETs, correct inductance and capacitance values, loop compensation and choices for power dissipation, load regulation, efficiency and size can be time consuming. Also, late changes may require the power supply to be reconfigured to new specifications.

By Zaid Salman, Technical Marketing Manager, and Sarika Arora, Product Marketing Manager, Intersil Corporation

Electronic systems that require a large amount of digital processing are frequently implemented with field-programmable devices such as field-programmable gate arrays (FPGAs) or complex programmable logic devices (CPLDs) instead of a custom application-specific integrated circuit (ASIC). Although a custom ASIC might offer a cost advantage over a field-programmable device, the field programmable devices offer the advantages of instant manufacturing turn-around, low startup costs, and speed and ease of design changes. These advantages have propelled FPGAs and CPLDs into the devices of choice to implement complex digital systems such as ethernet switches and routers, storage area networking devices, and multimedia content delivery systems.

Employing FPGAs and CPLDs

The procedure for implementing a circuit design using an FPGA or CPLD comprises the following general steps: design entry, design validation, design compilation, and device programming.

The design entry phase consists of capturing the design, either through the creation of a graphical schematic diagram using a computer-aided design tool, or by description of the circuit using a hardware description language such as Verilog or VHDL. After the design is captured, it is validated through the use of circuit simulation to verify correct functionality and performance. If the circuit does not perform as desired, the engineer returns to the design entry phase to make any required changes to the design and then repeats the design validation phase. The design entry and design validation steps may be repeated multiple times before a design is reached that meets all the functional and performance requirements.

After a satisfactory design is obtained, the engineer uses software provided by the FPGA or CPLD device vendor to "compile" the design into a form that is used to configure the device that will implement the design. The file that results from the compilation process is downloaded to the FPGA or CPLD and programs the internal logic with the correct functionality.

Powering Field-Programmable Devices

FPGAs are powered by three basic supply rails: the core supply rail, the I/O supply rail, and the auxiliary supply rail. Each of these rails has different load current requirements. The core supply rail, VCCINT, provides power to the internal logic of the device, which generally has the most demanding current requirements. The voltage on VCCINT can be as high as 3.3V for older generations of FPGAs, to as low as 1.2V for current devices.

The I/O supply rail, VCCIO, provides power for the input/output blocks of the FPGA. The voltage on this rail could be 1.5V, 1.8V, 2.5V, or 3.3V depending on the I/O standard being utilized. The particular choice of I/O standard is driven by the devices to which the FPGA will communicate.

The auxiliary supply rail, VCCAUX, is used to power the digital clock managers and JTAG I/O circuits on the FPGA. This voltage is usually 2.5V or 3.3V.

Variable Power Requirements

The programming and configuration of an FPGA or CPLD can be changed at any time by the engineer simply by repeating the design compilation and downloading steps described above. There is no limit to the number of times that the FPGA can be reconfigured to a new design. There are no circuit board traces to change, no components to swap and nothing to resolder, thereby allowing design troubleshooting and tweaking to be achieved very quickly and easily. Also, functions and features can be added to a given design with little to no impact on the physical layout. This is what gives field-programmable devices their tremendous advantage as an implementation medium for complex digital systems.

However, such flexibility does not come without a price. The power requirements for an FPGA, specifically the supply current that it will draw, are proportional to the complexity of the design. Reconfiguring an FPGA to new functionality will change the demands on the power supply system that provides power for it. The more of the FPGA that is utilized, the more supply current it will require. Supply current requirements will also increase with clock frequency, so the faster the FPGA is run, the more power it will draw. As a result, functional changes to the FPGA will dictate changes to the power supply design.

Monolithic Dual-Channel Buck Regulator

To address the need for compact and flexible power systems, and to provide digital designers with a solution that enables quick design and reconfiguring of FPGA power supplies, Intersil has introduced the ISL65426. The ISL65426 is a dual-channel synchronous buck regulator that is capable of providing up to 6A of total load current with efficiency up to 95%. The two output voltages are logic-programmable or resistor adjustable, with the load current for each output channel being user-configurable. So if the FPGA/CPLD power needs change during the course of the design, the new requirements can be met by simply reallocating the load current for each channel.

This fully integrated synchronous buck DC/DC regulator eliminates the engineering effort required to select power MOSFETs, determine loop compensation parameters and simplifies the selection of inductors and capacitors. Overall component count is reduced because the internal high-side MOSFETs are implemented with PMOS devices instead of typical NMOS devices, thereby eliminating the need for bootstrap capacitors. Internal digital soft start capability and internal loop compensation eliminate the external soft start capacitor and the external RC compensation network.

A thermally enhanced QFN package, the high 1.1MHz operating frequency and reduced BOM component count results in a compact power supply solution for the VCCINT and VCCIO supply rails of an FPGA.

A block diagram of the ISL65426 is shown in the following figure:

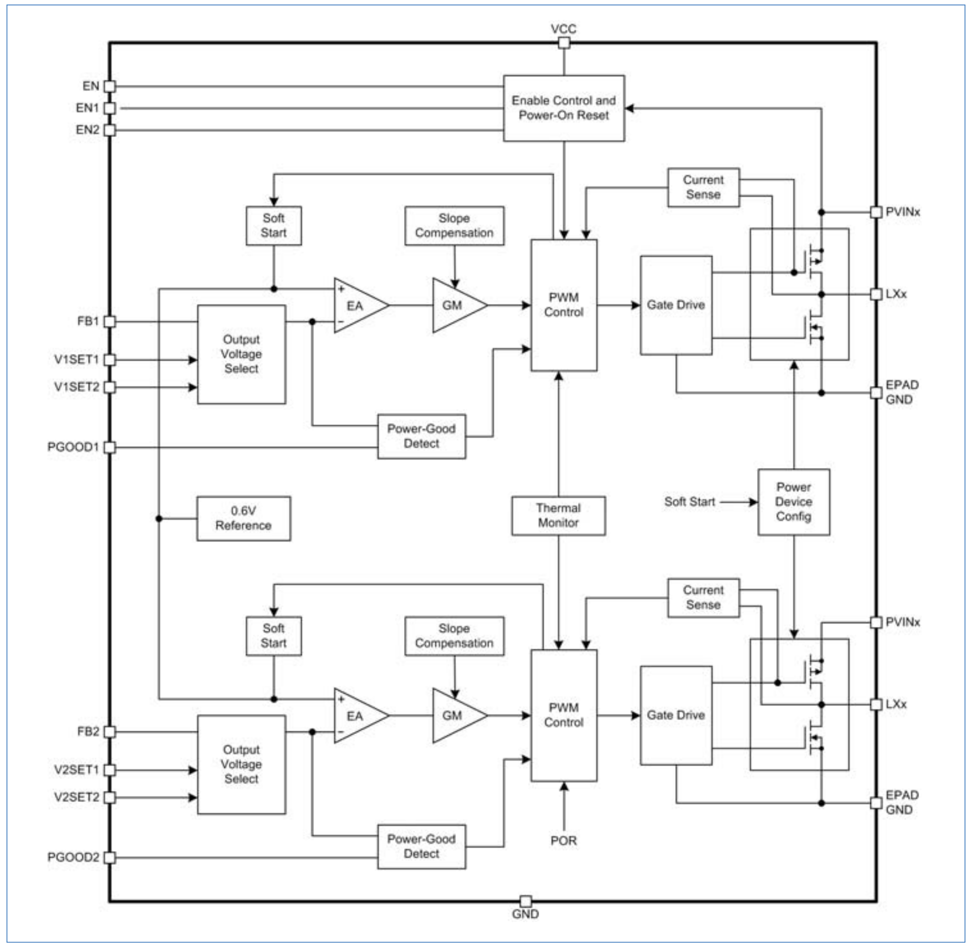


Figure 1. ISL65426 Functional Block Diagram.

Configurable Load Current Capability

The ISL65426 facilitates quick design of the power supply system through its use of a unique architecture that consists of user-configurable power blocks. This power block architecture allows partitioning of six 1A-capable modules into one of four power configuration options. There is one master power block associated with each synchronous converter channel. The four remaining power blocks are slaves that can be user-assigned to either of the master converter channels, as shown in the following figure.

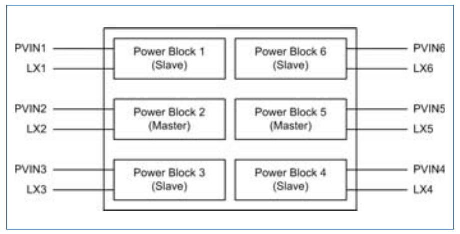


Figure 2. ISL65426 Power Block Architecture.

Utilizing the power blocks, the load current capability of each channel of the ISL65426 can be assigned. The chip contains two logic pins, ISET1 and ISET2, that program the allocation of load current for each channel according to the following table:

ISET1	ISET2	Channel 1 IOUT	Channel 2 IOUT
low	low	2A	4A
low	high	5A	1A
high	low	4A	2A
high	high	3A	3A

Table 1. Output Current Configurations.

Each power block has its own power supply connection, PVIN, and inductor connection, LX. The ISL65426 can be used to regulate two output voltages from one or two input supplies. As the load current requirements of a given power supply design change, the design can be retargeted with minimal effort. Because the ISL65426 contains internal power switches and is internally compensated, a change in load current allocation between the channels can be made simply by changing the ISET1 and ISET2 logic levels and the PVIN and LX connections to the chip.

The following figures illustrate some typical configurations:

Flexible Output Voltage Selection

The ISL65426 features the ability to program the output voltage for each channel without the use of external feedback resistors. Four logic pins,

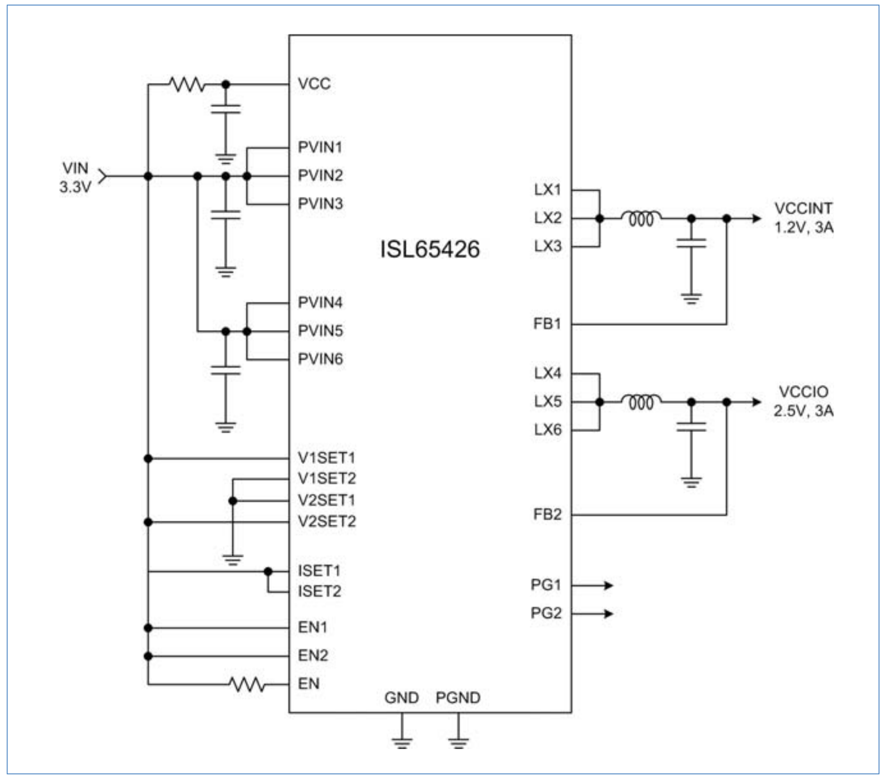


Figure 3. ISL65426 in Single-Supply, 3A/3A Output Current Configuration.

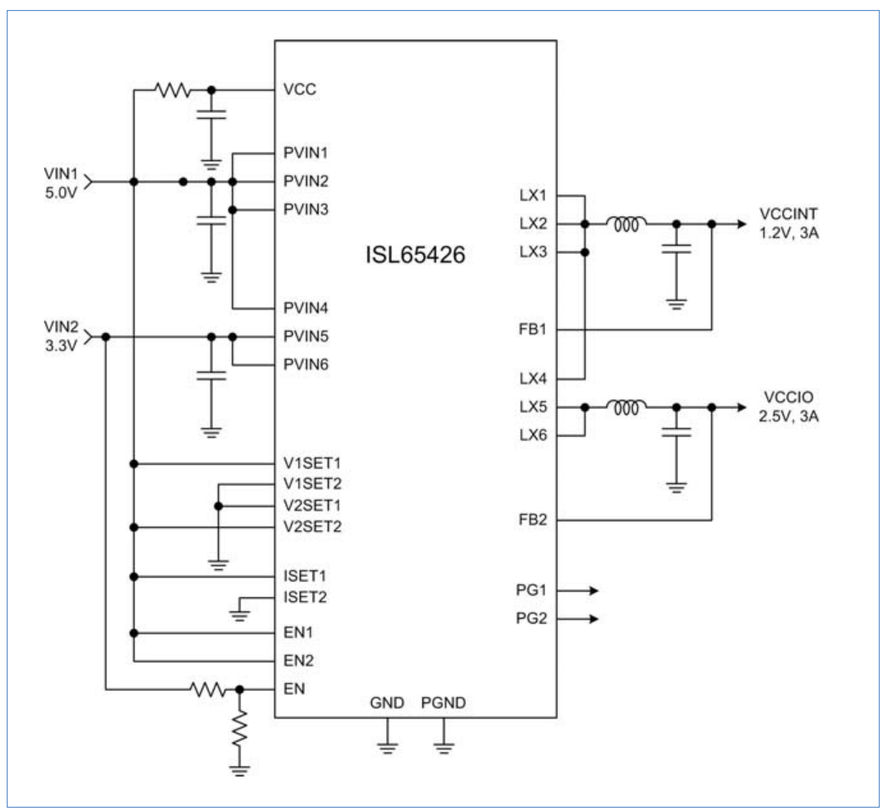


Figure 4. ISL65426 in Dual-Supply, 4A/2A Output Current Configuration.

V1SET1, V1SET2, V2SET1, and V2SET2, select the output voltage for each channel from a list of common values. Essentially a 2-bit VID input, this provides further ease of redesign and retargeting as it enables modification of the output voltages through logic rather than with a physical change to the power supply board and its components, allowing changes to be made quickly and reliably. Additionally, the 2-bit VID input enables digital control of the output voltages of the ISL65426 regulator channels in those systems where such control is needed. Table 2 lists the output voltage selections:

V1SET2	V1SET1	Channel 1 VOUT	V2SET2	V2SET1	Channel 2 VOUT
low	low	0.6V	low	low	0.6V
low	high	1.2V	low	high	1.8V
high	low	1.5V	high	low	2.5V
high	high	1.8V	high	high	3.3V

Table 2. Output Voltage Configurations.

Eliminating the need for feedback resistors simplifies the design, reduces component count, and increases the overall accuracy of the system. Yet this ease of output voltage selection does not come at the expense of design flexibility since the ISL65426 retains the traditional resistor divider method of setting the output voltage. The internal reference voltage of the chip is 0.6V, and through the use of resistor feedback, the output voltage for each channel can be set to any value between 0.6V and 4V when using a 5V input supply.

Integrated Fault Protection

The ISL65426 is equipped with overvoltage, undervoltage, overcurrent and overtemperature protection mechanisms so that all fault monitoring and protection is fully integrated into the chip and requires no external components.

In an overvoltage situation (when the output voltage exceeds the overvoltage level defined as 115% of the reference voltage), the ISL65426 will actively try to regulate the output voltage down to the output setpoint.

For undervoltage protection, the feedback voltage is monitored and compared to the undervoltage threshold (defined as 85% of the reference voltage). Upon detection of an undervoltage condition on either of the converter channels, a 4-bit counter is incremented. If an undervoltage condition is detected on both converter channels in the same switching cycle, the 4-bit counter is incremented twice. The counter will continue to increment as undervoltage conditions are detected in each converter channel. Once the counter overflows, the undervoltage protection logic shuts down both regulators.

The overcurrent protection circuitry also utilizes of a 4-bit counter to keep track of overcurrent events. The current in each power block is measured and compared to the overcurrent limit that is appropriate for the particular power block configuration in use. If the measured current exceeds the overcurrent threshold, a 4-bit up/down counter is incremented by one. If the measured current falls below the overcurrent threshold before the counter overflows, then the counter is reset. If both converter channels experience an overcurrent event during the same switching cycle, then the counter is incremented by two. Once the counter overflows, both converter channels are shut down. If the measured current in both converter channels falls below the overcurrent limit in the same cycle, the counter is reset.

Finally, for overtemperature protection, an internal temperature sensor continually monitors the junction temperature of the ISL65426 and if it exceeds 150°C, the sensor commands the ISL65426 to shut down both regulator channels and latch off.

Voltage Monitoring and Supply Sequencing

Each converter channel of the ISL65426 features its own enable signal and power-good signal. This allows individual control and monitoring of each output voltage, making voltage tracking and supply sequencing possible. There are two enable signals, EN1 and EN2, that enable or disable each channel, as well as a system enable, EN, that can be used to turn on or shut down both channels at once. When the enable signal is received and the channel is enabled, a digital soft-start function ramps the output voltage by stepping the reference voltage up gradually over a fixed interval of 20ms. For voltage monitoring, each converter channel features its own power-good signal that is asserted when the output voltage for that channel is outside the regulation limits.

Sequencing of the two output voltages of the ISL65426 is achieved by connecting the power-good signal from one channel to the enable input of the other. In this configuration, the second output will not begin its soft start cycle until the first output is in regulation. Figure 5 illustrates this:

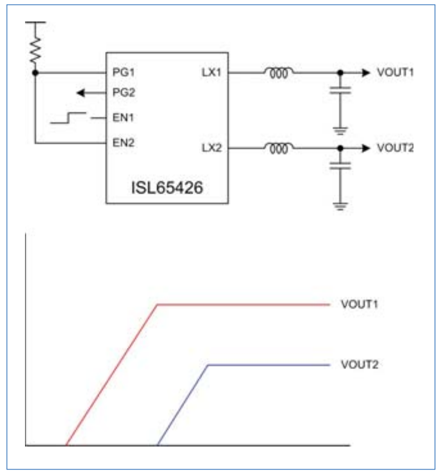


Figure 5. Supply Sequencing with the ISL65426.

Complete FPGA Power Solution

With its ease of configurability, integrated power devices, high efficiency, integrated fault monitoring and protection, support for the use of ceramic capacitors and RoHS compliancy, the ISL65426 represents a complete and environmentally friendly power solution. Design changes can be implemented quickly, easily and reliably, resulting in shorter design cycles and fewer design iterations for the overall FPGA or CPLD system implementation.

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The Vital Importance in Choosing the Right Power Architecture

Considering Costs and Future needs with new Topologies

The importance of Power Supply Design has never been Greater. The options open to the Designer can be bewildering, but help is at hand

By Dhaval Dalal, Systems Engineering Director, ON Semiconductor, India.

Traditional methods of power conversion are getting increased scrutiny as energy regulations become more stringent. It has been shown that energy savings of 15-20% can be obtained if higher power efficiency architectures are employed in power supplies used in common consumer and computing equipment. While everyone talks about higher power efficiency, nobody wants to pay for it. Hence, it is imperative to clearly identify the right power architecture for the given requirements.

The power conversion industry is in the midst of a dramatic shift driven by many important factors. Energy regulation practices are becoming more widespread. These practices demand higher efficiency from power converters in all operating modes. Some examples include standby requirements of <0.5W and efficiency requirements of >80% for many external power supplies required by the California Energy Commission and are also used by Energy Star in the US. Harmonic reduction requirements are increasing the use of power factor correction (PFC) front-ends. The IEC 1000-3-2 is imposed by the EU and Japan and voluntarily implemented in many other countries.

Power density requirements are becoming more and more demanding because end consumers want more functionality in smaller packages. Shorter time to market pressures on manufacturers requires a more modular approach to the power system design.

As each of these first three forces becomes stronger, the viability of traditional topologies to meet system requirements diminishes. However, design engineers are unable to take full advantage of emerging approaches because of the dominance and subsequent pressure of the shorter time to market requirement.

The situation is graphically illustrated in figure 1. Design engineers are busy making incremental improvements with the familiar architecture, while the improved performance requirements are causing additional cost. If they invest in alternative architecture, they can reap the benefits of improved performance at parity cost today while creating a potential for much better performance and/or much lower cost in the future. It is the role of management to identify the right architectures to invest in and allow designers the time to optimize those in order to improve long term metrics. Also, it is the role of component suppliers such as ON Semiconductor to minimize the resources required for such transition by supplying the right components and design tools to these designers.

Distributed vs. Centralized power architecture

Choosing the right power architecture involves breaking down the application requirement into different power processing blocks and choosing the right power processing topology for each block. In simpler systems, the whole system may consist of only one block and the power conversion occurs in just one step. As system requirements get complex, the option is to go to multi-stage power conversion and often to place the blocks in different physical locations (known as distributed architecture). Theoretically, by distributing the power processing, one can optimize the system better to serve distinct load requirements. However,

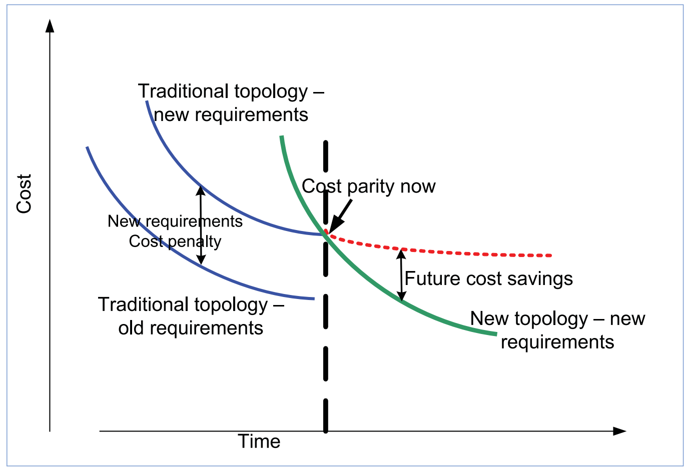

Figure 1. Impact of architecture/topology choice on system cost over time.

such an arrangement often adds cost. Also, in many systems, the distributed architecture concept is carried to the extreme by adding multiple processing stages. While each stage can be optimized, the overall system efficiency from the line to the load suffers considerably.

Application topology grid for off-line applications

When one talks about identifying the right topology, there is naturally no single answer for all applications. In terms of simplicity and widespread use, flyback topology comes closest to being the universal topology. The actual choice is primarily dictated by input voltage and output power and voltage. Factors such as efficiency, size, multiple outputs, and output regulation requirements are secondary determinants.

Figure 2 illustrates a generalized approach of identifying appropriate topologies for a given power level for off-line applications. On the horizontal axis, the power level ranges from few watts to over 1 kW. The bottom band is where the right application can be inserted for ease of association. The traditional topology band shows that the flyback is the choice for low power (up to ~150 W). After that, forward converter becomes more viable, followed by half-bridge or 2-switch forward at higher power and finally a full-bridge topology at the highest power levels. This is conventional wisdom developed over decades of power industry evolution.

However, also shown in figure 2, the emerging topology band provides alternatives at each power level to the conventional approach which are more befitting choices to meet the emerging demands of higher efficiency and better power density. The reason these topologies are more appropriate lies in how they optimize the use of various power components such as FET switches, transformers, inductors, diodes, EMI filters and snubbers. Figure 2 lists the major power components required for each topology, but the component stresses and second order effects require closer attention.

Let us look at the difference between traditional and valley switching flyback converters as an example. Both topologies are similar in terms of

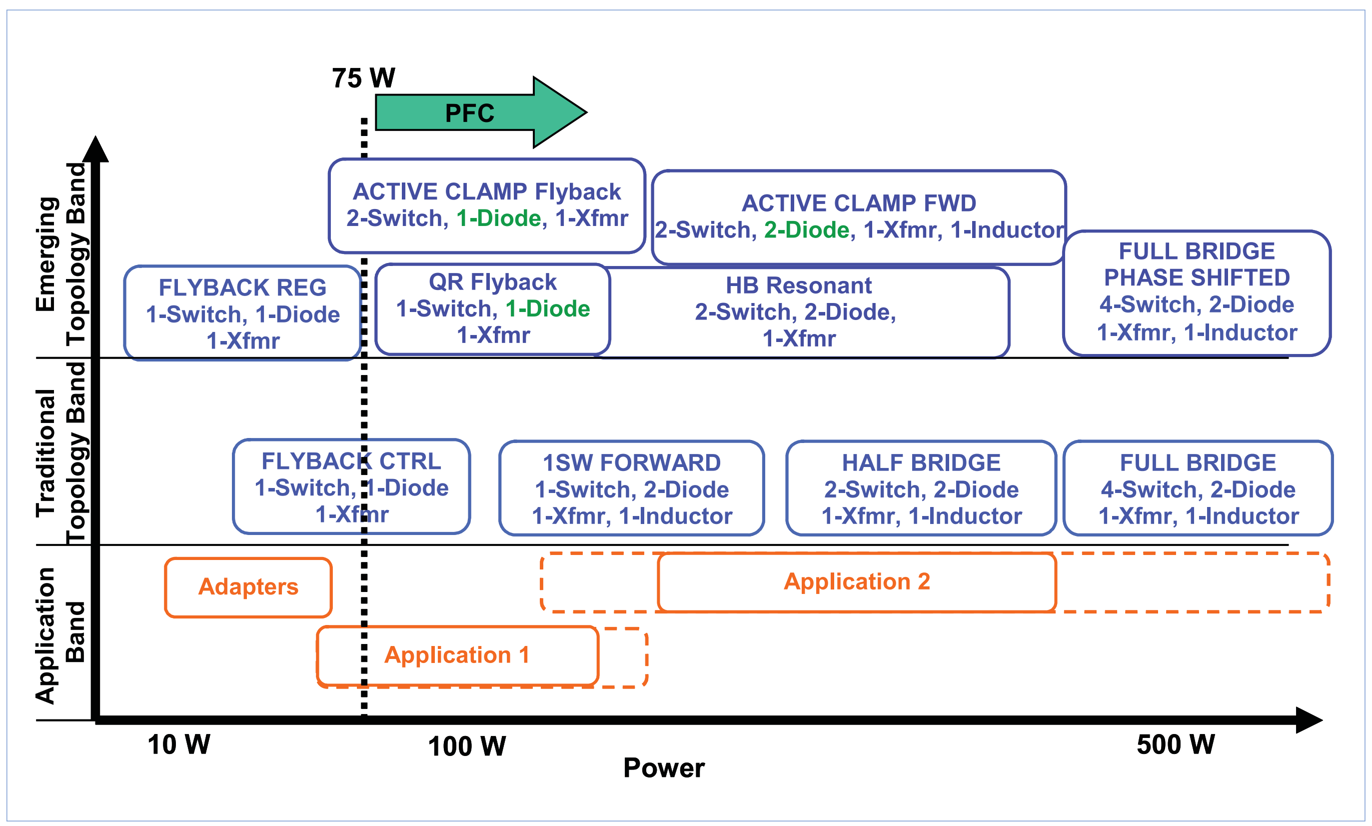

Figure 2. Major Power Components Required for Each Topology.

Attribute	2SW Forward	Active Clamp	Active Clamp Comments
Dmax	0.5 (0.46)	0.65 (0.6)	Higher D leads to several advantages
Vds/rating	425/500 V	714/800 V	two 500 V vs. one 800 V
Np	115	150	More turns
Iprim (rms/pk)	1.78/2.81 A	1.56/2.15 A	Lower currents
Additional needs	2 reset diodes Drive ckt Snubbers	Clamp switch Drive ckt Clamp cap	⇒Low current ⇒Floating drive req'd ⇒Low value (nF), HV
Inductor	X uH	0.77*X uH	23% reduction in Inductor for same freq.
Sec. peak V	18.5 V	14.2 V	More margin for 30 V
Transformer	1-Q operation	2-Q operation	Better core utilization

Table 1. Comparison between active clamp converter and 2-switch forward converter.

power component arrangement, so one switch, one magnetic and one diode are typically used. However, the valley switching flyback reduces switching losses, thereby improving efficiency for similar components or reducing component cost for similar efficiency. In addition, the valley-switching converter offers an easy way to do synchronous rectification in the output if even higher efficiency is required. With traditional flyback, synchronous rectification involves more complexity and cost. The valley switching topology does require a more complex (and novel) control scheme and also has some other characteristics such as variable frequency that the designer has to deal with. However, these are quite easily addressed by smarter controllers that incorporate all the control and protection features and also provide complete design tools for easing the task of the designers.

Another example to evaluate is the comparison between a 2-switch forward converter and an active clamp forward converter that is shown as an emerging alternative for mid-power applications. Again, in terms of component usage, both approaches use the same number of power components. However, a means of comparing different topologies called component stress factor (CSF) analysis was recently introduced. Using such approach, as shown in Table 1, it is clear that the active clamp approach has lower CSF compared to the 2-switch forward for both primary and secondary components. In addition, the ease of synchronous rectification is another key factor separating the two approaches for high efficiency application requirements.

Other considerations

While component stress factor is one of the ways of evaluating topologies, there are other considerations. One of them is whether the system is using the PFC front-end or not and whether any hold-up time is required. If PFC is used and the hold-up time is not required, the input voltage remains relatively constant and the half-bridge resonant converter becomes a better candidate for mid-power applications. This topology eliminates the output inductor and hence provides lower cost alternative. However, it is a variable frequency approach and does not handle line and load variations very well.

Similarly, if there are multiple outputs in the converter, the choice of topology becomes trickier. Any forward derived converter would require coupled choke approach to achieve good cross regulation. Even though flyback converter allows better cross regulation naturally, some outputs may require post regulation. In such cases, the architecture choices need to be reevaluated in view of newly emerging post regulation techniques.

For the PFC front-end, boost topology may be the natural solution, but there are more options in terms of method of control today and need careful consideration. Specifically, by matching the right PFC topology to the right SMPS stage, significant cost savings in the bulk capacitor can be attained.

Summary

In summary, the emerging end customer and regulatory requirements are clearly the driving forces behind a number of innovative and exciting architecture and topology choices for the power supply designer. While it is not natural and easy for the designer to evaluate such varied choices, decision tools and guidelines are becoming available from various sources to make this task easier. Combined with optimized semiconductor solutions, these tools will eventually drive to improved cost/performance metric in many mass market power supply designs.

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Integrated RF Power Amplifier/Filter Front-ends Accelerate Wireless Handset Performance

RF designers break through the integration barrier

Mobile handset design has involved massive levels of integration over the past 15 years, and is set to continue. Here, we see the massive power and space savings achieved today.

By Joe Madden, Mobile/Wireless Market Analyst, Avago Technologies

CMOS designers have been integrating a wide variety of functionality into large ICs for many years. Everyone has seen the incredible impact of Moore's law on performance and cost in everyday life. Within a mobile communications terminal, many components have been either integrated into RFICs or eliminated as direct digital up/down converters have become available.

In communications terminals, two RF components have resisted the pull of integration so far. Filters and RF power amplifiers are constructed with techniques that are incompatible with on-chip CMOS integration. Filters have traditionally been constructed using ceramic or surface-acoustic-wave (SAW) techniques, while RF power amplifiers have been constructed with GaAs heterojunction bipolar transistors (HBTs) or FET devices. Because these technologies are quite different to the silicon or SiGe processes used for RFICs, both power amplifiers and filters have remained as discrete components, separate from the massively integrated chipsets that now perform most of the RF functions in a handset. Acoustic resonator technologies and advanced low-noise, high-linearity transistor techniques have already enabled a significant level of miniaturization for each of these discrete functions. Figure 1 shows the separate film bulk acoustic resonator (FBAR) filter and enhancement-mode pseudomorphic high electron mobility transistor (E-pHEMT) power amplifier used in many of today's CDMA PCS handset designs.

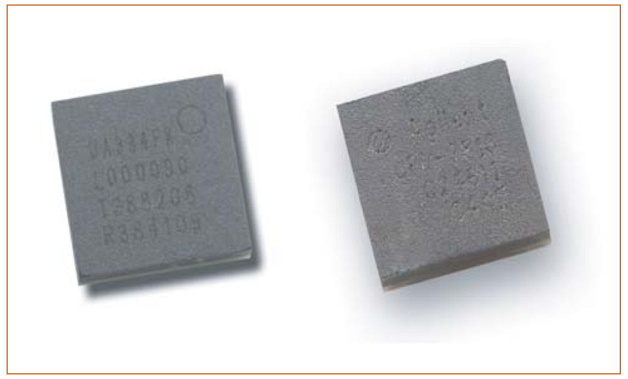

Figure 1. Typical discrete components. A typical FBAR filter (left) and an amplifier using an E-pHEMT active die (right).

However, today's monolithic filter and amplifier techniques allow designers to break through the RF integration barrier. Important advancements include:

- Surface acoustic wave (SAW) filters
- FBAR filters
- Heterojunction bipolar transistors (HBTs)
- E-pHEMT

Because each of these techniques reduces a particular RF function to a monolithic device, the valuable next step of higher integration can take place. Previous technologies such as ceramic filters involved non-monolithic structures, which are very inconvenient for integration with monolithic amplifiers.

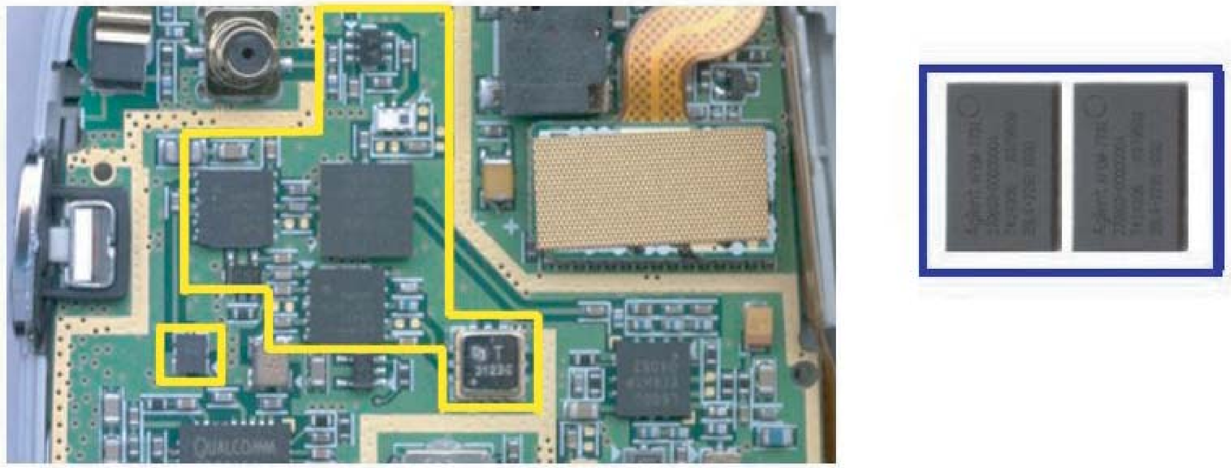

Figure 2. A typical dual-band CDMA handset and an illustration of size savings possible with RF integration.

Recently, several companies have begun development of RF modules using multiple chip technologies and multi-chip on board (MCOB) packaging. This compromise allows for the best possible filter and power amplifier performance through the use of optimized semiconductor processes. A GaAs HBT or E-pHEMT amplifier can be integrated with a silicon-based FBAR filter in an inexpensive package. At the same time, an MCOB module can greatly reduce size and improve performance of an RF front-end.

The first, and most obvious, advantage of an integrated RF front-end module (FEM) is the dramatic size reduction that can be achieved. Figure 2 shows the typical layout for a dual-band CDMA handset. The yellow outline denotes the space required to accommodate the duplexers, filters, and amplifiers for both 800 MHz and 1900 MHz frequency bands. The blue outline shows, to the same scale, the board space required to implement two duplexer/amplifier integrated FEMs. The tremendous size reduction can be attributed primarily to the elimination of multiple input/output interfaces for several components A second advantage of using an RF FEM lies in the efficiency improvement that can be realized. By optimizing the interface between a power amplifier and the filter/duplexer at the output, a designer can extend the talk time of a typical handset by half an hour or more.

The freedom to match power amplifiers and filters to impedances that are optimal for efficiency or linearity performance can yield significant benefits. In Figure 3, a comparison of amplifier and duplexer combinations is shown in which the same amplifier is used with different levels of integration. In all three tests, the output power from the duplexer was set to +24.5 dBm. The improved matching and subsequent reduced insertion losses of the transmit chain in the integrated front-end module result in huge efficiency gains. In a CDMA handset, this efficiency improvement can translate into 35 to 45 minutes of additional talk time.

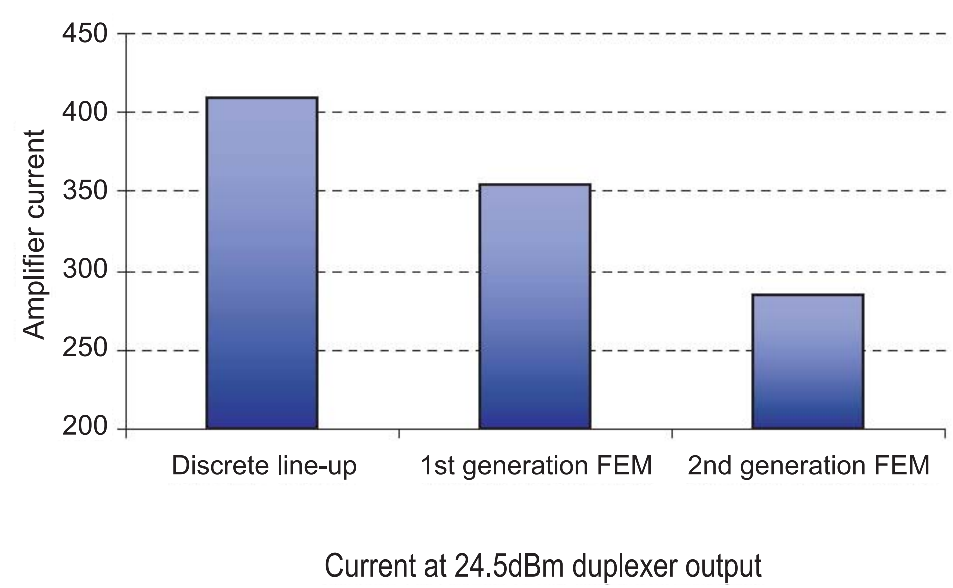

Figure 3. An efficiency comparison for PCS CDMA handset designs.

A third benefit: An integrated FEM is less susceptible to RF interference due to the very short line lengths possible between RF components. The total electrical length between the transmitter output of the RFIC and the antenna can become very short with the integration of multiple functions into a miniature MCOB component. Therefore the RF section of the PCB will both receive less interference and emit less interference which could potentially affect other components.

Where will this performance improvement take us? With the adoption of zero-IF architectures and other advancements in the application of digital techniques, it seems clear that further integration is inevitable for RF components. The question remains: Will future integration of RF amplifiers and filters take place in the RFIC and/or baseband chipsets, or will there be a separate RF integration path?

Several market dynamics point to the likelihood of a partition, which leaves the RF integration in a separate component. For example, in the GSM and W-CDMA markets, the RFIC is often supplied by a different vendor than that of the baseband chip. Because CMOS technology is improving in speed and performance continuously, most experts agree that integrated baseband/RFIC chipsets will become practical in the next few years. The low cost of CMOS technology makes the economic driver fairly compelling: once CMOS can support the functionality of the RFIC, we can expect the market to demand the lower cost point that then becomes possible.

On the other hand, RF components such as power amplifiers and specialized filters require very different kinds of performance from the semiconductor process. Power amplifiers require high linearity and low noise contribution from the transistor, while boosting signal levels to nearly 1 watt. CMOS-based amplifiers have made some progress in recent years, but are not expected to be competitive with high-mobility materials for high power applications, due to the optimization of the CMOS process for low current/low capacitance transistor applications. Therefore, in mobile wireless applications where significant power is required, CMOS amplifiers have significant disadvantages in linearity and efficiency.

Filters and duplexers pose an even more significant challenge for CMOS technology. Most mobile handsets use ceramic, SAW, or FBAR resonators today, taking advantage of the high Q available from the ceramic or acoustic

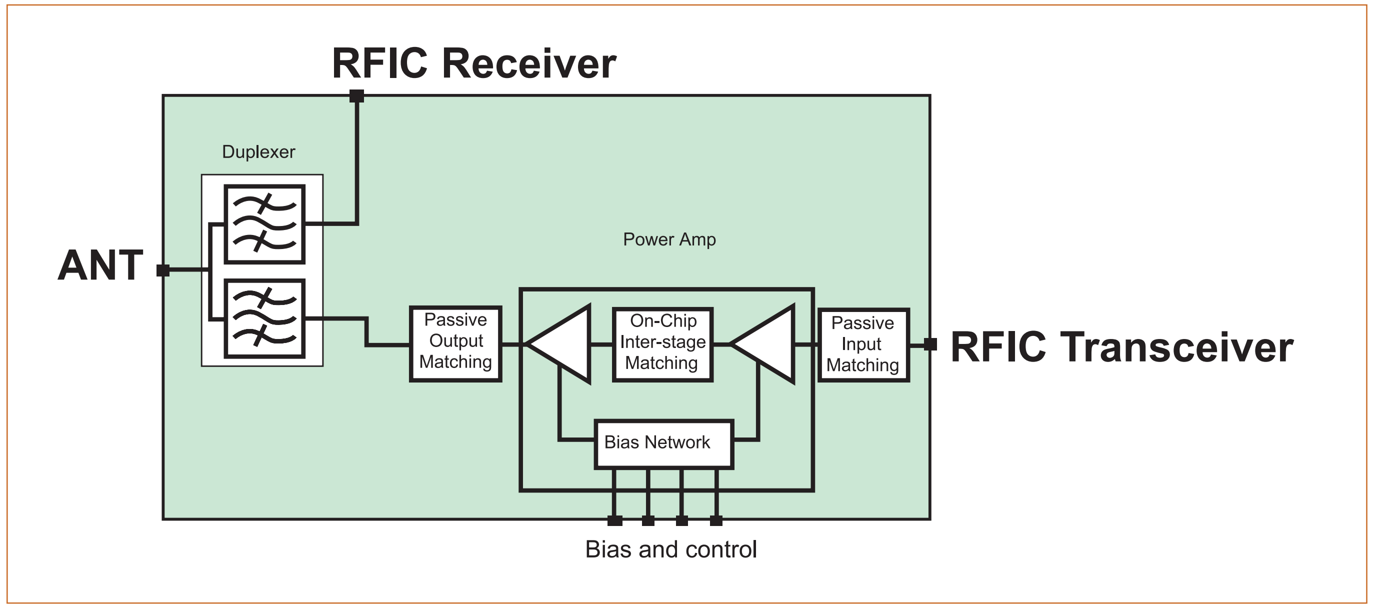

Figure 4. A block diagram for a simple front-end module.

technologies. While inductor Q in a CMOS device typically measures roughly 100, unloaded Q values can range from 1000 to 3000 for ceramics, and as high as 3000 for monolithic FBAR resonators. The higher unloaded Q directly translates into lower insertion losses for the filter and steeper roll-off for improved rejection performance. Therefore, many chipset suppliers are considering integration of embedded filters into the RFIC. This approach holds some promise for simple filter applications such as GSM receiver and transmitter filters, where discrete die can be fabricated on a silicon wafer process such as FBAR, then the die can be embedded into the baseband or RFIC component. (Note: the integration of SAW filters in a similar way can be difficult due to the thermal mismatch of the quartz crystal substrate and the silicon-based RFIC.)

In FDD applications such as CDMA and W-CDMA, a duplexer is typically used to separate receiver and transmitter frequency bands. Because the duplexer must be located at the interface to the antenna, the power amplifier is naturally between the RFIC and the duplexer (Fig. 4). Therefore, for CDMA and W-CDMA, embedding the duplexer into the RFIC becomes problematic. Integration of both filter and power amplifier technologies would be necessary to make an elegant solution.

For mobile handset applications, the best compromise between performance, cost, and supplier dynamics appears to be the architecture shown in Figure 5. With an integrated baseband/RFIC chipset, the digital portion of the handset, shown outlined in green, can be driven to very low cost with high performance since CMOS process and design can be optimized for these functions. One or two separate RF front-end modules, shown outlined in blue, will take advantage of the higher efficiency performance available in GaAs power devices and the high-Q filter performance of monolithic resonator topologies.

The overall trend in mobile handset design has involved massive levels of integration over the past 15 years. That trend will continue, with performance and cost benefits for the multi-band, multi-mode handsets of the future. With the RF advancements currently in development at multiple companies today, we can look forward to handsets with 2G and 3G functionality, with room left over on board for far more memory, processing power, and more advanced applications than ever before.

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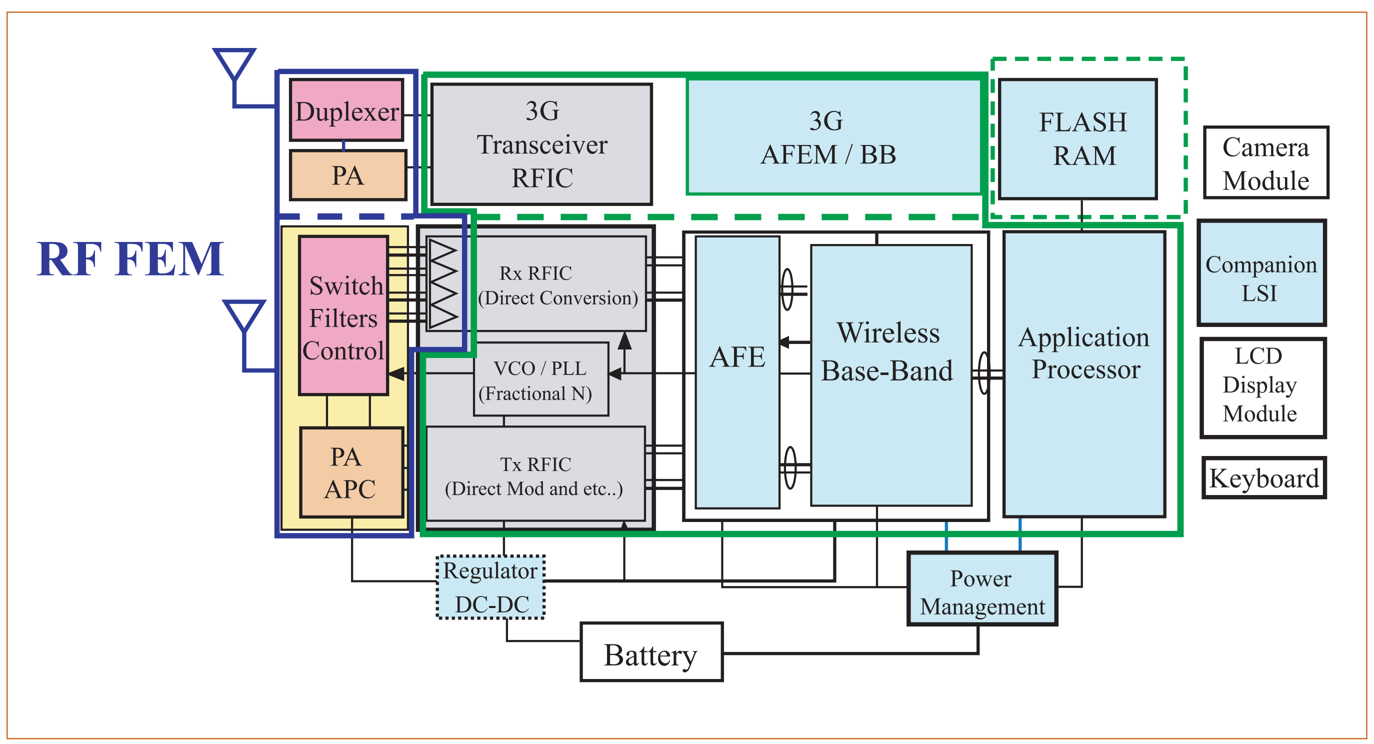

Figure 5. Future mobile handset partitioning in a dual-mode GSM and 3G handset.

Are Commercial Converters Viable in Military DC/DC Applications?

Cost and time savings can be significant

A look at the factors affecting selection of DC/DC converters for military applications and the growing attractiveness of these products.

By Martin Brabham, Military and Aerospace Industry Director, XP Power

Defence equipment manufacturers continue to be driven towards commercial off-the-shelf (COTS) power supplies to meet commercial and time-to-market challenges. The advantages are not just lower costs and better availability but also elimination of the up front expenses and risks associated with custom power supply development. But there are risks as associated with using COTS-based DC/DC converter systems too. Obsolescence, changes in specifications that invalidate end product qualification, lack of supporting data relating to military specifications and poor support from the power supply vendor who is not focussed on the defence market are all factors that need serious consideration. Are the promised benefits of the COTS route worth these new risks? The answer is almost certainly 'yes' for many applications, providing the selection task is undertaken with a clear understanding of end application and the relevant military specifications to which the end system and the power supply must conform. Of course, the choice of vendor is also important – they must have a proven track record in supplying power supplies into major military or aerospace projects.

What to look for in the specifications

Military Standards are challenging reading for even the most enthusiastic of engineers. The following guidelines are no substitute for a detailed review but they do provide a 'quick start guide' to the selection of COTS-based DC/DC converters for military applications. As in most fields of engineering, requirements are often interlinked. For example, the need for a wide range of input voltages may impact the size, efficiency and output power of a converter. As a result, a holistic approach to defining the most suitable power supply needs to be taken – some design trade-offs may be needed, but these will normally be outweighed by the many advantages of taking the COTS approach. Here are the most important considerations when selecting military DC/DC converters.

Input voltage. 28V and 270V systems are the most common in military applications. These are well defined in MIL-STD 1275A/B for Vehicles and MIL-STD 704A-F for Aerospace. A converter with a nominal input of 28V may be required to operate from 15V to 40V input. DC/DC converters with an 18V to 36V input range are commonplace, those with wider input ranges less so.

Input immunity. Spike, surge and ripple are demanding specifications for military systems. These specifications cannot normally be met by a standard COTS DC/DC converter but external filtering/conditioning modules can be used to bring converters up to required standard. Look out for converters that are available with complementary filter units – the overall performance of the power system will be dependent upon both units being properly matched.

Output voltages and power ratings. Most standard output voltages - 3.3V, 5V, 12V, 15V, and 28V- are available in COTS DC/DC converters and some manufacturers may make changes if non-standard is required. However, moving away from a standard product tends to increase the cost, lead time and risk of obsolescence. The problem is sometimes solved by using a standard part that has a voltage trim function but care needs to be taken not to get to close to OVP point when raising voltage and that reduced power is acceptable when lowering voltage.

EMI (electromagnetic interference). The most common standard for military systems is MIL-STD 461E. The choice of DC/DC converter has a major impact on overall system performance in this respect, so selecting a converter that has filters to MIL-STD 461E is an important step in reducing the risk of the system failing to meet EMI requirements.

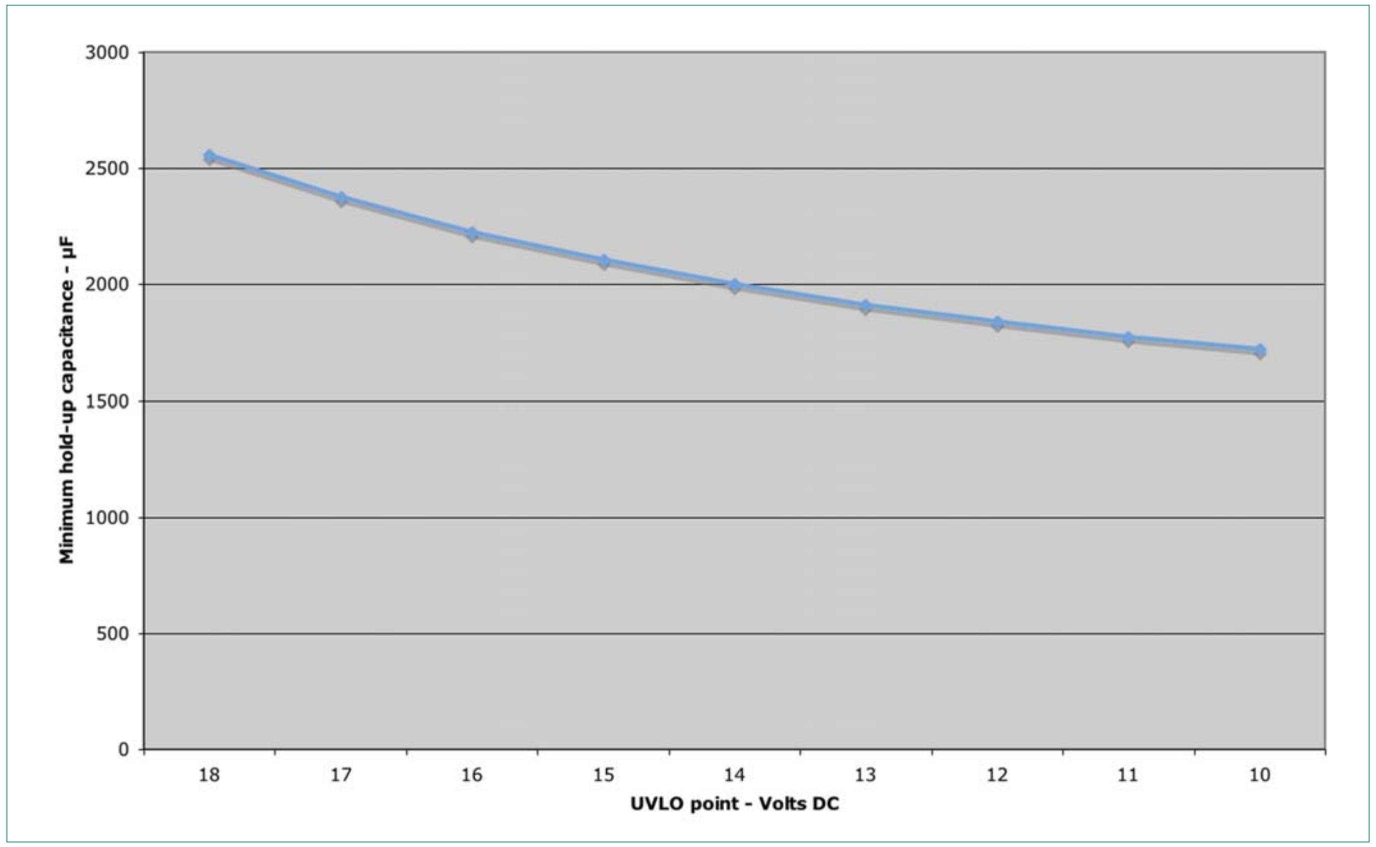

Figure 1. Hold-up capacitance vs. UVLO point @ 28V input; 85% efficiency; 50ms drop-out.

Operating and storage temperatures. Specmanship can come into play here and it pays to read data sheets with care. Some data sheets show ambient temperatures for COTS converters, others specify case temperatures or baseplate temperatures. Most military applications require converters to work within sealed enclosures and conduction is the primary cooling method. In these instances the baseplate temperature is the most useful figure to extract from the converter vendor so that heatsink requirements can be calculated. Low temperature operation, down to -55 deg C, is a common requirement in military applications. The majority of industrial DC/DC converters are not tested below -40 deg C and there can be a price premium of 30% to 40% in order to gain the extra 15 degrees for low temperature operation.

Cooling. As already mentioned, conduction is the main cooling method in military systems. Conventional heatsinks may not be needed if the system enclosure wall provides adequate thermal conductivity. The converter is simply mounted onto the heatsink or enclosure using a thermal pad or paste. Some converters are designed so that heat is dissipated through the base of the module. The idea is that heat is dissipated via the printed circuit board (PCB). This can simplify system assembly but the poor thermal conductivity of the PCB may mean that extra copper planes or heat spreading materials are needed, added to cost and complexity. In some designs convection cooling can be used, then the ambient and case temperature figures for the converter can be used to determine the most suitable cooling arrangements.

Hold-up and brown-out ride through. Military systems are often operated in circumstances where the quality and consistency of the input supply varies. The ability to handle input voltage dips or short-term discontinuity of supply is a common requirement. Most DC/DC converters will have an under-voltage lock-out (UVLO) function at their input to prevent them being damaged by excessive input current – this will cause them to turnoff during a voltage dip. A hold-up capacitor can be used to delay the voltage dropping below the lock-out point – the lower the under-voltage lock-out point the smaller the capacitor required. Of course, capacitors store more energy at higher voltages so you get less energy storage at lower voltages but it is nevertheless desirable to have a low UVLO point. Smaller capacitors mean lower cost and less board area. Figure 1 shows the capacitance needed for different UVLO points to provide hold-up for a converter running10Watts output at 85% efficiency and with a 50ms dropout from a nominal 28V input. The capacitance value shown is the minimum value required.

Size: In most designs it is desirable to keep the DC/DC converter footprint as small as possible to conserve PCB space. An important consideration in selecting a converter is that some require external components to meet the datasheet specification, so this needs to be factored into the design from both a size and cost perspective.

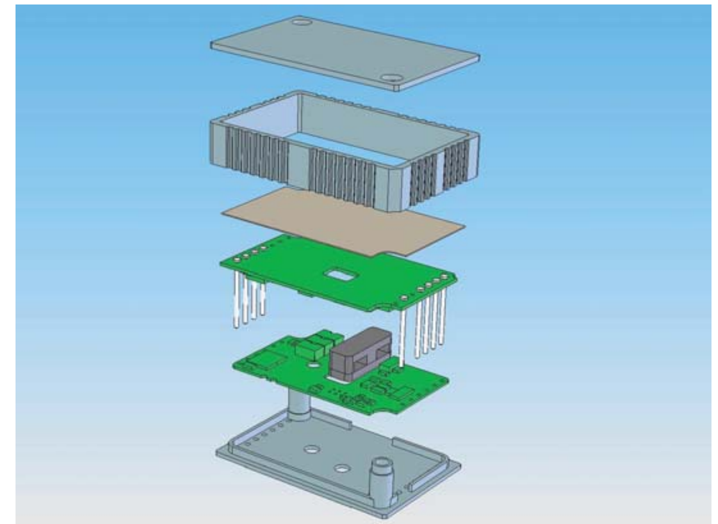

Figure 2.

Figure 3.

Protection and control/monitoring features. Over-voltage and over-temperature protection are standard requirements but these can be implemented within the converter or external to it. External protection can be more easily customized and some DC/DC converters offer internal protection that can be disabled to enable external circuits to be used. The most common control and monitoring features needed are frequency synchronization, an inhibit signal for switching the converter on and off remotely, voltage trimming, and a remote sense function that monitors the voltage at the point of load to enable the converter to automatically adjust its output voltage with varying load levels.

Type of load. The type of load - resistive, capacitive or inductive, will affect the performance of any DC/DC converter and this needs to be taken into account so that the required average power levels and transient response characteristics can be realised.

Having taken all of the above factors into account, the choice of DC/DC converter for military applications falls into 3 broad categories.

Category 1: Industrial COTS

These will be the lowest costs devices with relatively few added features. Such converters are either baseplate cooled or air cooled and the products will normally be part of a range of DC/DC modules that includes converters for telecom applications (48V nominal input), Industrial (12V and 24V) and transportation (100V nominal input). It is unlikely that there will be much supporting data to provide compliance to MIL-STD for EMI or environmental performance – although often there will be anecdotal evidence. These products have a higher obsolescence risk because commercial products typically have a shorter life-cycle than military or aerospace products – it is also more likely that the design or the manufacturing process will change over time for these products.

Category 2: Sealed MIL-STD 883 products

These are higher in cost than industrial products and are designed specifically for the military market. They are usually fully-featured and will operate over a wide temperature range, typically -55 deg C to +125 deg C and may be housed in a hermetically sealed case, or use hermetically sealed components, which makes them excellent for high reliability operation over an extended service life. EMI filtering and surge protection are normally either included or available as options. There is low risk of obsolescence as long as the PSU vendor is well known and these converters are normally available on standard military drawings (SMD), which means that companies using them can be sure of being notified of any design changes.

Category 3: Military COTS

New families of DC/DC converter that are built specifically for defence and avionics applications, without the compromises found in converters that also have to serve telecom or transport markets, are beginning to appear. These meet military specifications for EMI and environmental tolerance, have low obsolescence risk and include the full feature sets found in industrial converters. They operate over -55 deg C to 100 deg C temperature range and would, from a cost point of view, typically fall between the Category 1 and 2 types of products. Typical construction is shown in Figure 2. The products are normally sealed, although not hermetically. This is generally acceptable if the final system enclosure is sealed. They are usually available on short lead-time or from stock. EMI filters and comprehensive test data should be available from the vendor.

The final choice of DC/DC converter category will be determined by the technical and commercial requirements of the application. However, price and time-to-market considerations are likely to drive ever-increasing demand for military COTS products, such as those shown in Figure 3, as attractive alternatives to MIL-STD 883 devices in all but the most demanding applications.

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Low-Threshold Voltage MOSFETs Provide Increased Battery Life

Advanced silicon and packaging technology bring the edge in delivering power efficiency

Decreasing power consumption and extending the battery life is the goal of every design engineer working on portable electronic products. Battery technology has progressed very slowly, so designers of portable products pay a lot of attention to power management to improve battery life.

By Yalcin Bulut, Vishay

For many years, semiconductor manufacturers targeting power management applications have struggled to keep pace with the demands of end system users. An increasing number of portable electronic products, with heightened levels of functionality, demand peak performance and challenge designers to achieve the highest efficiency possible within the device's physical bounds. Although the battery industry has been making efforts to develop alternative battery technologies with a higher energy capacity than that of conventional Nickel-Cadmium (NiCd) batteries, it is nowhere close to delivering the power requirements of new-generation portable devices. Therefore, portable applications have led to innovative developments in low-power circuit designs so that design engineers can ensure that the end system utilizes battery resources as efficiently as possible. Components are a major part of the power budget in portable devices, and obviously, to keep up with that demand, semiconductor component manufacturers continue to drive innovation to help reduce power consumption in portable devices.

Taking a cellular phone as an example, reducing the operating voltage of the major components of the handset, such as the analog and digital baseband chips, is one way of reducing power consumption. When maximum performance from a DSP or microprocessor isn't necessary, the core supply voltage can be lowered to operate at a reduced clock frequency. More and more new-generation low-power applications are implementing this technique to maximize system power conservation. The formula **PC~ $(V_C)^2$.F** describes the power consumption of a DSP core, where **PC** is core power consumption, $\mathbf{V_C}$ is core voltage, and **F** is the core clock frequency. Lowering the internal clock frequency can reduce the power consumption; lowering the core supply voltage can reduce it even further.

How Advanced Silicon and Packaging Technology Can Help

While there are many design factors that affect the performance of new power-hungry portable devices, this article focuses on power MOSFETs—the most common power switches for low-voltage applications—to illustrate the impact of the latest silicon breakthroughs on increasing power requirements. In order to explain the impact of these advancements, it helps to understand some critical parameters of power MOSFETs.

Channel on-resistance ($r_{DS(on)}$) is controlled by the electric field present across and along the channel. Channel resistance is mainly determined by the gate-to-source voltage difference. When V_{GS} exceeds the threshold voltage ($V_{GS(th)}$), the FET starts to turn on. Many operations call for switching a point to ground. The resistance of a power MOSFET channel is related to its physical dimensions by the formula **R=ρL/A**, where **ρ** is resistivity, **L** is the length of the channel, and **A** is W x T, the cross-sectional area of the channel.

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance

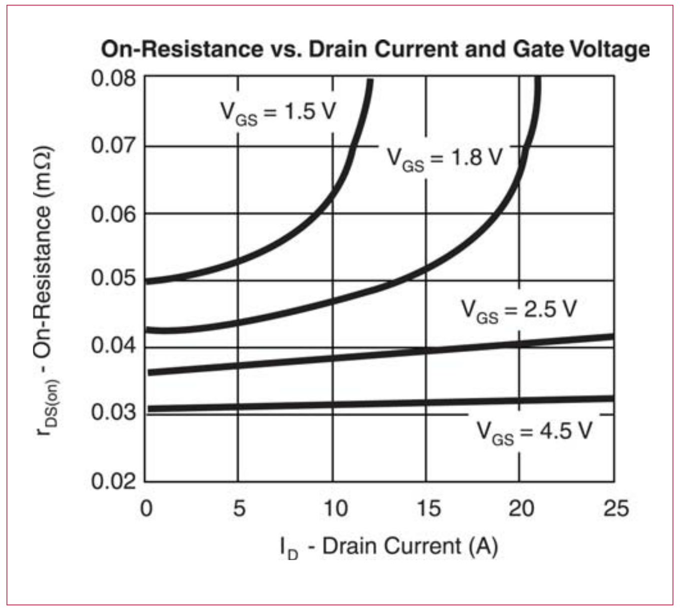


Figure 1. $r_{DS(on)}$ versus V_{GS} characteristic.

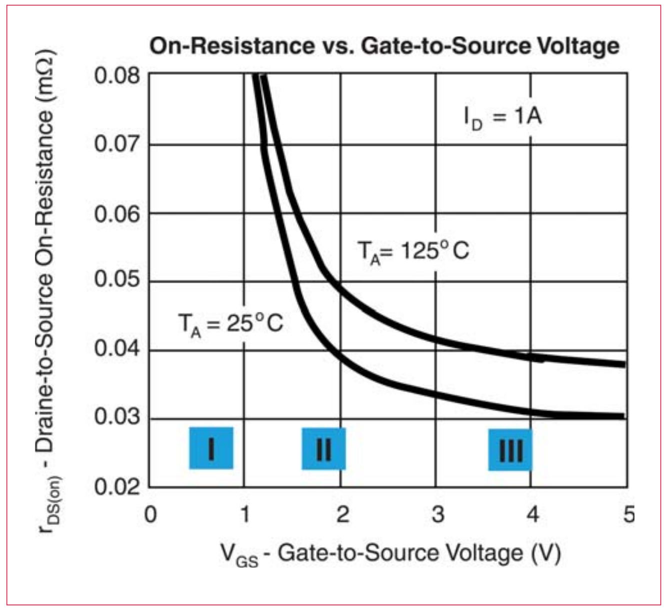


Figure 2. $r_{DS(on)}$ versus Id for different gate voltages. (Source: Vishay Siliconix Si8419DB datasheet)

between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the incremental channel resistance ($r_{DS(on)}$) approaches infinity.

Figure 1 explains the $r_{DS(on)}$ versus V_{GS} characteristic. Region I corresponds to the condition when the accumulative charge is not sufficient to cause an inversion. Region II corresponds to the condition where sufficient charge is present to invert a portion of the p region, forming the channel, but not enough that the "space charge" effect is important. Region III corresponds to the charge-limited condition where $r_{DS(on)}$ does not change appreciably as the gate-body potential is raised.

The threshold voltage ($V_{GS(th)}$) is a parameter used to describe how much voltage is needed to initiate the channel conduction. V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the "knee" of the curve (Figure 2).

High-speed performance and low-power operation can be achieved by utilizing low-threshold voltage transistors. By using low-threshold power MOSFETs in a signal path, the supply voltage (V_{DD}) can be lowered to reduce the switching power dissipation without affecting the performance. That's why, to address the ever-increasing demand to minimize power consumption and increase battery life, many of the ASICs found in portable electronics systems are designed to operate at core supply voltages around 1.5 V. Until now, however, the lack of power MOSFETs with guaranteed turn-on operation at such low voltages has made it difficult for designers to take advantage of these sub-1.8-V voltages without the use of level-shifting circuitry, which adds complexity while increasing power consumption. Vishay Siliconix is addressing this problem with a breakthrough family of power MOSFETs that are the industry's first with guaranteed on-resistance ratings at 1.5-V.

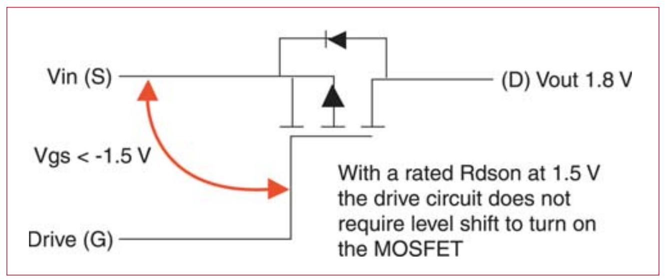


Figure 3. Reducing the $V_{GS(th)}$ point allows the driver voltage to turn on the switch from a lower-output voltage, reducing the need for a level shifting.

Historically, a threshold voltage no lower than 1.8 V was needed to accommodate the negative temperature coefficient of the threshold point that occurs in all power MOSFETs. For operation at 125 °C (which is quite possible in portable applications), the existing MOSFET designs had to maintain the MOSFET threshold high in order to prevent the MOSFET from turning itself on despite a V_{GS} of 0 V being applied.

When it comes to portable devices and cell phones in particular, there is no end in site to the demand for new multimedia features. For designers struggling to deliver higher data capabilities while juggling the unique power requirements of next-generation portable devices, however, there is little question that the advanced silicon and packaging technology of today's power MOSFETs may bring the required edge in delivering power efficiency, ultra-compact size, and low cost required to make these multimedia phones a reality.

www.vishay.com

Budgeting Power to Save World Energy

The power budget approach to power supply design

The need to save energy and minimize power supply cost, make the Budget approach a must for the Designer.

By Douglas Bailey, Power Integrations

Various governmental and standardization bodies around the world, committed to protecting our dwindling energy resources, have enacted power supply regulations to help save energy and further minimize power supply costs.

However, if the power supply efficiency regulations focus on making power conversion more efficient, but the system-level product misuses the converted power, any potential energy savings may be lost. For this reason, new regulations are emerging that define the number of watts required to power standard system-level functions. This presents the designer with more design-for-efficiency decisions ... and choices. The designer can choose whether to derive energy savings from the power supply, from the functional system, or from a combination of both.

Applying this "power budget" approach to standby power usage has resulted in the introduction of many efficient products (popularized by the 1Watt Standby movement). This article looks at a few of the more common applications where a power budget approach was used to reduce power consumption in standby modes ... and shows how the derived savings can be applied to other modes.

White Goods

Washing machines and white goods, in general, require small amounts of low-voltage DC power to operate their controls and status displays. Typically, the physical enclosure of the machine provides sufficient isolation, enabling the use of a non-isolated type of power

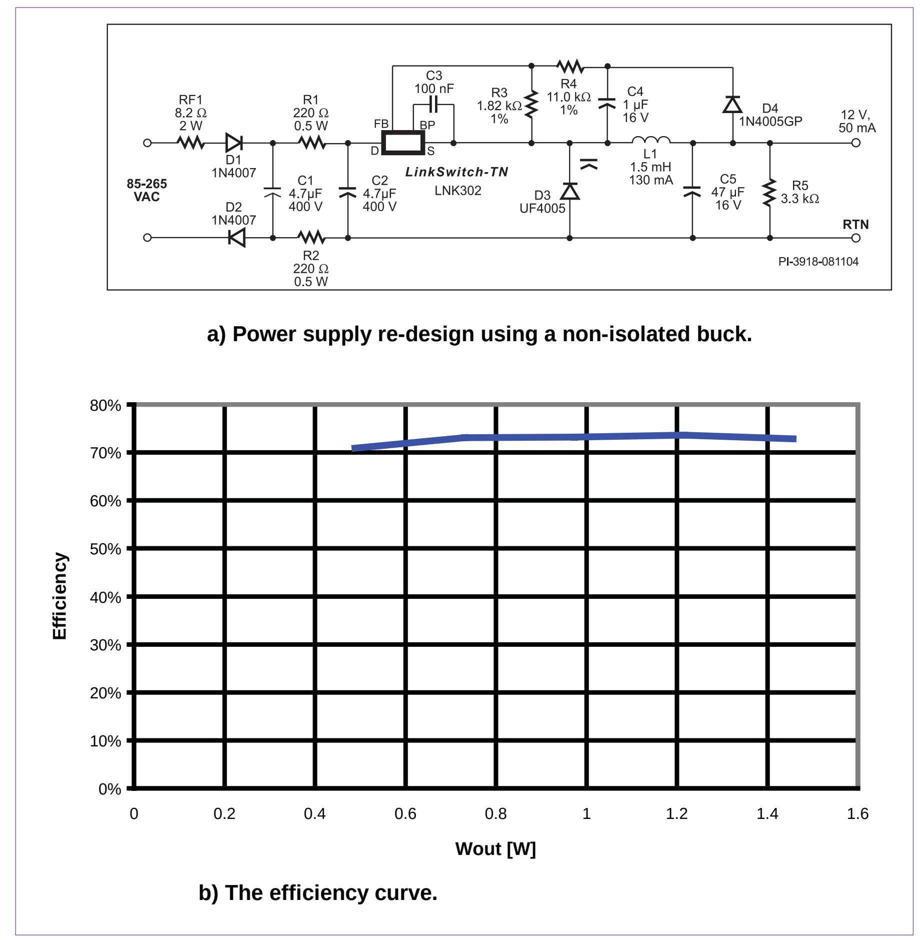


Figure 2. Efficiency curve of the non-isolated buck in the power supply.

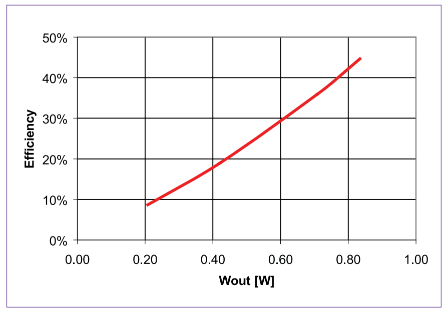


Figure 1. Efficiency curve of the post-regulated capacitor-dropper power supply.

supply that is both easy-to-implement and inexpensive.

One of the most popular types is the post-regulated capacitor-dropper (see Figure 1), which uses a minimum number of discrete components to provide the small amounts of current needed to drive the system's electronics. However, the efficiency of a cap-dropper is about 30 percent at the full load of 50 mA, making the conversion of power for the control systems extremely inefficient. In standby, the efficiency drops to 18 percent.

In the example shown in Figure 1, the 360 mW of power absorbed by the microcontroller and other electronics was costing a continuous 2 W of power drain. This equates to the energy of one wash cycle every two weeks or about 10 percent of the total energy usage of the washer over a one-year period.

To achieve a 1 W power budget on the standby power of this same appliance, the designer would have to redesign with a more efficient power supply technology. The use of a non-isolated buck (see Figure 2) can provide 720 mW of power for just 1W of input power, and free 360 mW of power for use in driving the electronics. Put in practical terms, the benefit of using the non-isolated buck in the redesign is this: any consumer wishing to use less power in standby than in wash mode can limit laundry days to a bachelor-approved "once-a-month."

Printers

The power used in inkjet printers varies from ≤ 1 W in standby mode to 70-to-80 W in peak-power mode (generally when the paper feed motors are engaged). Given this large dynamic range, the power budget for a printer is best viewed as the average of operation over a substantial period. Figure 3 shows the power usage of a typical inkjet printer.

The standby-mode functions are well-defined, and can be generally summarized as follows: check the "ON" switch for activity, and keep the "Power Connected" LED illuminated. However, printers also have a sleep mode that permits fast power-up when a print-job is issued: this mode needs to be considered when using a power-budget approach to design.

To maximize use of available power across the printer's entire power range, the power supply needs to deliver efficient power from standby to full peak-power modes.

Figure 4 shows such a power supply, designed using an integrated switch-mode IC with peak-power capability.

Power delivery, proportional to $P = 0.5LI^2f$. L (where L = transformer inductance, I = current limit, f = frequency), is predefined for the design. The current limit, which is defined in the ON/OFF control scheme, is also predefined to one of 4 levels. The integrated switch-mode IC with peak-power capability changes average switching frequency to provide variable

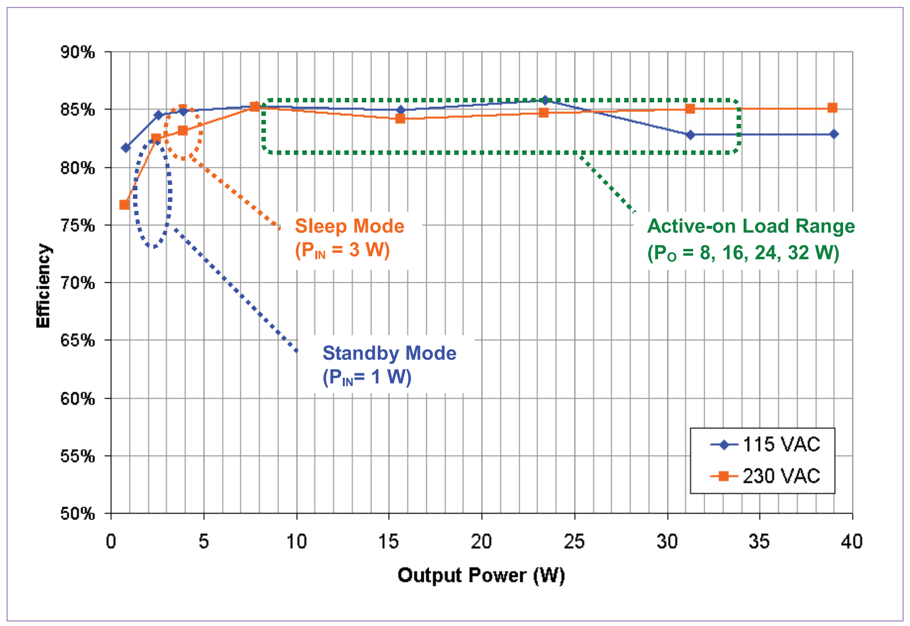


Figure 3. Power usage of a typical inkjet printer.

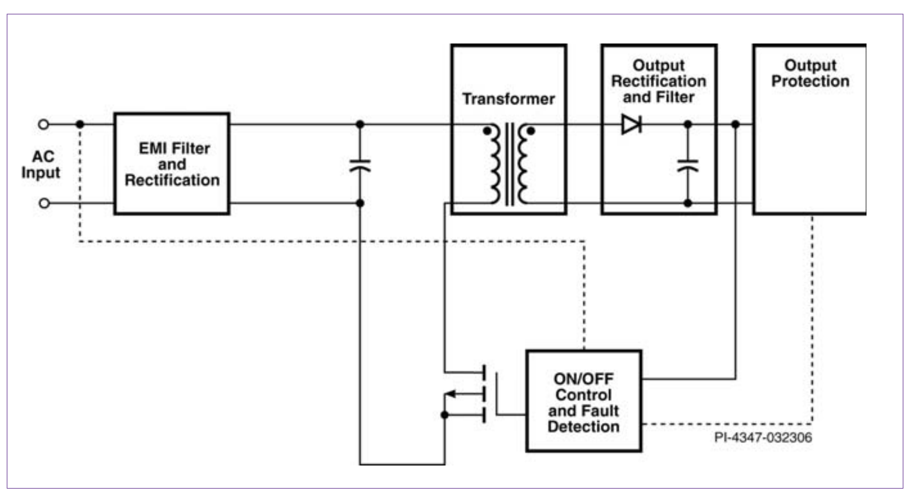


Figure 4. Power supply featuring an integrated switch-mode IC with peak-power capability.

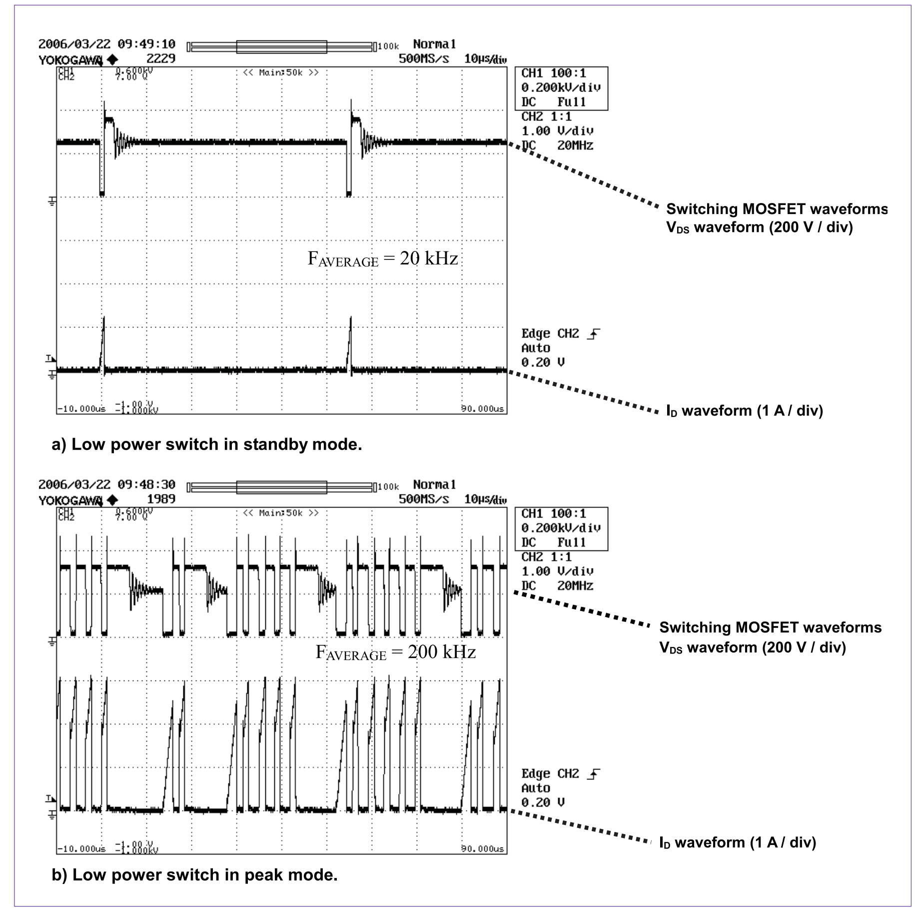


Figure 5. Peak-power management using intelligent switch-mode IC.

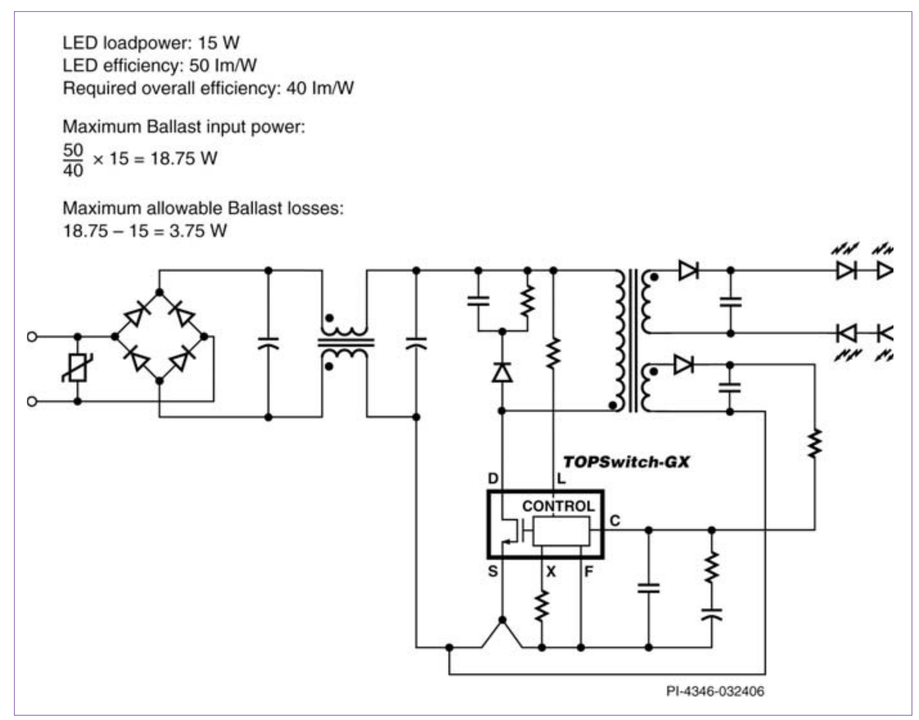


Figure 6. Power supply for an LED lighting source.

amounts of power across the range required by the printer, as shown in Figure 5.

LED Lighting

California's new Title 24 brought advancements in efficiency to residential lighting installations. The regulation requires that, under most circumstances, high-efficiency lighting be installed on the hard switch points in every room. The target for lighting efficiency is 40 lumens per watt, which is out of the range of most incandescent technologies, making fluorescent or LED lighting a necessity. The current standard, which ignores the ballast losses of the incandescent light, is likely to change to address the need to manage these losses.

LED use in general lighting is beginning to gain momentum, and can achieve 40 lumens per watt when a highly efficient power conversion technology is used. A luminaire using LED sources with a conversion efficiency of 50 lumens per watt requires a power conversion efficiency of at least 80 percent to deliver 40 lumens per watt (input power to output light). For a 15 W luminaire, this requires losses in the luminare to remain at or below 3.75 W. Figure 6 shows an example of an LED lighting source designed using this power budget approach.

Summary

New regulations are forcing engineers to apply pre-defined power budgets to their design. Optimizing for power conversion efficiency in the supply unit is no longer regarded as the only means to reduced energy usage. Given the tighter regulations governing system-level power usage, the designer must now look at ways to derive energy savings from the power supply, from the functional system, and from a combination of both. Taking a power budget approach to design results in more power-efficient products in standby mode ...and can lead to new orders of efficiency in no-load and peak-power modes, as well.

www.powerint.com

The Analog Side for 3G Mobile Power Reduction

Mixed signal and analog play their part

While functionality increases, demands for extended operation continue. Here we see how the vital Analog side contributes

By Dudy Sinai, Senior New Product Definition Engineer, Wolfson Microelectronics plc

Many of the design challenges in 3G mobile phones revolve around implementing additional functionality, such as videoconferencing, while prolonging or at least preserving battery life. On the digital side, that has led IC designers to use smaller process geometries and adopt such techniques as core voltage and clock scaling to reduce CPU power consumption.

However, since mixed-signal and analogue functions—primarily audio—account for an increasingly large part of the total power consumed, low-power design in this area is just as important. This requires a different set of techniques because shrinking transistors or lowering supply voltages has an adverse effect on mixed-signal performance. Moreover, clock scaling cannot be used on purely analogue circuitry where there is no clock.

Additionally, the pin count and printed-circuit trace totals rise as functionality increases. Groups such as the Mobile Industry Processor Interface Alliance are working to unify some of the multimedia communication buses in 3G products to save power and board space. But a highly suitable solution to the problem already exists, in the form of the well-established AC97 interface protocol.

Granular power management

Among the most power-hungry components are the loudspeakers. The small membranes and lightweight magnets of speakers used in mobile phones generally result in lower efficiency, which is difficult to improve without making the speaker unacceptably large, heavy or expensive. The audio CODECs and amplifiers driving these speakers, however, offer considerable latitude for power savings.

The three output transducers (earpiece, loudspeaker and headset) are usually driven by three separate output stages, only one of which needs to be powered up at any given time. To avoid unnecessary supply current drain, smart-phone audio ICs feature increasingly granular power management—ideally with a separate control bit for each output driver, input preamplifier, digital-to-analogue converter, analogue-to-digital converter and analogue mixer. Software designed with power efficiency in mind takes advantage of this controllability to disable any functions not currently needed.

Sample rate conversion

Another perennial problem is the requirement to record and play back audio files recorded at different sample rates. Although digital sample rate conversion can be used to make this possible, the method is computationally very expensive, slowing down the CPU and increasing its power consumption.

Two alternative methods avoid that drawback. The first is to let the audio digital signal processor (DSP) cores associated with D/A and A/D converters run at different speeds depending on the sample rate. Phase-locked loops (PLLs) provide a power-efficient way to generate the necessary clocks—usually by multiplying the word clock, whose frequency equals the sample rate, by a fixed number, such as 256.

Another method is the variable-rate audio feature built into AC97-compliant CODECs. This makes it possible to support all standard sample rates while keeping the master clock constant, at 24.576 MHz, and while transferring data across the digital interface at 48 kHz irrespectively of the sample rate.

When playing or recording audio at sample rates below 48 kHz, such as the commonly used 44.1 kHz rate, the CODEC skips sampling approximately one out of every 12 data frames and times the 11 remaining samples more evenly. Even simultaneous recording and playback at two sample rates can thus be achieved. The power consumption of the extra digital logic that implements variable-rate audio is comparable to that of one or two high-quality PLLs and is far lower than for the digital sample rate conversion performed by a CPU.

Serving two clockdomains

Opportunities for power savings also exist in the CODECs digital core. Reflecting the origin of smart phones as hybrids between traditional mobile phones and PDAs, today's typical audio subsystem consists of a mono voice CODEC and a stereo, hi-fi CODEC, which may or may not reside on the same piece of silicon. Although they are interconnected in the analogue domain, each CODEC has its own digital core and audio interface, and is slave to its own clock domain. The voice clock is synchronized to the communications processor; the hi-fi clock is derived from the applications processor.

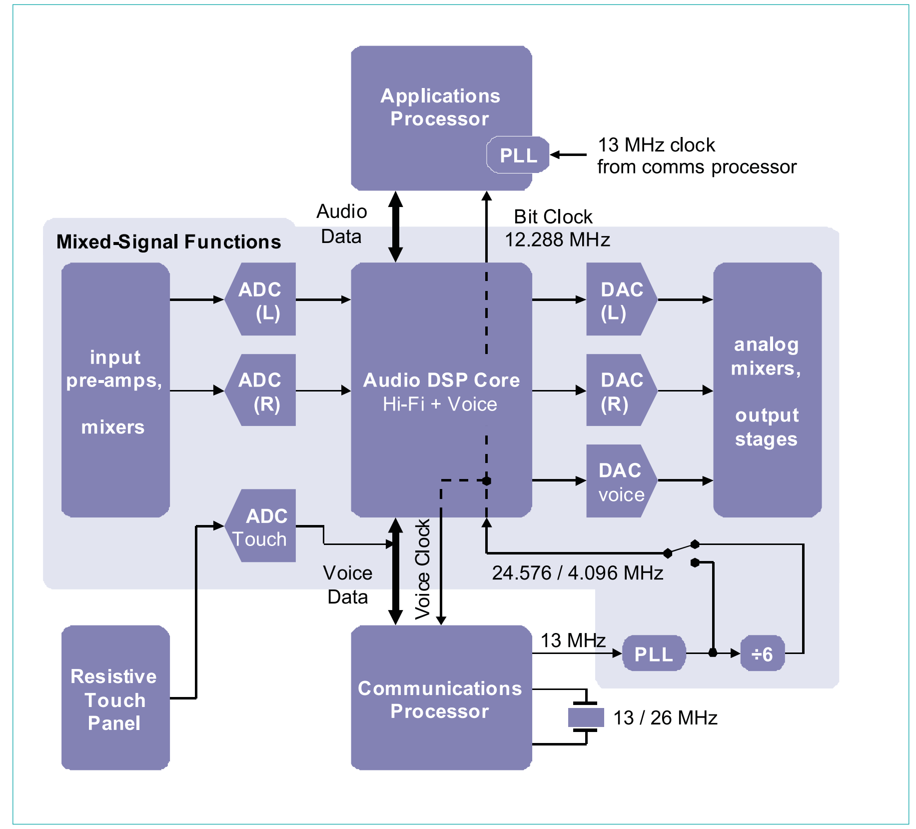


Figure 1. Single Core Architecture (e.g. WM9713L).

Besides increasing chip size, this architecture also results in two cores running simultaneously when music, MP3 ring tones or other signal tones are played during a call, as well as in phone call recording. While sample-rate conversion combined with digital mixing could unify the two audio streams for processing in a single CODEC, the power consumed in the process would far outweigh any power savings achieved through the elimination of one CODEC.

There is, however, another approach which only requires a single audio DSP core, while preserving separate D/As and analogue signal paths. AC97 CODECs are particularly suited to this because, as discussed above, the variable-rate audio mechanism keeps their master clock constant, at 24.576 MHz. With the hi-fi clock thus fixed at one frequency, the voice clock can be locked to it as a fixed ratio: Dividing the 24.576 MHz hi-fi clock by six yields a 4.096-MHz voice clock (512 times the standard telephony sample rate of 8 kHz). By generating the clocks on-chip and operating as clock master on both audio interfaces, the audio subsystem eliminates any frequency mismatch that might otherwise result in unintentionally dropped samples and thus in audible distortion (see figure).

The single-core architecture saves power whenever both audio streams are active. Playback during a call is achieved using just one audio DSP core, operating at 24.576 MHz, whereas the dual-core architecture also requires a second core, running at 4.096 MHz, and thus consumes extra power.

For phone call recording, the AC97 interface is slowed to one-sixth its normal speed, so that it becomes synchronous with the voice interface. One A/D converter can then be used to digitize the microphone signal and feed the data to the baseband chip set, while another A/D, using the same clock, captures an analogue mix of both sides of the phone conversation for recording through the AC97 interface under the control of the applications processor. The same scenario in the Dual Interface CODEC Architecture would have required a separate DSP core for the second A/D, running at the frequency dictated by the applications processor.

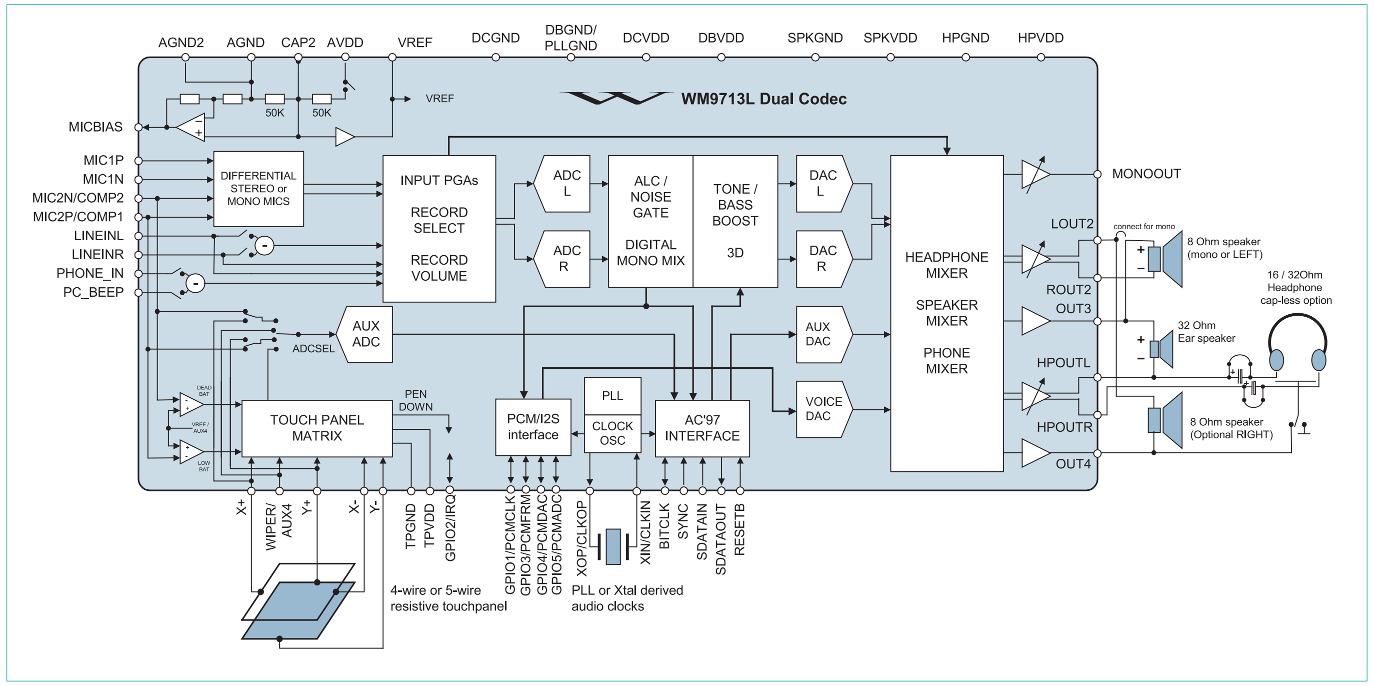


Figure 2. WM9713 AC97 PCM and hi-fi Touch-CODEC.

The single-core implementation also requires less silicon. Besides the gate count reduction due to the elimination of one audio DSP core, an A/D is eliminated.

Touchscreen digitization

Many 3G phones feature touchscreen interfaces to allow for more intuitive user interaction. The digitization of the touchscreen signal needs only a relatively slow, low-resolution A/D converter, but some details of its implementation can significantly affect overall power consumption in the system.

To measure touch coordinates, a current must be driven through the resistive layers of the touchpanel that overlays the screen. The current far exceeds the A/D converter's supply current and should therefore be minimized. Factors affecting this current are the frequency of measurements and the delay between driving the touchpanel and taking a measurement. Both also affect the accuracy of measurements, and a minimum sample number is necessary to achieve a responsive user interface.

Pen-down detection is another concern with touchscreen displays. Many touchscreen controllers rely on a polling routine whereby a CPU regularly checks whether the screen is being touched. Such polling prevents the CPU from remaining in sleep mode when there is no user input and thus increases the CPU's power consumption.

With touchscreen controllers capable of independently detecting pen-down and sending an interrupt, the CPU can spend more time in sleep mode. The same pen-down signal can also be used to control the touchpanel driver circuits and A/D converter, ensuring that they run only when necessary.

Flexibility in the interpretation of the AC97 interface specification makes it easy and very efficient to control and transfer touchscreen digitizer information over the same four-wire ac link bus that transfers the audio data and control, thus saving on the need to connect to a separate touch digitizer chip.

The future

Because the AC97 interface might be used for data other than solely audio or modem data, and because the 48k frame-per-second frame rate is sufficient for foreseeable needs, other functions within the 3G phone could conceivably use this bus for transfer of control and system data. Once we break free of the limits of using AC97 only for audio, then other benefits become apparent.

For example, power management functions could easily be transferred over the excess bandwidth of the ac link. If this happens while audio or touch functions are asleep, then the ac link could run at very low speeds, thereby saving power.

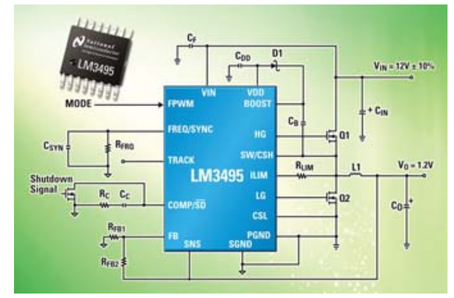
Further, the inherent sleep and wake-up protocols built into the ac link specification are well-suited to building very low-power multipurpose communication subsystems.

This extended interpretation of the usability of the AC97 interface opens the way to further

beneficial reductions in system power consumption and board area, and should be considered as an attractive future component of 3G phone architectures.

www.wolfson.co.uk

PWM Controller Utilizes Unique, Low-Noise, Emulated-Current-Mode Architecture for Design Flexibility



National Semiconductor has introduced a new pulse-width modulation (PWM) buck controller employing National's unique emulated-current-mode (ECM) architecture for output voltages with extremely low duty cycles at frequencies up to 1.5 MHz.

The LM3495 powers digital application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), digital signal processors (DSPs) and other embedded processors.

Deep sub-micron ICs require tight regulation accuracies and the LM3495 offers industry-leading accuracy of +/- 1 percent over a wide temperature range. In addition to a host of system integration features, the LM3495 addresses the needs of point-of-load (POL) module manufacturers with fault-protection features that ensure a reliable end product.

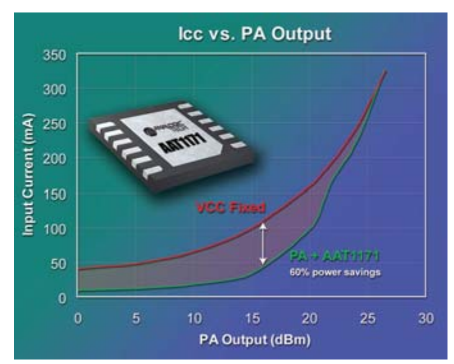
This new device gives designers a choice between the company's new ECM architecture and existing voltage-mode portfolio, the LM274x family. Both architectures allow designers to reach very high operating frequencies and conversion ratios without having to deal with switching noise problems.

The LM3495 has an input voltage from 2.9V to 18V for use in 3.3V, 5.0V, 12V and intermediate-bus systems, as well as an output voltage that is adjustable from 0.6V to 5.5V for existing and future core and I/O voltages. The controller has low-side sensing and a programmable current limit that does not require a sense resistor allowing reduced power dissipation, component count and system cost. In addition, the LM3495 has input under-voltage lockout, switch-node short protection, adaptive duty cycle limit and hiccup-mode current limit protection that eliminates thermal runaway during fault conditions. It also has an internal soft start with tracking capability.

The LM3495 has a 200 kHz to 1.5 MHz switching frequency that can be synchronized to reduce radiated system noise. Its on-chip gate drivers are capable of driving FETs suitable for output currents in excess of 20A. The LM3495 has soft shutdown and glitch-free start-up into pre-biased loads to ensure deep sub-micron cores are not damaged. Available in a TSSOP-16 package, the device operates from a single input rail, eliminating the need for an external bias supply.

www.national.com

Efficient step-down converter for WCDMA & CDMA PA



AnalogicTech has introduced the AAT1171, a fully integrated voltage-scaling DC/DC step-down converter optimized to control the power amplifier (PA) in WCDMA and CDMA handsets. By dynamically controlling the operating voltage of the PA in mobile phones, the device increases amplifier efficiency and extends talk time.

The conventional WCDMA handset transmit profile operates the PA at approximately +16dBm output power for approximately 50 to 60 percent of its operating life. When powered from the AAT1171, instead of being powered directly from the battery, the PA consumes 60 percent less power at this +16dBm level, enabling longer battery life, smaller batteries, and thus smaller and lighter mobile phones.

The device operates across a wide voltage input range of 2.7V to 5.5V. Its input voltage is controlled by a real-time output signal from the baseband processor and delivers up to 600mA of continuous load current.

By supplying a variable output voltage of 0.6V to 3.6V, the AAT1171 optimises PA efficiency at both low and high transmit levels. To meet stringent WCDMA requirements, the output voltage responds in less than 30 microseconds. To improve efficiency even further, the IC provides the lowest quiescent current available under both full and light load conditions. The no load quiescent current is 45 microamps (typical).

The AAT1171 also maximizes efficiency and extends handset talk time by providing an integrated 85mohm bypass MOSFET. When transmitting at full power, the MOSFET switch bypasses the DC/DC converter and output inductor to provide a low resistance path between the battery and the PA, allowing the system to operate very close to the minimum battery voltage. The switch is activated by setting the bypass input high, or forcing the baseband DAC voltage output to 1.3V.

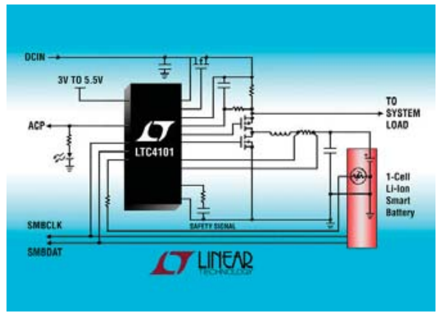
Operating at 2MHz switching frequency, the AAT1171 allows the system designer to use a small 2.2µH inductor and 4.7µF capacitor on the output. The IC also features current-limiting, short-circuit and over-temperature shutdown protection circuitry to ensure device integrity.

Specified over the -40 to +85 degrees C temperature range, the AAT1171 is immediately available in a Pb-free, 12-pin TDFN33 package.

www.analogictech.com

NEW PRODUCTS

4A 1-Cell Li-Ion SMBus Battery Charger Needs No Microcontroller



Linear Technology Corporation announces the LTC4101, a fast, precision smart battery charger controller that operates with or without a host microcontroller. The IC is fully compliant with Rev. 1.1 SMBus specifications and meets the requirements of Smart Battery System (SBS) Level 2 charging functions. It is optimized for 3V to 5.5V charging voltages and suitable for 1-cell Li-Ion and 3- to 4-cell nickel-chemistry batteries. Fast charging up to 4A with 0.8% voltage accuracy and 4% current accuracy is achievable. Synchronous switching operation provides high efficiency charging from a wide input supply voltage range of 6V to 28V. The LTC4101 is housed in a small 24-pin SSOP package and is ideal for use in portable computers and instruments.

For flexibility, the LTC4101 integrates a 10-bit DAC for charge current programming and an 11-bit DAC for charge voltage programming. Using the charger's input current limit feature, a maximum charge rate is achieved without overloading the input supply, such as a wall adapter. The SMBus interface remains alive when the input power is removed and responds to all SMBus activity directed to it, including SafetySignal status, which in tandem with the IC automatically monitors the battery temperature, connectivity and battery type information.

The LTC4101 is rated for operation from -40°C to 85°C.

www.linear.com

New Voltage Regulator Shrinks Portable Devices

STMicroelectronics introduce an advanced high-frequency step-down DC/DC converter particularly suited for use in data-storage applications, such as hard disk drives, DVDs, Blu-ray Discs, High-Definition DVDs, and in portable devices, such as MP3 players and digital cameras, that require high efficiency, small size, and light weight.

The new ST1S06 includes a synchronous rectification block to avoid the use of an external Schottky Diode while improving the device's efficiency up to 95%.

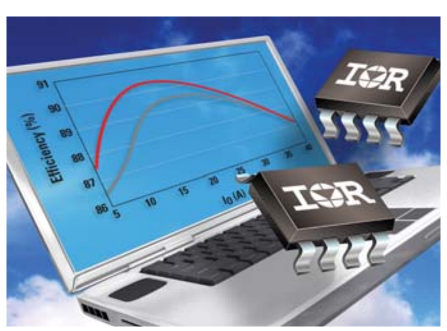
Other key features of the ST1S06 include an output current capability of 1.5A maximum over all operating conditions, a high switching frequency of 1.5MHz and great stability, allowing a drastic reduction in Printed Circuit Board (PCB) area. The high frequency performance allows the device to operate with a small inductor, while the high stability permits the use of small, low-ESR, ceramic capacitors. As a result, the ST1S06 requires only a few external components to operate: the small inductor, two capacitors and, for the adjustable version, two resistors.

The device provides a soft-start, minimizing start-up problems in battery-powered devices and is available with fixed output voltages or in the adjustable version using an external resistor divider.

Built using ST's proprietary BCD6 smart-power technology, the ST1S06 is offered in two versions: with and without an enable feature. Both versions are available in the increasingly popular tiny DFN6 3 x 3mm ECOPACK® package. The voltage regulator can be combined with several codified versions of a demo board for evaluation purposes. The demo boards are orderable in the ST web site.

www.st.com

New MOSFETs for high efficiency DC-DC buck converters



International Rectifier has released the IRF7835PbF and IRF7836PbF, 30V synchronous buck HEXFET® MOSFETs for DC-DC synchronous point-of-load (POL) converters. The SO-8 synchronous MOSFETs are designed for applications where requirements of small size, high efficiency and improved thermal conduction resulting in increased power density are desired, such as point-of-load (POL) converters and notebook microprocessor power supplies used in high-end servers, as well as advanced telecom and datacom systems.

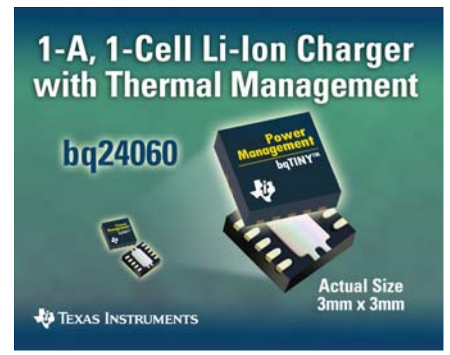
Reducing total gate charge (Qg) up to 25%, optimizing the body diode losses and maintaining similar $R_{DS(on)}$ performance as previous devices, improves critical light-load efficiency in battery-operated systems by as much as 1.5%.

The new IRF7835PbF targets the latest generation of mobile processors requiring a thermal design current of 35 amps from a two-phase voltage regulator using one control and two synchronous MOSFETs per phase. The device may be used in applications up to 11A per MOSFET. The new IRF7836PbF is designed for power rails using a single control and a single synchronous MOSFET, and may be used in applications up to 9A per MOSFET.

These devices are RoHS-compliant. Data sheets are posted on the International Rectifier Web site.

www.irf.com

Li-Ion Battery Charger with LDO Mode and Thermal Management



Texas Instruments introduces a new 1A, bqTINY™ single-cell lithium-ion (Li-Ion) linear charger with enhanced thermal fold-back regulation and low dropout power management. The new 3mm x 3mm device will enable personal digital assistants (PDAs), cell phones, digital cameras and wireless headsets to charge more safely and efficiently from a battery charge cradle or AC adapter.

The bq24060 battery charger with integrated 1A power FET and current sensor can withstand an input voltage of up to 26-V. Designed to extend battery life, the device offers complete charge management capability with unique safety and low-dropout features. The bq24060 charges the battery in three phases required by battery cell manufacturers, including pre-charge conditioning, constant or thermally regulated current and accurate constant voltage. The charger's algorithm reduces charge times, maximizes total charge and protects the battery from thermal and electrical dangers. The device re-starts the charge when the battery voltage falls below an internal threshold, and it enters a low-power sleep mode when the external input supply is removed.

A reverse-blocking protection scheme is integrated to prevent battery drainage in the absence of DC supply. In addition, the bq24060 can be configured to operate in LDO mode to allow the system to fully operate without the battery. This is also useful for board test before complete system test during the end-equipment manufacturing process.

The devise features over-voltage protection for the charger and the system during high-voltage conditions by quickly disconnecting them from the adapter. In addition, enhanced thermal fold-back regulation allows it to run continuously in harsh environments where ambient temperature is high, such as in an automobile, or when connected to an incorrect adaptor with a higher input voltage.

The bq24060 charger and evaluation modules are available from TI and its authorized distributors. The device comes in a 10-pin, 3mm x 3mm MLP package.

www.ti.com

NEW CONSTANT CURRENT DRIVERS DELIVER FIXED 100mA OUTPUT

Supertex, Inc. introduces CL6 and CL7, two linear, constant current, LED drivers with fixed output currents of 100mA. The devices are ideally suited for applications using 24V/48V inputs.

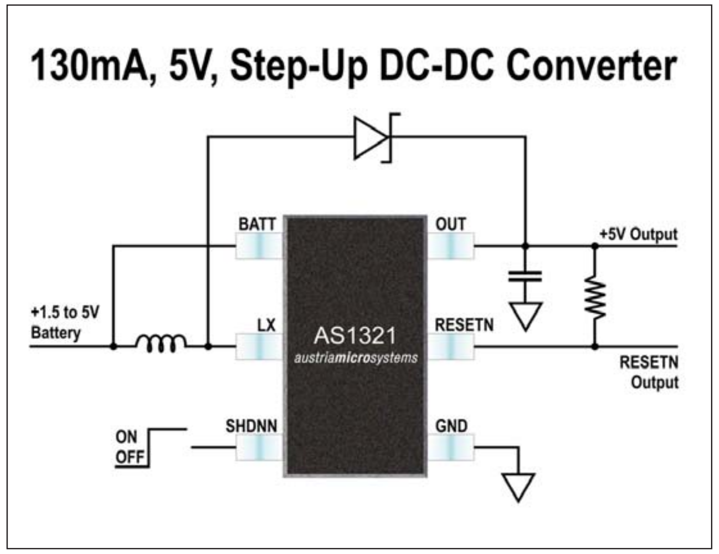
Both devices feature built-in reverse polarity protection and over-temperatureprotection. With maximum ratings of 90V, they are able to withstand transients without any additional protection circuitry when used as recommended.

The CL7 also features an active low enable input pin allowing logic level control of the LED for on/off or PWM dimming control. "The introduction of CL6 and CL7 further broadens Supertex's family of high performance LED drivers," states Ahmed Masood, Vice President of Marketing for Supertex. "CL6 and CL7 are simple, easy-to-use devices that provide constant current output and low EMI noise in 24V/48V LED lighting applications."

CL6 is available in D-PAK (CL6K4-G) and three lead TO-220 (CL6N5-G) packages. CL7 is available in a power SO-8 (CL7SG-G) package. They are all Green and RoHS compliant. Samples are available from stock.

www.supertex.com

5V 130mA step-up DC-DC converter for size and power critical applications



Austriamicrosystems announces the AS1321, a high efficiency step-up DC-DC converter with a fully integrated synchronous rectifier.

The AS1321 improves on the excellent performance of the existing AS1320 while boosting the output voltage to 5V. With a supply voltage of 1.5 to 5.0V the IC is capable of delivering a 130mA output current at 2V input voltage. With an efficiency of 96% it provides the ideal solution for battery powered portable applications that require a 5.0V supply voltage.

"The high output current combined with the low power consumption makes the AS1321 an ideal solution for battery powered devices such as medical and diagnostic devices, digital cameras, PDA's and smart phones, cordless phones and other handheld products," said Walter Moshammer, marketing director for standard linear at austriamicrosystems. "The IC is also particularly well suited for dual-cell powered battery devices."

A shutdown mode drawing less than 1uA is also available. In this mode the battery is connected directly to the output to enable direct battery feed-through. This enables the input battery to be used as backup or as a real-time clock supply when the converter is off and eliminates the need for a costly back-up battery. To ensure stable operation the integrated power on reset circuitry enables the AS1321 to reset any type of microprocessor after power up ensuring a stable start in all devices.

The device is available in SOT23-6pin packaging.

www.austriamicrosystems.com

Companies in this issue

Please note: **Bold**—companies advertising in this issue

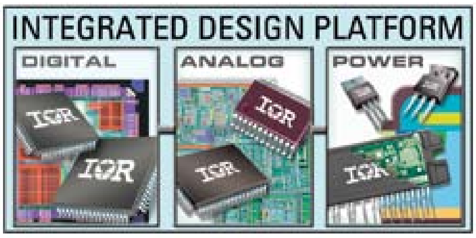
SIMPLE, SENSORLESS CONTROL FOR DIRECT DRIVE WASHERS

Simplify Design, Improve Efficiency, Accelerate Time-to-Market

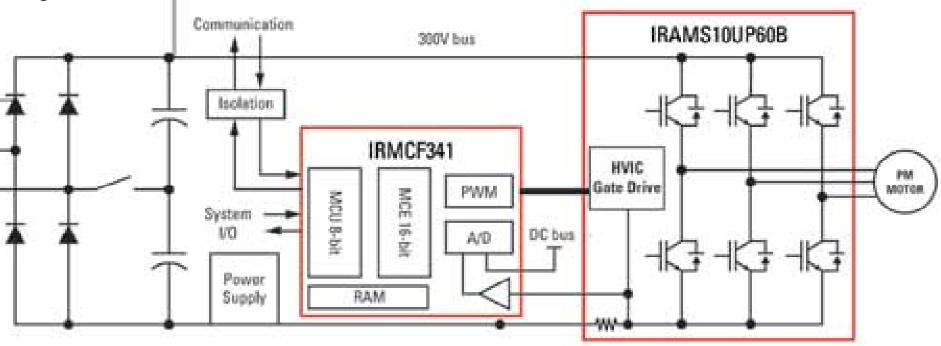
iMOTION™

DIGITAL

- Motion Control Engine™ (MCE) eliminates Hall Effect sensors
- Integrated microcontroller enables application layer software development
- No coding, simple graphic block editing

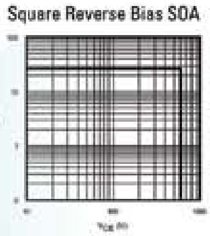


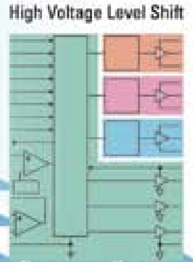
LEAD FREE



ANALOG

- Analog Signal Engine™ (ASE) integrates all signal conditioning and conversion circuits required for single current shunt
- Industry-leading high voltage technology





POWER

- Utilizes three-phase monolithic gate driver IC matched with highly efficient Trench IGBTs
- Insulated metal substrate technology for reduced EMI
- Replaces over 20 discrete parts

IR's *iMOTION* simplifies design of variable speed motor control in horizontal and vertical axis washing machines to improve washing cycles and save up to 70% of energy usage.

With *iMOTION*, you can design a system that:

- Turns a motor for evaluation in days instead of weeks
- Performs more efficiently without added system cost
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