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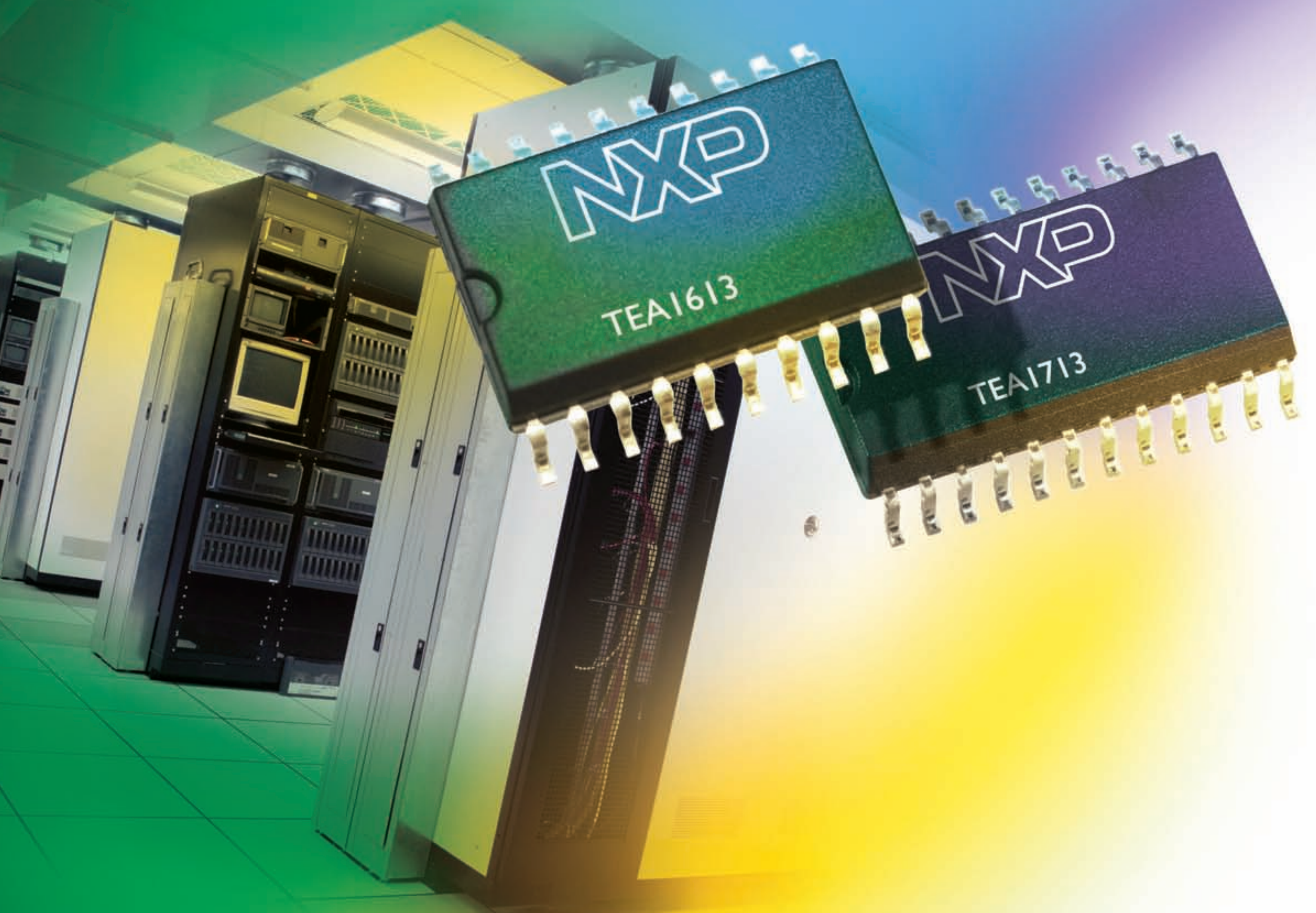
March 2009



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Special Report - Digital Power

ISSN: 1613-6365

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Power Systems Design
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Registration of copyright: January 2004
ISSN number: 1613-6365

Send address changes to:
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Volume 6, Issue 2

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Cover graphics courtesey of Analog Devices, Inc.

The Digital Divide Softens

Now with the year in full swing, it's not a pretty or hopeful sight. The problems in the economy, world instability and our own industry 'knee jerking' as ever as an almost regular reflex-action in an attempt to contain and slash costs. Some of the outcomes have been brutal for us.

True, we have a business climate that is extremely tough. It is just the hard face of commerce where often good people are let go. The thing to remember, no matter what the current scenario, is that the business will, over the long haul, thrive and grow. As Intel's CEO said recently "All cycles end". OK, we have a problem at the moment where companies feeling the dramatic decline in orders and sensitive about shareholder value, will be relentless in their quest to re-assure them by making informed and dramatic financial cuts. I would guess though, that the huge future cost-burden to these companies of the inevitable compensation shortly to be followed by intensive restructuring, rehiring and retraining when the industry recovers, is not even a consideration at the moment. The resurgence will, I guess, pay for it…

The broad area we call 'digital power' is now accepted in the industry as having its rightful place and is no longer a dirty word. Even the designers, who were once skeptical and did not believe there was a real need, are now taking notice. And digital power companies on the other side who were trying to convince everyone that this was the way to go, have been very smart to give designers, who are not 'digital experts' the tools to be able to help them to utilize the benefits of digital power into their new designs. Control and respect for power has entered a new dimension. With the focus on energy 'wisdom' and conservation, together with the need to deliver the required performance at the right cost in today's environment, the real-world benefits are not difficult to see, to believe and to implement.

I'd like to extend a welcome to Mike Noonen, Senior Vice President, Global Sales & Marketing at NXP, to PSD's advisory board. Mike's experience and judgment will be extremely valuable.

In this issue we have a selection of editorially requested and contributed articles with features to follow our theme of digital power. I have also given account of the new launches together with my interviews and company announcements over the past month.

I hope you enjoy this issue. Please, as ever, let me know about your design ideas, solutions and projects for editorial inclusion and do keep your feedback coming. It is of immense value in tailoring the magazine to fit engineering needs and to that of your colleagues.

Don't forget to check out our fun-strip Dilbert at the back of this issue.

All the best!

Cliff Keys.

Editor-in-Chief, PSDE
Cliff.Keys@powersystemsdesign.com

ABB Wins €123 Million Efficiency & Productivity Contract

ABB, the leading power and automation technology group, has renewed an agreement worth about €159 million over the next five years to manage maintenance and increase productivity at several plants in the Werk Bobingen industrial park near Munich, Germany.

ABB, a leader in power and automation technologies that enable utility and industry customers to improve performance while lowering environmental impact, will provide performance-based maintenance services at the site for polyester product manufacturers Johns Manville, Performance Fibers, Trevira and Teijin Monofilament. ABB will evaluate plant processes to improve efficiency of maintenance and repair operations, maintain power generation and distribution facilities, and infrastructure such as fire protection and site security for the entire 80-hectacre complex.

Bobingen industrial park near Munich, Germany.

"ABB's combination of innovative service solutions, local knowledge and unsurpassed application experience has helped us build an effective relationship with customers at this site," said Veli-Matti Reinikkala, head of ABB's Process Automation division. "Our reputation for delivering results has been crucial to maintaining this successful partnership over the years."

ABB has more than 150 similar strategic full service agreements with customers in the paper, mining, chemicals, and oil and gas industries globally. ABB best practices applied to maintenance operations improves the performance and reliability of production assets, increasing plant efficiency and reducing costs so that customers can focus on the their business, adding new value to their bottom line.

www.abb.com

CamSemi Appoints Top Exec from iWatt

CamSemi, a leader in power management ICs for optimised energy-efficient off-line power conversion, has appointed Mark Muegge as the company's VP Marketing. He joins with immediate effect to take charge of all corporate and product marketing activity and to help define the next generation of power management ICs that will be critical in further strengthening CamSemi's growing market position and sales.

Muegge brings over 20 years' semiconductor industry experience into the company and an exceptionally strong profile and background in the power supply controller market. He was the first employee to join iWatt's founders in 2000 and co-invented its primary side sensing technology to develop simpler, safer and lower cost power supplies. He built and led the company's engineering team which designed several high-performance controllers. Prior to joining CamSemi, he was Director of AC/DC Products overseeing the marketing and development of the largest part of iWatt's product portfolio.

Mark Muegge VP Marketing, CamSemi.

"Mark is joining CamSemi at the perfect time as we look to expand our product lines, develop our share of the power supply controller market and target new market opportunities. His track record of success, in-depth market knowledge and first-class engineering skills are invaluable and will have an immediate impact in building on our achievements to date," said David Baillie, CEO of CamSemi.

In addition to iWatt, Muegge has held a number of senior marketing and engineering roles within the industry including: Hi/fn where he defined the company's flagship security co-processor product; Quality Semiconductor, the logic chip and speciality memory manufacturer; and communications IC supplier IDT. He started his engineering career at AMD following a BSEE degree from the University of California, Davis.

www.camsemi.com

Digi-Key Corporation Expands Cree Product Line to Include Gallium Nitride (GaN) HEMTs

Digi-Key Corporation and Cree, Inc. have announced that Digi-Key is now stocking Cree's Gallium Nitride (GaN) HEMT transistors for general purpose microwave applications. Digi-Key's portfolio of Cree offerings encompasses SiC power components, SiC MESFETs, high-brightness and high-power LEDs, and now, GaN HEMT transistors.

Cree's GaN HEMT general-purpose transistors, in power levels ranging from 10W to 90W, are ideal for microwave applications that require high efficiency, multi-octave bandwidth performance. These transistors offer high frequency performance to 6GHz, high gain, and low parasitic capacitance within small package footprints. This enables smaller, lighter, and more energy efficient systems, often with fewer amplifier components, than required with other microwave transistor technologies.

"We are pleased that Digi-Key is stocking Cree GaN HEMT transistors," said Jim Milligan, Cree's director of RF and microwave products. "Digi-Key has the distribution expertise and industry channels to help accelerate the adoption of our GaN HEMT technology."

Digi-Key President and COO Mark Larson commented, "Relied upon by engineering and purchasing communities for product selection and availability, Digi-Key is committed to providing its customers with the latest and most sought-after technologies. To that end, we are very pleased to make Cree's GaN HEMT transistors available to our customers."

www.digikey.com www.cree.com

Rutronik and Intersil Enter European-Wide Agreement

Rutronik Elektronische Bauelemente GmbH has entered into a European-wide franchise agreement with Intersil, one of the leading manufacturers of high performance analogue products. Deliveries of supplies to European customers and their production facilities throughout the world started January 2009. Rutronik now has the full bandwidth of analog components in its portfolio.

The Intersil portfolio of analogue and mixed signal products with its focus on application-specific products (ASSP) and standard products for a wide field of applications is the ideal solution to plug the gap in Rutronik's analog portfolio. As part of its Fab-Light strategy Intersil uses some very diversified analog manufacturing processes and, in parallel, leading external analog & mixed signal foundries. In this way Intersil's high speed and high precision components will be able to offer Rutronik customers even greater competitive advantages and an extremely high level of innovation. Power Management products in the low voltage sector round off Intersil's range of products. The target markets at which the full portfolio is aimed are industrial applications, communications, computing and consumer applications.

"We are particularly looking forward to this co-operative venture", commented Markus Krieg, Marketing Director at Rutronik. "With Intersil we are able not simply to offer our customers high-performance alternatives to the few high performance analogue and mixed signal manufacturers on the market but also, Intersil is more of a partner that, with its product strategy, delivers even more system expertise on the user market than other analog broad-liners. With the Intersil portfolio we will in future be able to cover the entire analog signal chain. We are certain that together we will be able to develop business significantly and consistently gain a greater market share in Europe."

Markus Krieg, Marketing Director at Rutronik.

Intersil benefits from the distributor's existing analogue organisation, which is opening up a wide base of customer potential to the manufacturer. The customer structure of the two companies is mainly within the industrial applications and communications segments. "Rutronik is now another strong Design-In partner for us in Europe," stated Peter Schubert, Sales Director Distribution Europe at Intersil. "Our products have truly unique properties within Rutronik's portfolio. We are extremely pleased about this. Together we shall build up our joint market presence on the high performance analogue market.

www.rutronik.com

www.intersil.com

Vincotech Names Joachim Fietz Managing Director

Vincotech, a provider of power modules and other technologies used in industrial, solar, automotive and GPS applications, today announced that its board of directors has named Joachim Fietz managing director. Fietz, 50, will be based at the company's Unterhaching, Germany headquarters and will report to the board of directors. Vincotech is owned by The Gores Group, Los Angeles-based private equity firm.

During his 20+ year career, Fietz has held various senior-level leadership positions in engineering, sales and operations. He most recently served as chief executive officer of Innominate Security Technologies AG, a Berlin-based company which develops and sells advanced network security products to global customers. He also served as managing director for Storage Technology GmbH, where he restructured and refocused the business to achieve significant profit and sales increases. At Sun Microsystems, Fietz managed the German sales team, where he drove growth in core vertical markets.

Fietz stated, "I'm excited to work closely with the Vincotech team to further accelerate growth and profitability. In spite of the challenging economic outlook ahead, I believe the business is well positioned to capitalize on current market opportunities. It is a great opportunity for me to partner with the Gores Group, a premier private equity firm, which is so focused and committed to helping businesses achieve their full potential."

Joachim Fietz, Managing Director, Vincotech.

Fietz received a master's degree in mechanical engineering from the University of Hannover, graduating Summa Cum Laude.

www.vincotech.com

InPower Completes its Range of Intelligent Digital IGBT Gate Drivers up to 6.5kV

Following the demand for digital control of power electronics observed in the last few years, InPower Systems GmbH introduced intelligent digital gate drivers for high-power IGBT modules with blocking voltages up to 6.5V to the market.

InPower Systems GmbH, a young and innovative enterprise in the field of power electronics with office locations in Germany (Bavaria and Hamburg) and Czech Republic, develops, manufactures and markets digital IGBT gate drivers.

Since its foundation in April 2002 until the patent disclosure for its drivers (DE 10 2006 034 351 Al) in February 2008, the company has developed a wide driver product portfolio for IGBT modules with medium and high power with blocking voltages from 1200V to 6500V. InPower's digital drivers are deployed in the areas of industrial drive engineering, electric power supply, traffic engineering, power engineering for alternative energies and induction heating.

In close collaboration with its customers, the company develops competitive new products with an emphasis on the increased reliability of its drivers and price-performance ratio.

Switching losses are a major contributor to the overall losses in the most applications. Based on the variable gate resistors, InPower's digital IPS gate drivers reduce switch-on losses by up to 20%, improving the efficiency of the entire process.

InPower has developed a wide driver product portfolio for IGBT modules.

Excellent protection of the IGBT and the free wheeling diode is provided by the digital multi-level desaturation protection and di/dt protection, active feedback clamping and multiple soft shut down. All protection features are controlled by the software and guarantee an exceptional protection of the IGBT and diode.

These drivers may be used both in dual- and multilevel topologies. They are very flexible and therefore suitable in adaptation to the special implementations. Customers are not required to possess programming skills or additional equipment as the IPS drivers are supplied plug-and-play i.e. modified and optimized for the IGBT module used.

The high peak output current of up to 70A, high output power up to 15W, short signal transition times, adaptable timing constants and delay times, wide supply voltage range from +14V up to +30V, high switching frequency up to 120kHz and isolation testing voltage from 5,000V up to 10,000V are key features of the IPS gate drivers and make them easy to implement in various applications such as industrial drives, power-supplies, transportation, renewable energies and induction heating.

www.inpower-sys.com

Making Grids Smart for the Power System of the Future

By Martin Gross, Head of Power Systems North America, ABB Inc.

There is a convergence occurring today between the business realities of the utility industry, the energy demands of modern society, and the sustainability requirements of the environment in which we live. The combination of these is driving the development and implementation of a new power delivery system.

This is the “smart grid” network, and it utilizes the same basic infrastructure we know today, but applies advanced information and communication technologies to introduce greater functionality at every level of the system.

The result is a power grid that is more reliable, more resilient and more flexible than even the most modern systems currently in operation. These characteristics in turn will support the development of renewable energy sources while improving the efficiency of power delivery systems and reducing CO_2 emissions.

Many pressing factors today, from the economic to the environmental, are amplifying the need for the grid itself to evolve. We need our power delivery infrastructure to do more, much more than it does today. To meet the many challenges facing it, the grid needs an infusion of intelligence.

There is a great deal of variation both within and outside the power industry as to what exactly should be included under the idea of a smart grid.

ABB takes an expansive view of the smart grid, defining it more by its capabilities and operational characteristics than by specific technologies. We

Martin Gross, Head of Power Systems North America, ABB Inc.

see an increasingly automated system, based on industry-wide standards, created not through radical change but a gradual transformation of the existing system.

The concept of intelligence in power systems as we see it is centered on the idea of pushing sensory and analytic capabilities further down the system hierarchy. In a smart grid, more can be done locally at the substation or even device level, allowing operators and computing resources in the control center to be more effectively utilized. A smart grid also produces a stream of information about system conditions and operating characteristics that will be increasingly valuable to managing the commercial side of a given utility or grid operator.

Utilities are already implementing “smart” devices in various ways. Substation automation, for example, has been an industry trend for many years, enabling substations to perform more complex and autonomous functions while serving up a host of useful information from the field to the utility control center. Similarly, SCADA systems, reactive power compensation and feeder automation are all being used to reduce “line losses” for greater efficiency.

ABB’s Power Systems engineers working in our Grid Systems, Substation/Substation Automation, Power Generation and Network Management divisions throughout North America continue to make great strides in creating power systems designs that are transforming the United States’ century-old power transmission system into a rebuilt smart grid that will support the growing need for energy well into the 21st century.

The smart grid, of course, is more than any one technology, and the benefits of making it a reality extend far beyond the power system itself. The transition from the grid we know today to the grid of tomorrow will be as profound as all of the advances in power systems over the last hundred years, but it will take place in a fraction of that time.

This will require a new level of cooperation between industry players, advocacy groups, the public and the regulatory bodies that have such immediate influence over the direction this process will take. In the end, though, the smart grid will benefit all stakeholders.

www.abb.com

Digital Power to Grow Significantly

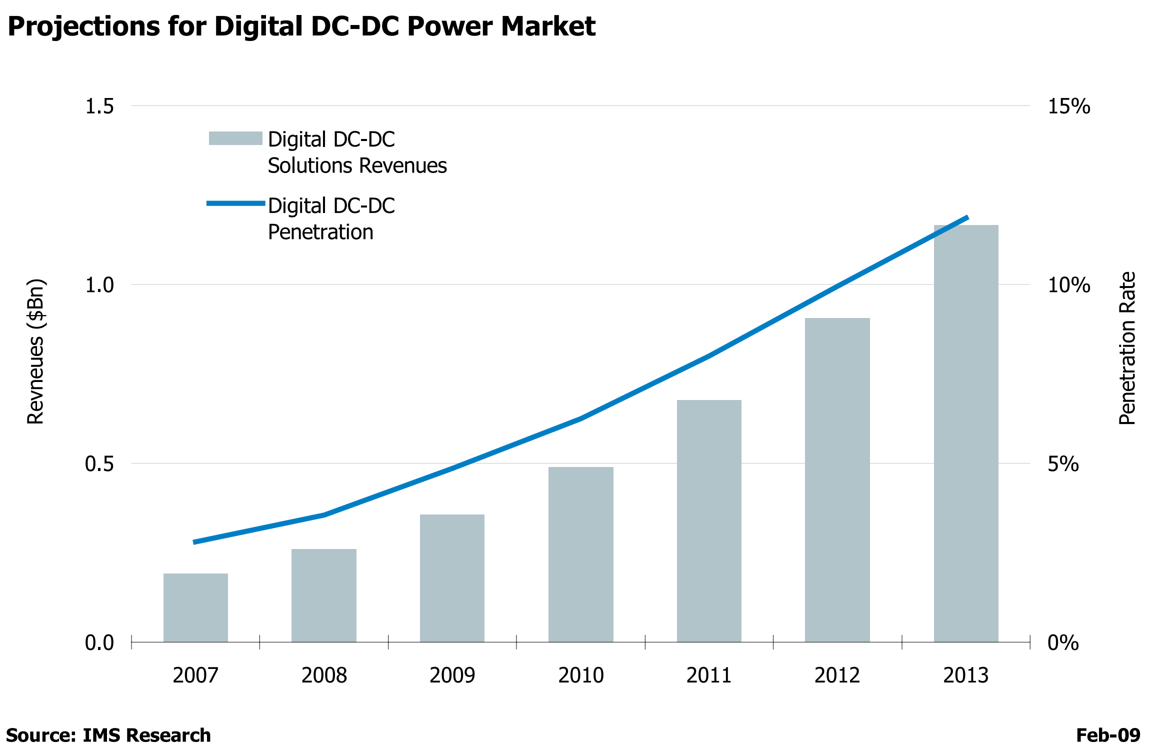
By Ash Sharma, Research Director, Power & Energy Research Group, IMS Research

The topic of digital power has divided the power industry over the past few years into two camps: those that think it will never take off, and those that believe it will revolutionize the industry. Increasingly, the consensus appears to be that it will gain significant adoption, but the questions remain – when will this be, and why hasn't it happened already? After all digital power as a concept has been around for many years.

Digital solutions have been proven to work in power designs for sub-systems such as rectifiers, inverters and UPS; yet adoption of digital power for DC-DC conversion remains relatively limited, despite a number of obvious benefits.

Whilst most users are not interested in whether a digital or analogue control loop is used, they may be convinced to switch to digital to reap the benefits of reduced component count, better control capability and improved efficiency.

Enhanced functionality now appears to be the main marketing angle used by suppliers active in the digital power field and is probably the most significant benefit of digital power, particularly in applications where there is a need for real time power system diagnostics and adaptive control under different loads or operation modes. Digital power can also reduce the overall cost of new designs, by allowing companies to use the same design platform across multiple topologies and customising designs through the use of software.



Whilst there are some clear benefits of employing digital products in power designs, penetration of these products to date remains low. IMS Research's latest reports on the Global Market for AC-DC & DC-DC Power Supplies and the Global Market for Power Management ICs found that in 2008, just 3.6% of DC-DC solutions revenues were from digital products (Figure 1). In order for digital power to really take off on a large scale, a number of issues need to be overcome.

Firstly, prices of digital power products will need to fall further in order to gain wide scale adoption. Whilst prices are often described as 'comparable' to analog solutions, this is typically only true for specific designs with a large number of voltage rails and only when comparing the overall design cost rather than just comparing component costs. It is inevitable that prices of digital products will fall further as more suppliers enter the market and volumes rise; however, the customer will need to be persuaded on the basis that overall system costs will be lower.

Demand for digital power will need to be generated in new, high volume applications. To date, most demand has come from high-current designs in applications such as routers, servers and storage and switching equipment. The acceptance of digital power over analog in one or more high-volume application would help raise acceptance of the technology, further reduce prices and drive mass adoption.

Finally, one of the most critical restraints on digital power adoption is the reluctance of designers to switch – the 'inertia to change'. Digital designs will require power supply designers, often traditional analog engineers, to learn new design techniques and take into account new layout considerations. Some designers may have difficulties with software design and will prefer to continue using "old fashioned" analog techniques. This obstacle is in part being addressed by a number of power IC vendors that are providing much greater design support for customers and in some cases taking care of the entire design process.

IMS Research projects that penetration of digital products in DC/DC solutions will continue to grow significantly, reaching nearly 12% by 2013, implying that revenues of digital DC-DC solutions will increase by some 35% per year on average over the next five years. Whilst one can debate whether this forecast is too aggressive or too conservative, what seems unarguable is that the future for digital power is very positive.

www.imsresearch.com

Frequency Response of Switching Power Supplies – Part 2

Extracting test Signals from noise

In this article, Dr. Ridley continues the topic of frequency response of switching power supplies. Last month's article focused on the broadband noise generation of power supplies. This article shows how we can extract single frequencies one-by-one from the noise with a frequency response analyzer. This allows us to perform control measurements on our switching power supplies.

By Dr. Ray Ridley, Ridley Engineering

Single Frequency Measurements for Switching Power Supplies

The previous article in the Design Tips series of this magazine[1] discussed the wide range of frequencies generated by a switching power supply. High noise is unavoidable when working with switchers, and the converter must also be tightly controlled in the presence of this noise.

This presents a challenge in two areas: firstly, the control chip must run reliably with the noise and predictably set the duty cycle of the switch from one cycle to the next. Secondly, measurements must be taken on the power supply once a control loop is closed to ensure that it is always stable.

Analog controllers do an exellect job of managing the first problem through the simple sawtooth ramp and reference technique of a standard PWM controller. Once the controller is working properly, we use traditional Bode plot measurements to assess performance and stability.

Power supplies are one of the few areas of analog electronics that still make conventional measurements rather than depending on prediction and modeling alone. The loop gain and stability margin can vary tremendously for a converter operating over its full range. Figure 1 shows the range of variation that can exist for a simple buck converter when

variations of line, load, temperature, and EMI filter are considered.

These curves show extreme changes in the gain and phase of the converter. The curves, however, assume linearized operation, with small-signal circuit models used to generate the plots. In the real world, the switching power supply may have regions of operation that are not well modeled, and even more variation is possible. Clearly, in the face of such extreme behavior, measurement of the power supply is an essential step in making sure the design of the control loop is rugged.

Figure 2 shows a typical noisy power supply waveform with an injected signal, used to make control measurements. This points out another unique requirement of switching power supplies – specialized equipment is needed to be able to extract the injected waveform in the presence of the switching noise. This is done with a frequency response analyzer.

Frequency Response Analyzer

A frequency response analyzer is a piece of test equipment designed to inject a sinewave into a circuit, and measure the response of the circuit at that single frequency at two different test points in order to generate a gain and phase response. The injected sinewave is swept from frequencies as low as 0.1 Hz, up to the switching frequency of the converter.

The role of the frequency response analyzer is to extract extremely small test signals (sometimes much less than 1 mV) from noisy waveforms, and compare their gain and phase. The technology needed to do this is not new, having been used for decades in our field.

Figure 3 shows a block diagram of an analyzer designed for switching power supplies. An oscillator puts out a test signal which is injected into the circuit to be measured. (Techniques for injection will be presented in later articles in this magazine.) Two input channels

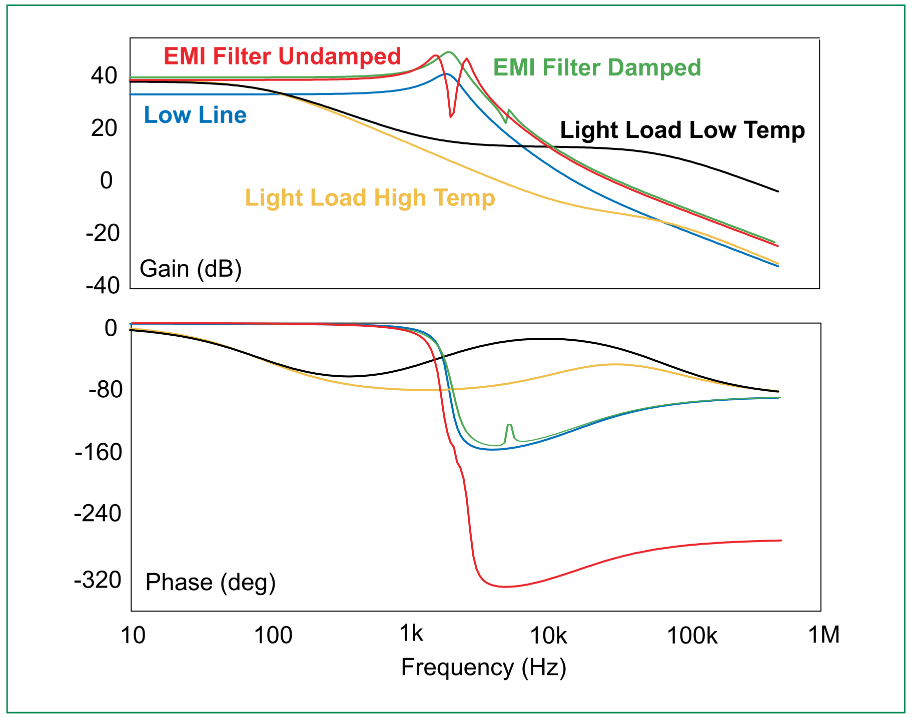


Figure 1: Variability of Bode plots for a "simple" buck converter with variations of line, load, temperature, and EMI input filter.

on the analyzer are used, connected to different test points in the circuit. Each input channel processes a test signal, first with analog signal processing to eliminate noise, then with digital signal processing. The output of the digital processor interfaces with a computer. Early versions of frequency response analyzers used purely analog techniques to create Bode plots.

The analog section of the input channels work in a similar way to radio receivers, using wide band amplifiers, and heterodyning techniques with mixers and filters to isolate the test signal, and reduce the frequency of the carrier down to an easily measurable quantity. Communication theory tells us that the gain and phase of the test signals can be preserved when producing an IF bus in this manner. This greatly simplifies the task of the A/D conversion stage of the system.

After A/D conversion, the data is passed to a microprocessor, and then to a computer to perform further digital filtering and noise reduction. The results can then be presented as a traditional Bode plot to the user.

Using these techniques, extreme values of signal to noise and dynamic range can be obtained, in excess of 110dB. This is essential for reliable measurement of switching power supplies. Further details of the theory are given in [2].

This process cannot be short-circuited with modern "frequency-response analyzer on a chip" products that have recently been introduced. The integrated

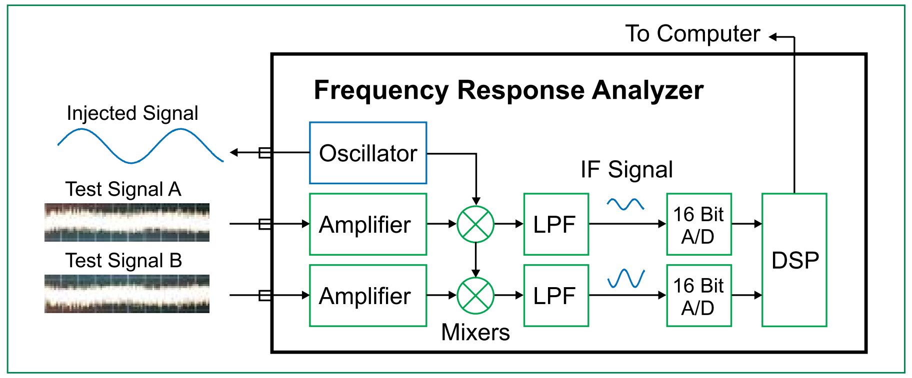


Figure 3: Frequency response analyzer test equipment block diagram.

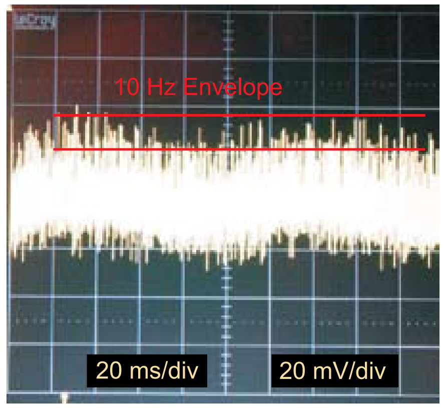


Figure 2: Typical power supply waveform with signal and noise.

chips for this have neither the dynamic range, or noise-rejection capability needed for switching power supply measurement, although they may work reasonably well for linear, non-switching circuits where noise levels and gains are low.

Using the frequency response analyzer, individual frequencies are extracted from the noise, and two signals can be accurately compared in terms of gain and phase. This allows us to study the control characteristics of a system and design the feedback loop properly.

Summary

The frequency response analyzer is a highly specialized instrument that we use, and it is essential for stabilizing power supplies quickly and efficiently. In the next two articles in this series, the essential role of loop gain measurements will be discussed and compared to the technique of trying to design control loops with step-load response measurements.

References

1. "Frequency Response of Switching Power Supplies", Power Systems Design Magazine, Design Tips Archive, January 2009. http://www.powersystemsdesign.com

2. http://www.apinstruments.com/files/102Bman.pdf. Page 58 shows detailed block diagram of frequency response analyzer functions for a high-performance instrument suitable for measuring switching power supplies.

3. http://www.switchingpowermagazine.com/downloads/Measuring Frequency Response.pdf Techniques for using a frequency response analyzer.

On the Road

Reported by Cliff Keys, Editor-in-Chief, PSDE

Analog Devices

I participated in ADI's launch of the company's new, low power current-to-signal converter for the medical market. This is a high growth area that is becoming an important part of our industry. With the constraints on funding, medical authorities need to get the best return on the high investment of modern equipment in terms of patient service and efficiency of deployment.

ADI's Current-to-Digital Converter Technology Lowers CT System Cost

Enables enhanced imaging with industry's highest levels of channel integration and speed

The use of CT (computed tomography) scanning is increasing as technology improvements provide clearer, more detailed pictures of the human body for physician analysis and diagnosis. At the same time, healthcare facilities are faced with a growing need for better quality, faster, and more affordable diagnostic imaging equipment. Analog Devices, Inc., the leading provider of data conversion technology and longtime collaborator to the medical imaging industry, is addressing these needs with a new current-to-digital converter chip that enables high slice count CT systems to capture real-time moving images – such as a beating heart – with a high degree of accuracy and detail.

The ADAS1128 is a 24-bit current-to-digital converter that changes photodiode array signals into digital signals. The product offers 128 data conversion channels, provides an unparalleled increase in speed from 6kSPS (kilosamples per second) to 20kSPS, and supports four times more channels (128 versus 32) than any other integrated converter solution available on the market today. This level of performance and integration means a 50 percent reduction of a CT detection system's electronics cost versus older designs.

Higher slice count CT systems require an increase in the number of data acquisition channels necessary to process images. The level of integration of ADI's ADAS1128 chip enables lower cost CT systems by reducing the cost per channel of the data acquisition circuits.

CT imaging combines special X-ray equipment with sophisticated computers to produce internal 2D and 3D images of the human body. CT scans of internal organs, bone, soft tissue, and blood vessels provide more detailed images than X-ray exams, enabling physicians to more easily diagnose problems that include cancer, cardiovascular disease, and musculoskeletal disorders. Today, it is estimated that more than 62 million medical CT scans are done in the United States annually, compared to three million in 1980.

By quadrupling the number of data conversion channels, ADI's new current-to-digital converter is setting a new performance benchmark for CT detection system designs."

Lower Power Current-to-Digital Converter Features 24-Bit Resolution and 128 Channels,

The ADAS1128 replaces previous converter-based technology having low levels of channel integration. The product integrates a 24-bit resolution ADC (analog-to-digital converter) with 128 simultaneously sampled data converter channels, selectable sample rates up to 20kSPS, and on-chip temperature sensor and reference buffer into a 1cm^2 single-chip solution. Along with supporting four times more channels, the product delivers over three times the throughput of any other solution available on the market.

The ADAS1128 consumes less than half the power of other solutions (4.5mW/channel versus10 mW/channel at full speed). It also offers superior overall performance specs, such as no charge loss, more choices of full scale ranges, and ultra-low noise (down to 0.4 fC for low-dose X-ray systems).

Other recent medical announcements from ADI include the award-wining AD927x family of eight-channel (octal) receivers for ultrasound systems. These products, along with other ADI offerings, represent today's broadest IC product portfolio geared specifically toward the healthcare imaging market.

Availability

The ADAS1128 current-to-digital converter is available now in volume production. The ADAS1128 is housed in a compact 10-mm X 10-mm mini BGA (ball grid array) package. For more information, visit http://www.analog.com/pr/ADAS1128. Along with CT systems, the ADAS1128 also enables the design of X-ray-based security imaging systems used in shipping yards, harbors, and airports.

www.analog.com

LEM

I participated in LEM's press conference in Munich, Germany. LEM, market leader in providing highest quality solutions for the measurement of electrical parameters, is already widely known and respected for its core products of current and voltage transducers. These are to be found in a broad range of applications in industrial, traction, energy, automation and automotive markets. The company is now actively exploiting these strengths, developing opportunities in new markets with new applications.

LEM Reduces Current Transducer Size by 30%

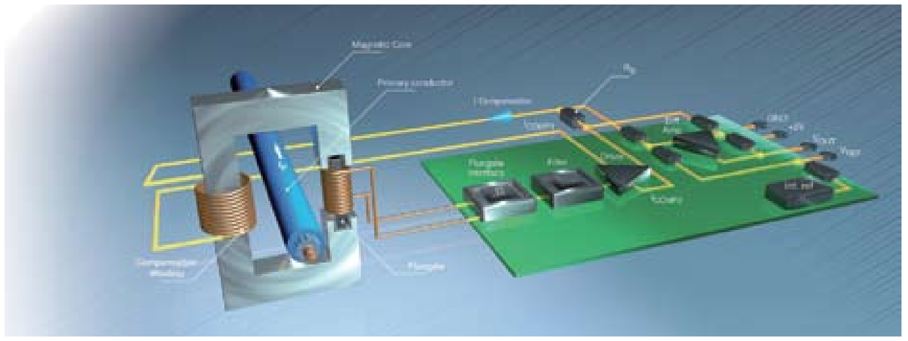
Utilizes Fluxgate technology

LEM has introduced several ranges of PCB-mounted current transducers housed in a package 30 percent smaller than the company's LTS devices.
The CAS, CASR and CKSR family of transducers are intended for AC and DC isolated current measurement from 6 to 50A_{RMS} nominal, up to 3 times the nominal values for the peak measurement and up to 300kHz (+/-3dB). All the models (6 A_{RMS}, 15 A_{RMS}, 25 A_{RMS} and 50 A_{RMS}) are housed in the same compact package and can be set up on PCB according to the needs for different ranges from 1.5 A_{RMS} to 50A_{RMS} (according to the models).

The new transducers have been specially designed to respond to the technology advances in drives and

inverters, which require better performance in areas such as common-mode influence, thermal drifts (offset and gain; Max thermal offset drift for the models with reference access: 7 to 30 ppm/K according to the models), response time (less than 0.3 microseconds), levels of insulation and size.

To obtain this performance the Closed Loop Fluxgate technology has been used. This enables LEM to combine high accuracy and attractive price without compromising any of the advantages of the LTS family, such as size, dynamic performance and wide measuring range.



Closed Loop Fluxgate technology.

Although the new transducers are 30 percent smaller than the existing LTS family, their insulation performance allows use in industrial applications without a special layout of the PCB. The CTI (Comparative Tracking Index) of the plastic case is 600. The CKSR model has one more primary pin than the three pins of the CAS and CASR models and a different primary footprint enabling higher creepage and clearance distances of 8.2mm to be achieved. This is particularly useful when higher insulation is required in applications with high working voltages such as 600 V_{RMS} according to the EN 50178 standard.

Moreover, this additional primary pin allows a configuration of the CKSR 6-NP model for a nominal current range of 1.5A_{RMS}.

All transducer models have been designed for direct mounting onto a printed circuit board for primary and secondary connections. They all operate from a single 5V supply. The CASR and CKSR models provide their internal reference voltage to a VREF pin. An external voltage reference between 0 and 4V can also be applied to this pin.

The CAS, CASR and CKSR family of transducers are suitable for industrial applications such as variable speed drives, UPS, SMPS, air conditioning, home appliances, solar inverters and also precision systems such as servo drives for wafer production and high-accuracy robots.

www.lem.com

Synopsys

I met with Juergen Jaeger, Director Product Marketing for the ASIC Verification Synplicity Business Group at Synopsys. With over 20 years of industry experience, he is currently responsible for the Confirma ASIC/ASSP verification platform including the HAPS prototyping system. He explained that prototyping was an essential part of product development these days due to complexity and the extreme cost if problems are not realized at an early stage. The performance of a new product in terms of power efficiency, functionality and time to market are more important to the profitability than ever before.

Synopsys Defines Next Era of Rapid Prototyping

Synopsys has introduced its expanded Confirma™ rapid prototyping platform. The addition of the recently acquired CHIPit® products, tools and technologies simplifies the implementation and deployment of rapid prototypes, allowing users to begin hardware-assisted system validation and embedded software development sooner. Complementing the HAPS high-performance prototyping hardware, the expanded Confirma platform now also offers a software-configurable architecture and transaction-based co-verification capability. With the combination of a proven prototyping methodology, IP, services, hardware and software, the Confirma platform is a comprehensive solution for a wide variety of prototyping applications. Synopsys now delivers the most comprehensive Software-to-Silicon Verification Solution - including rapid prototyping, virtual platforms, functional verification and analog/mixed signal circuit simulation - addressing the key challenges in the system-on-chip (SoC) verification process.

"Growing SoC complexities, increasing amounts of embedded software, and the high cost of emulation have forced new approaches to system design and validation," said Juergen Jaeger, Director Product Marketing for the ASIC Verification Synplicity Business Group at Synopsys. "Build-your-own prototyping boards, although widely used for many years,

Juergen Jaeger, Director Product Marketing for the ASIC Verification Synplicity Business Group at Synopsys.

have become increasingly difficult for customers to design, manufacture and implement. Our Confirma platform, the technology-leading rapid prototyping system, represents the next era of comprehensive hardware-assisted verification that enables development teams to simultaneously validate and more economically deliver their complex chips and software."

The Economics of Hardware-assisted Verification

The growing complexity of chip design and software content is increasing the cost of embedded software development and system validation. Traditional approaches such as "big-box" emulation systems are too expensive and slow for wide deployment to embedded software developers and verification teams. Custom-built FPGA-based prototypes can address these issues but are difficult, time-consuming and expensive to implement and debug. The Confirma rapid prototyping platform helps solve the problems associated with these traditional approaches and brings all the critical components together into a comprehensive and affordable solution that enables more design teams to take advantage of the benefits of hardware-assisted verification.

Recently acquired CHIPit® products, tools and technologies simplify the implementation and deployment of rapid prototypes, allowing users to begin hardware-assisted system validation and embedded software development sooner.

The Expanded Confirma Platform

The expanded Confirma platform is a complete suite of products for rapid prototyping including FPGA-based prototyping systems and boards, interface and memory boards, and implementation and debug software. The Confirma platform provides all of the elements needed to quickly implement a rapid prototype:

Hardware platforms:

- CHIPit family of rapid prototyping systems featuring a programmable interconnect architecture for greater automation and providing emulation-like capabilities optimized for transaction-based verification

- HAPS™ family of rapid prototyping boards providing high performance for system validation and embedded software development

- An extensive collection of high-speed interface and expansion boards enabling prototypes to be easily customized to cover a wide range of applications

Software tools:

- CHIPit Manager Pro prototype configuration and project management software

- SCE-MI (Standard Co-Emulation Modeling Interface) compliant transaction-based co-verification interface

- Certify® multi-FPGA implementation and partitioning software

- Identify® Pro debug software with TotalRecall™ visibility enhancement technology

- Synplify® Premier, the technology-leading FPGA physical synthesis tool

Complementing the product offerings are a wide range of service, training and support options, ranging from one-week training classes to full turn-key services as well as Synopsys' worldwide support for geographically distributed hardware and software design teams.

Part of a Comprehensive Software-to-Silicon Verification Solution

The Confirma rapid prototyping platform is part of Synopsys' Software-to-Silicon Verification Solution that offers the industry's most comprehensive suite of proven embedded software development, system validation, functional verification and circuit simulation software, hardware, intellectual property (IP), methodologies and services for complex system-on-chip (SoC) development. New solution-level integration includes co-simulation and debugging between Synopsys' Confirma platform and VCS® high-performance simulator, and support for synthesizable DesignWare® IP in Confirma rapid prototypes. The Confirma products also integrate with Innovator-based virtual platforms to enable a hybrid virtual/physical prototyping environment for embedded software development and verification.

www.synopsys.com

Solyndra Reshapes Solar

California PV manufacturer delivers breakthrough systems for commercial rooftops and strengthens European presence

I talked with Clemens G. Jargon, Solyndra's Vice President EMEA and Managing Director of Solyndra GmbH in Munich, Germany; he is responsible for overseeing the company's rapidly growing European operations. Solyndra designs and manufactures photovoltaic systems, comprised of panels and mounting hardware, for the commercial rooftop market employing high volume manufacturing to meet the needs of the global solar market.

Reported by Cliff Keys, Editor-in-Chief, PSDE

A splendidly elegant solution using proprietary cylindrical modules (as opposed to the conventional flat modules) and thin-film technology, Solyndra's PV system is designed to generate significantly more solar electricity on an annual basis from typical low-slope commercial rooftops with lower installation costs than conventional PV flat panel technologies.

Commercial rooftops represent a vast, under-utilized resource and huge opportunity for generating solar electricity. Since its founding in 2005, the company has been developing technology and ramping manufacturing capacity to produce its proprietary CIGS-based thin film PV system. Solyndra is currently shipping its systems, comprised of panels and mounting hardware, to fulfill more than $1.5 billion of multi-year contracts with customers in the United States and now, Europe. Headquartered in Fremont, California, Solyndra operates a state-of-the-art 300,000 square foot fully-automated manufacturing complex.

Designed specifically for commercial rooftop installation, Solyndra's thin film PV system features proprietary cylindrical modules which collect more available sunlight and generate significantly more solar electricity from low-slope commercial rooftops than conventional flat panel PV technologies. Further,

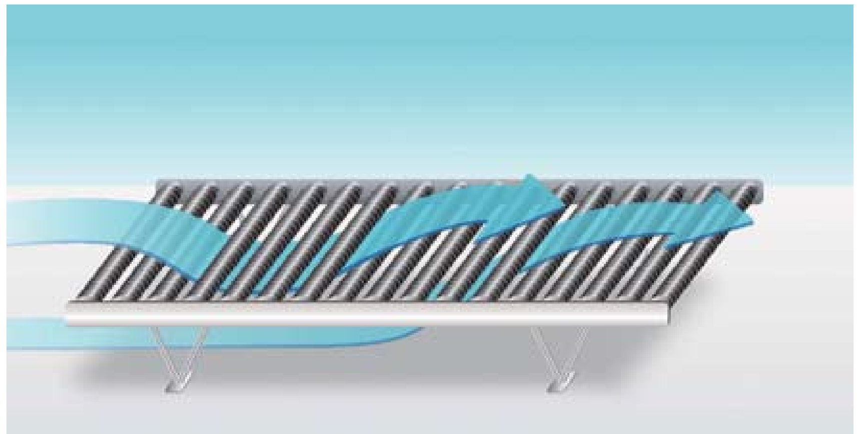


Figure 1: Solyndra innovative cylindrical elements have an extremely low wind resistance requiring only lightweight fixings.

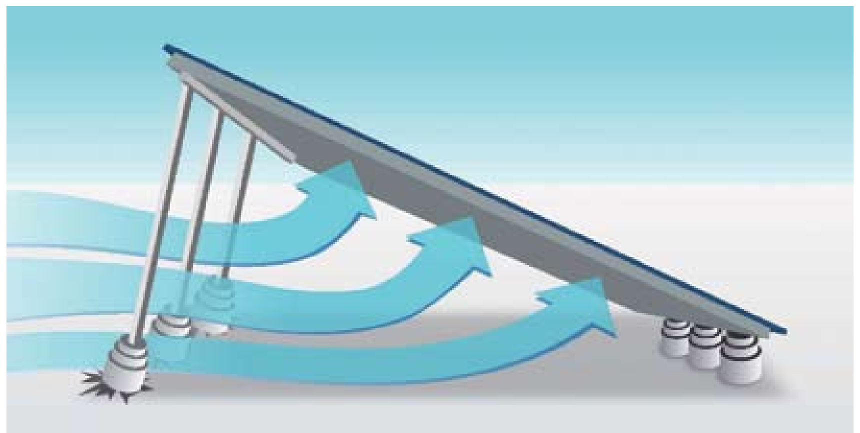


Figure 2: Conventional panels require heavily secured mounts to survive the force of wind pressure.

Simple installation, low maintenance and high efficiency provide a cost-compelling PV solution.

Solyndra's lightweight PV system is uniquely fast and economical to install due to simple horizontal mounting hardware and unique air-flow properties of the solar panels.

These innovative cylindrical elements that make up the array have an extremely low wind resistance, are easily installed by non-tech maintenance staff and do not suffer the efficiency-crippling drawbacks of more conventional panels of soiling due to weather, leaves, bird droppings or other debris – it all just washes away naturally.

Solyndra recently announced the opening of the company's European headquarters in response to the high demand in Europe for their unique photovoltaic (PV) systems which provide breakthrough solar electricity performance for commercial rooftops.

The commercial rooftops of Europe provide an immense opportunity for the generation of solar electricity and are of growing importance with the help of favorable incentive support in many countries. This move strengthens the company's ability to serve its customers in the region and allows it to play a greater role in the evolution of the European energy market towards a more sustainable future.

Solyndra's panels have already been fully certified for European solar installations and have independently-validated performance from multiple sources. The panels have received International Electro Technical Commission (IEC) and product certifications as well as GSE qualification for the Italian feed-in tariff system. Independent validation of the Solyndra PV system's energy yield performance has been done by leading institute Fraunhofer ISE of Freiburg, Germany and compared to field data from multiple international installations. Solar project developers and investors can now rely on Fraunhofer ISE for accurate, independently-validated system energy yield performance forecasts for Solyndra systems.

Solyndra has more than $1.5 Billion in orders and is entering its second year of international commercial shipments to customers in Europe and the United States. The company is already active in Europe with international solar power project integrators such as Phoenix Solar and Gecko Logic of Germany and leading international roofing systems manufacturer Carlisle Energy Services.

An interesting video on the manufacturing and installation can be viewed here:
http://www.solyndra.com/Products/Videos

www.solyndra.com

Dialog Raises Level of Configurability and Integration

New class of power management IC optimizing efficiency of portable consumer devices

I talked with Mark Jacob, Dialog's Director of Marketing for audio and power management who told me about the company's success in designing platform Power Management ICs for the high volume consumer market. These innovative products provide their customers with the same flexibility as standard products, but with the huge benefits of higher integration and performance found normally only in ASSPs. In today's financial and ecological environment especially, this gives the designer an extremely compelling route.

Reported by Cliff Keys, Editor-in-Chief, PSDE

Dialog Semiconductor has made its mark in the industry by creating the world's most energy-efficient, highly integrated, mixed-signal integrated circuits optimized for personal mobile and automotive applications. The company provides flexible and dynamic support, world-class innovation, and the assurance of dealing with an established business partner. Customers with a significant contribution to revenue include Sony-Ericsson, Apple, Bosch and Tridonic.

Headquartered near Stuttgart, Germany with operations in the USA, UK, Austria, China, Germany, Japan, Korea and Taiwan, the company has 250 employees worldwide.

Dialog introduced the DA9052, an advanced system power management integrated circuit (PMIC) that offers designers greater flexibility in reducing power consumption, size and cost in mobile phones and other portable multimedia devices. Conceived as a platform-PMIC, capable of supporting all major families of application and mobile graphics processors, DA9052 offers an unprecedented level of user-configurability.

Dialog's DA9052, advanced system PMIC.

Up to 14 power supplies, 16 GPIOs and other system function behaviour may be adapted in different operating modes as a means of eliminating power consumption overhead in the host processor. This high level of system wakeup/mode control within the PMIC reduces design cycle time and complexity by enabling software and application development to start at an earlier phase using a pre-validated PMIC platform.

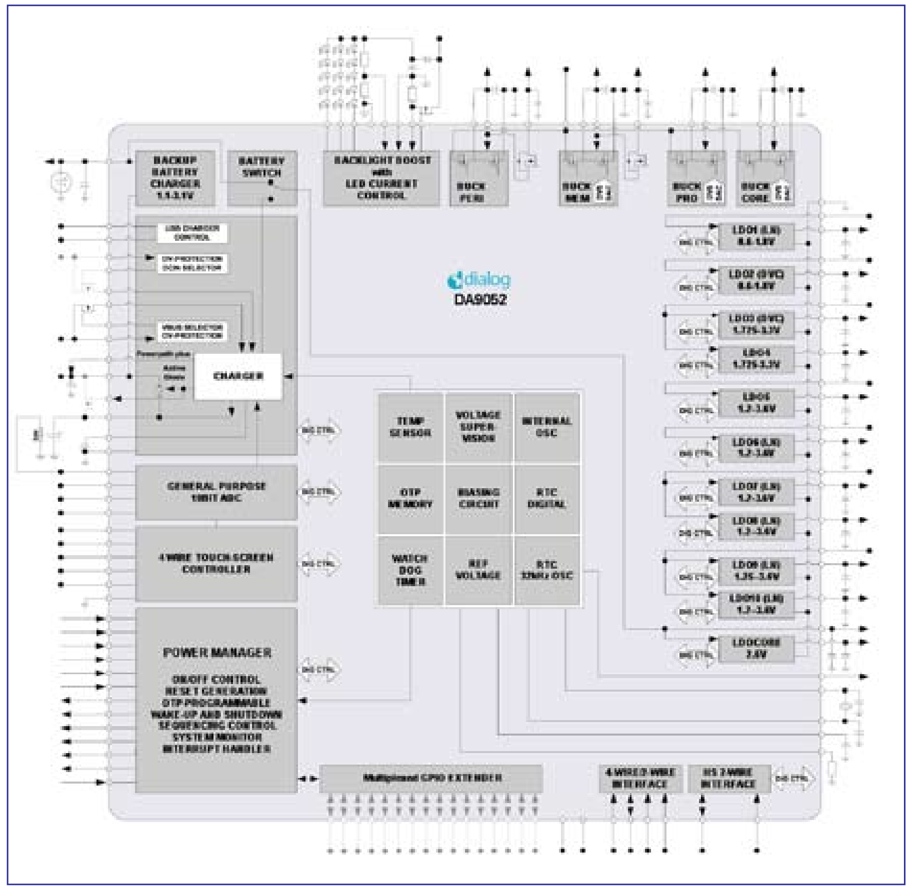
The DA9052 is easily set up through a simple graphical user interface in Dialog's Power Commander software utility. This configures power sequencing and multiple sleep modes. The device integrates 4 DC/DC buck converters and 10 programmable LDOs on-chip, and the LDOs can be connected to the DC/DC converters to improve system efficiency. Each output can be connected in series or parallel, adding further flexibility. To further optimise the processor energy-per-task, dynamic voltage scaling can be used on up to 5 outputs and Dialog's SmartMirror[1] dynamic biasing is implemented on all linear regulators.

Power dissipation within DA9052 itself is autonomously regulated on-chip. A dual-input switching DC/USB battery charger allows up to 1.2A to be drawn from a lithium battery with minimal thermal impact to the DA9052 device itself. This allows the increased output current to be sustained for maximum processor performance.

USB power inputs are over-voltage protected and the embedded power path controller manages energy flow between an AC adapter, USB cable and battery, whilst maintaining USB power specification compliance via the D+/D- data lines. This power path functionality is supported without any processor interaction, enabling power scenarios such as instant power-up with a fully discharged battery.

Mark told me, "Conventional discrete and fixed function PMICs lack the necessary control and flexibility demanded by end customers when embedded within a processor platform reference design, a new class of highly configurable platform PMIC is emerging which introduces a layer of user-software programmability. This enables our customers to tune the hardware at design-time to complement their own customisation activity without incurring the risk or time to market penalty".

www.dialog-semiconductor.com



DA9052 block diagram.

Front-End Power Supplies

Resonant power supply controllers drive maximum power efficiency

Typical application areas for digital-power Point-of-Load include telecom infrastructure, cellular base stations, high-end computers, and data storage equipments. These fields of application not only increasingly demand higher power efficiency, but also necessitate maximum system reliability.

By Alfred Grakist, Principal IC designer, NXP Semiconductors

In order to facilitate these requirements throughout the total power system and to 'upstream' the distributed power chain in the front-end power supply, the same requirements apply.

For bulk power front-end supplies, NXP's new generation of LLC resonant power supply controllers bring together the conditions to achieve maximum power efficiency, combined with unsurpassed power supply robustness. Key enablers in achieving this are the novel cycle-by-cycle adaptive dead time control and the also cycle-by-cycle acting capacitive mode protection. This article presents NXP's latest resonant controller devices: TEA1713 and TEA1613. Both products contain an identical new-generation half-bridge resonant controller. The TEA1713 combo controller also contains a Power Factor Correction (PFC) controller.

Half-bridge LLC resonant converter

The basic topology of the half-bridge resonant converter is shown in Fig 1.

The LLC resonant converter is supplied from a DC high-voltage DC bus, which often is generated by a preceding active Power Factor Correction stage. The resonant tank consists of a capacitor Cr and a transformer with Lr (leakage inductance) and Lp (magnetizing inductance). The Half-Bridge Controller (HBC) alternately drives the two power MOSFETs. The operating frequency determines the amplitude of the current. At the secondary side the high-frequency AC voltage is rectified and filtered to obtain the DC output voltage (V_{out}).

Adaptive dead-time control

The high efficiency of a resonant converter is possible because the MOSFETs are soft switching, also known as Zero Voltage Switching (ZVS). A sufficiently long dead time between the switching of both MOSFETs allows the half-bridge voltage (node HB) to rise or fall completely, so the MOSFETs can be switched-on with zero volts across them. This reduces the switching losses to an absolute minimum.

After the HB slope has completed, the primary current will flow through the more high-ohmic body diode of the MOSFET, until the MOSFET is switched-on. Therefore, a too long dead time will cause higher conduction losses.

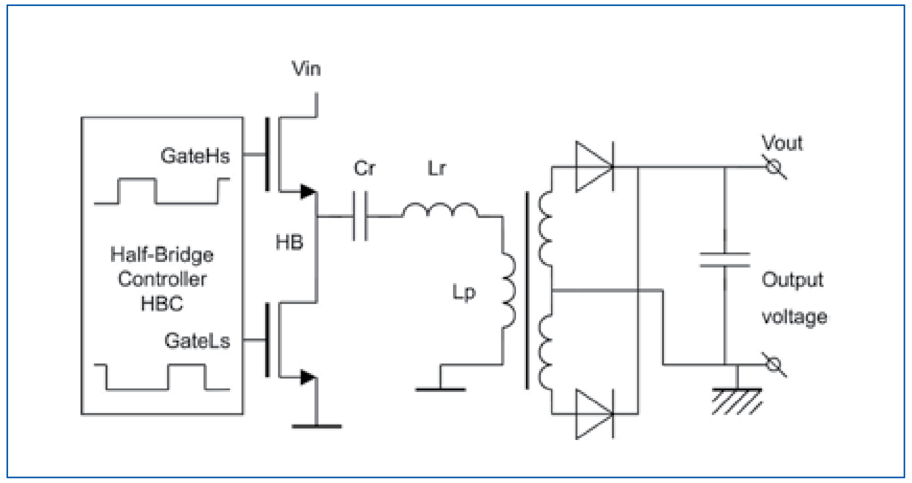


Figure 1: Resonant Topology.

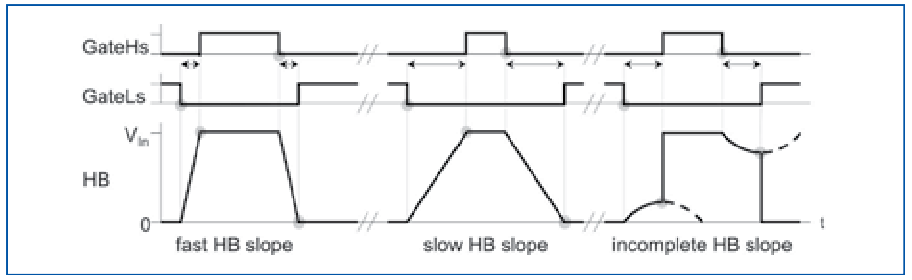


Figure 2: Optimal start-up of the resonant converter.

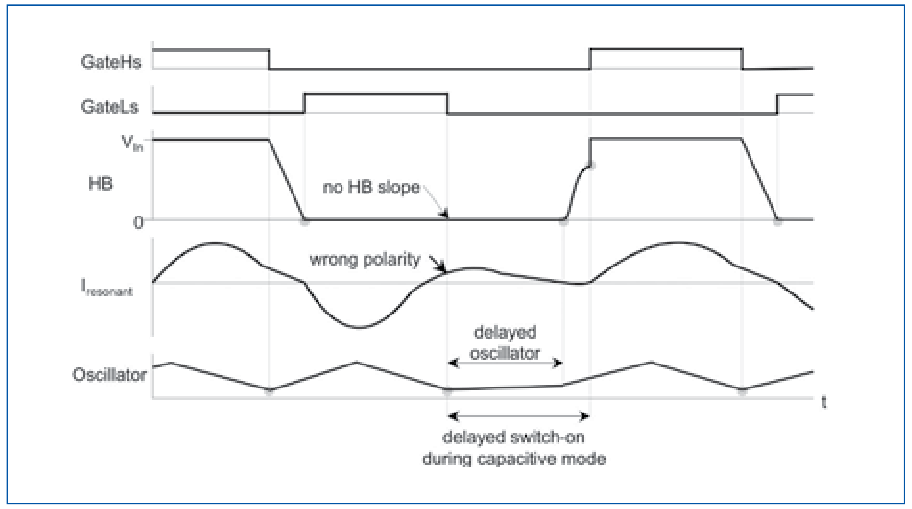


Figure 3: Capacitive Mode Protection.

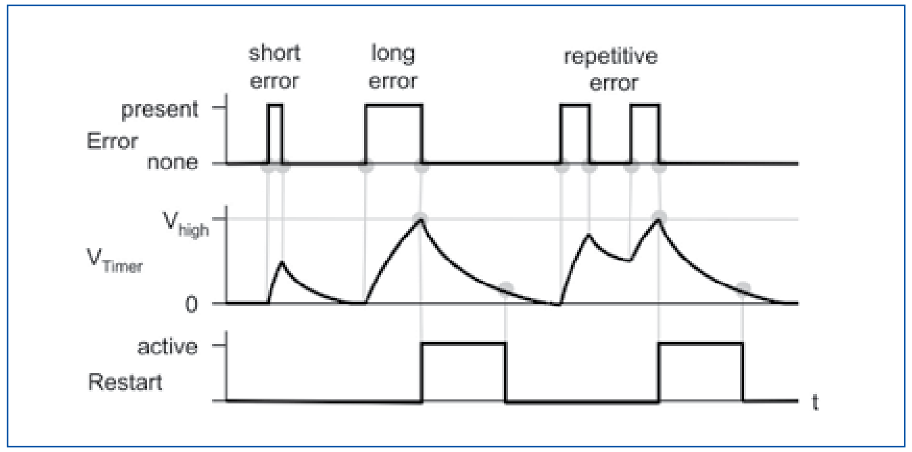


Figure 4: Burst mode.

The speed of the HB slope, and thereby the optimum dead time, varies with frequency, output load, input and output voltage. Controllers with a fixed dead time, either internally fixed or configurable, challenge the power supply designer to find an acceptable compromise for the choice of the fixed dead time value.

NXP's new generation resonant controllers are equipped with a true cycle-by-cycle adaptive dead time control function. Advanced circuitry in the HBC controller senses the end of the HB slope and will always switch-on the MOSFET at the optimum moment in time without any compromise. See Fig.2. Soft switching is ensured while minimizing body diode conduction time. The adaptive dead time function simplifies the design of the resonant power supply and maximizes efficiency.

Soft-start compromise

The resonant converter starts at a high frequency to ensure that the initial currents are within safe values. Then the frequency sweeps down towards the operating frequency. This is generally referred to as soft-start. The speed of the soft-start sweep is a compromise:

On one hand, the soft-start sweep should be fast so the output voltage is quickly available and the connected load can operate.

On the other hand, the soft-start sweep should be slow to prevent a too high inrush current.

The amplitude of the inrush current is hard to predict because it depends on input voltage, sweep speed and the load-dependent rise of the output voltage. NXP TEA1713 and TEA1613 resonant controllers have several functions to guarantee a fast, but safe and well-controlled start-up under a wide range of start-up conditions.

Two-speed soft-start mechanism

During a soft-start sequence, the first part of the frequency sweep, further away from the resonant point, the change in current as function of the change in frequency is much smaller than is the case closer to the resonant frequency. In anticipation to this effect, a two-speed soft-start function has been implemented. This soft-start sequence has a four times faster frequency sweep rate for the upper half of the frequency range, compared to the frequency sweep speed in the lower half of the frequency range. In this way, both a very speedy and very well controlled soft-start function is achieved.

Reliability and safety

Enhancing the reliability and robustness of switch mode power supplies is key in the reduction of field returns and involved cost of none quality. Anticipating on that, NXP has equipped the TEA1613 and TEA1713 with an extensive set of protections, yielding an ultimately robust power supply application.

Capacitive mode protection

One of the most important elements in the set of protections is NXP's patent-pending, cycle-by-cycle capacitive mode protection features. These features prevent the risk of a slightest damage to the power MOSFETS due to capacitive mode switching events. The MOSFETS do not need to be robust for reverse recovery events associated with capacitive mode switching. It allows a cost optimized power MOSFET selection without compromising on performance and/or robustness of the power supply design.

A resonant converter normally operates in inductive mode with the switching frequency above the resonance frequency where high efficiency is reached by Zero-Voltage Switching (ZVS) of the power MOSFETs. In special conditions like output short circuit, high load pulse or mains dip, the resonance frequency of the resonant tank can temporarily become higher than the operating frequency. This results in the resonant tank exhibiting capacitive impedance. In capacitive mode operation, the current continues to flow through the body diode after the MOSFET is switched-off and no slope at the half bridge node (HB) follows. Switching-on the other MOSFET at that moment is very dangerous because the high peak current caused by reverse recovery in the MOSFET with the conducting body diode can immediately destroy it. The TEA1713 and TEA1613 take three actions to protect against the hazardous capacitive mode operation.

The first action is taken by the adaptive dead time control of the TEA1713 and TEA1613. It delays the switch-on of the other MOSFET until the current has changed to the correct polarity. The MOSFET is switched-on after the half bridge slope has passed, thereby ensuring that the current has changed to the correct and safe polarity. See Fig.3. This action guarantees the prevention of dangerous reverse recovery switching of a MOSFET.

In capacitive mode it can take half the resonance period time before the resonant current has changed back to the correct polarity and the slope at the half bridge node occurs. To allow this relative long waiting time, the oscillator is slowed-down until the start of the half bridge slope is detected.

The third action is the increase of the oscillator frequency as long as capacitive mode operation is detected. This action will bring the converter back into the safe inductive mode.

Two-level over-current protection with boost voltage compensation

To prevent overheating of components or transformer saturation by (temporary) higher operation power, a two level over-current protection is provided. At the first lower current level, the frequency is regulated to limit the current. This Over-Current Regulation (OCR) also limits the current during start-up. A second higher current level protection will be triggered if the current increase is too fast to be regulated by the OCR, for example during an output short circuit. At this second level a more drastic corrective action is taken by an immediate step to the maximum frequency. This is the Over-Current Protection (OCP).

The input voltage of the resonant converter is often generated by a PFC and very constant. However, during start-up, during mains-dips or in a system without an active PFC the boost voltage can be lower. Then the primary current will be higher for the same output power of the resonant converter. The TEA1713 and TEA1613 provide a boost voltage compensation that adjusts the protection level for different input voltage levels. It allows a more accurate output over-current protection, which better protects the power supply load and thereby increases the safety.

Other protections

In the TEA1713 and TEA1613 an extended amount of protections are provided to design a safe and reliable power supply. The Over-Voltage Protection (OVP output) monitors the output voltage and protects the load. The Open-Loop Protection (OLP) acts when there is an error in the critical feedback loop. Some protections increase the frequency to solve an error. When the error is not solved by the increased frequency, the High-Frequency Protection (HFP) will detect this and restart the controller.

For a number of protections, exceeding the protection level is allowed for a limited time. For these temporary allowed errors a Protection and Restart Timer is integrated. When the error still exists after the preset protection time, the controller is restarted. The timer also defines the restart time. The power supply designer defines the protection and restart time independently by an external capacitor and resistor. Fig. 4 shows the operation of the Protection and Restart Timer.

To achieve increased efficiency at low power levels, the TEA1713 and TEA1713 facilitate burst mode operation. During burst mode switching of both PFC and HBC is halted periodically during which the power FETs of PFC are switched-off and the switching frequency is memorized. After the burst off time the HBC resumes switching at the memorized frequency, while the PFC restarts with a soft-start The optimal burst detection level is very dependent on the input voltage of the HBC that comes from the PFC (boost). In case of a passive PFC, or during mains dips, this voltage can change significantly, causing a major shift of the feedback voltage. In order to keep the burst mode operating properly, a compensation of the burst reference level is preferred. The TEA1613 has integrated boost compensation. A boost voltage dependent current flows out of the burst detection input of the controller. The power supply designer can freely set the optimal amount of compensation by the value of an external series resistor.

Flexible controller supply

The TEA1713 and TEA1613 provide ultimate controller supply flexibility. Due to the integrated high-voltage start-up source, the controllers can be started-up from any available high voltage rail, after which the supply function can be taken over by an auxiliary supply winding, or by means of a half-bridge point operated charge-pump supply arrangement. The integrated high-voltage start-up source will then be switched-off, reducing power consumption. Alternatively, the controller

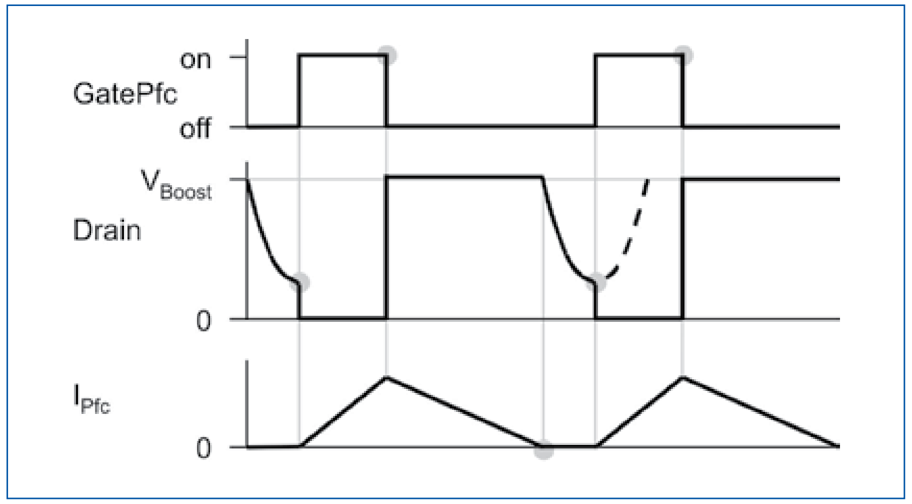


Figure 5: PFC Valley detection.

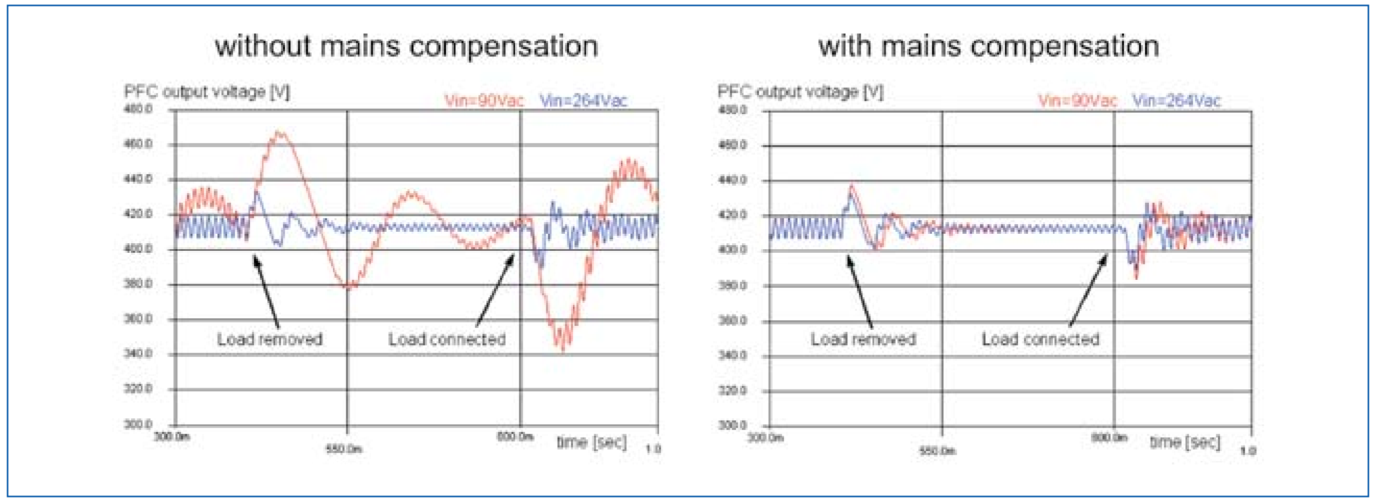


Figure 6: PFC Main compensation.

can also be supplied by means of a supply rail generated by a stand-by supply. The controller supply voltage ranges between 15V and 38V. An integrated series regulator will generate a safe and stable voltage (11V) for the gate drivers. The regulated voltage can be used as stabilised or reference voltage for external circuits.

Automatic start level selection of controller supply

In systems that use the high-voltage start-up source, a high start level of the controller supply (22V) is preferred. A large distance to the stop level (15V) allows the controller to operate from the charge in the buffer capacitor until the auxiliary winding takes over. In power supply applications that contain a separate standby supply, that standby supply can be used to supply the controller. Since it is continuously present, a much lower start level (17V) is allowed. The lower controller supply voltage reduces power dissipation. The TEA1713 and TEA1613 automatically select the appropriate start level by detecting the presence of the high-voltage.

Output under-voltage detection and restart timer

In systems where the controller is supplied from the HBC transformer, the controller will automatically stop when the output voltage drops during an overload or short because the controller supply also drops. This will not happen if a separate standby supply is used as controller supply source. In these cases, the integrated under-voltage detection of the output voltage and an integrated restart timer provide the same protective functionality.

Introduction to PFC topology

For power levels beyond 75Watt, mains harmonic reduction is required. The TEA1713 combines both the PFC and resonant controller into one IC. This allows good cooperation between both controllers and enables a cost effective power supply because the integration minimizes the number of external components.

The PFC generates a constant high voltage, which is the input of the resonant converter. The special built-in green functions allow a high efficiency at all power levels. This holds for quasi-resonant discontinuous operation at high power levels, quasi-resonant operation with valley skipping and medium power levels and burst-mode at low power levels.

Valley detection

The PFC operates in boundary conduction mode. To minimize switching losses, and thereby maximizing efficiency, the MOSFET is switched-on when the drain voltage is at its minimum. The controller senses the drain voltage and detects the valley. See Fig 5.

Mains compensation

A major disadvantage of a fixed output voltage boost converter in discontinuous mode is its input (mains) voltage dependent loop gain. To compensate the loop gain variation, the input (mains) voltage of the PFC is measured and used to automatically compensate the loop with a factor proportional to 1/Vmains2. Fig 6 shows the transient response to a load change without and with loop compensation.

NXP controllers

TEA1713

NXP's TEA1713 allows a small sized and cost effective system solution because of his high level of integration. It contains two controllers, one Power Factor Correction (PFC) controller and a resonant half-bridge (HBC) controller. In the 24-pins SO package all functions are available to build an efficient, safe and reliable power supply consisting of a power factor converter and a resonant converter.

TEA1613

NXP's TEA1613 is a resonant-only controller. It is suited for systems where the integrated PFC+HBC combination of the TEA1713 is not preferred. The TEA1613 in a 20-pin SO package has all the HBC and supply functionality of the TEA1713. In addition it has integrated burst mode detection. An output signal is available to hold the switching of an external PFC in burst mode.

With this series of products NXP is demonstrating its continued investment in the development of more energy efficient solutions like the TEA family and the trend towards higher efficiency power, resulting in smarter ICs that enable energy saving in end products.

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Die and Board Level Hot Spots

Thermal challenges need design solutions

For the past 50 years, the thermal management industry has offered only heat sinks, fans, and thermal grease as methods for electronics thermal management. During this same time electronic circuits have been packaged more tightly, generating more heat in a smaller footprint. As a result the electronics industry has reached a breaking point; a sort of thermal overload. The heat generated in these dense electronic systems can be quite large and has led to significant increases in on-chip temperatures that have reduced or limited the performance of components and systems.

By Dr. Paul A. Magill, Vice President of Marketing and Business Development, Nextreme Thermal Solutions, Inc.

The challenge of removing heat from ICs has increased significantly. This problem is no longer just at the chip-level but has grown to include hot spot formation on boards. The emergence of nano-electronics (90 nm feature size process technology going to 32nm by the end of the decade) has led to localized areas of high heat flux that are dominating the performance of electronics at the chip level. This same problem can also be found at the board level where devices such as MMICs, power MOSFETs and other power devices are being placed closer to devices, such as displays, that are very sensitive to high heat fluxes.

This article discusses methods for mitigating the effects of die-level and board-level hot spots through localized cooling of the on-chip heat source and the innovations that are driving new approaches in electronics cooling.

Thin-Film Thermoelectrics

Nextreme has introduced localized thermal management solutions deep inside electronic components using thin-film thermoelectric structures known as thermal bumps. The thermal bump was developed as a method for integrating active thermal management functionality at the chip level in the same manner that transistors, resistors and capacitors are integrated into conventional circuit designs today.

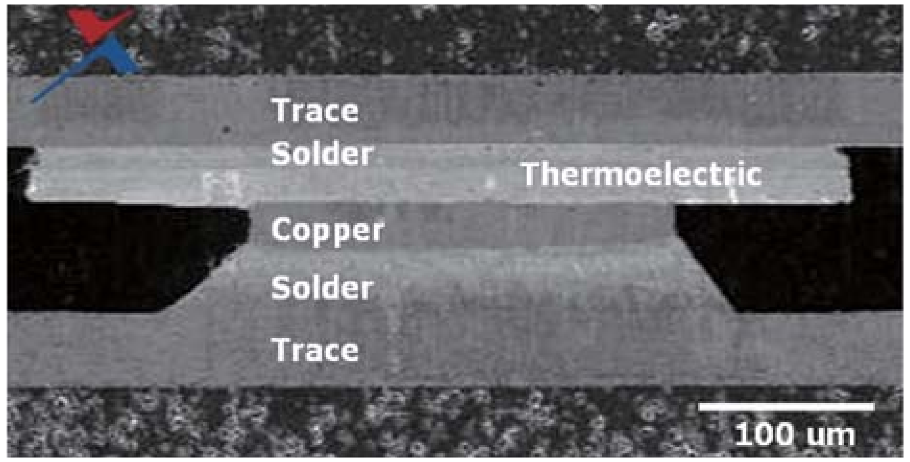

Figure 1. The thermal bump.

The thermal bump (Figure 1) is made from a thin-film thermally active material that is embedded into flip-chip interconnects (in particular copper pillar solder bumps) for use in electronics packaging.

Unlike conventional solder bumps that provide an electrical path and a mechanical connection to the package, thermal bumps act as solid-state heat pumps pulling heat from one side of the device and transferring it to the other as current is passed through the thermoelectric material.

The use of thermal bumps in power electronics offers many advantages in terms of size, efficiency and power-pumping capability. Thermal bumps today are already extremely small: 110µm (microns) in diameter by 65µm high and have the capability to be scaled to different sizes for different applications. The bump adds as little as 100 microns of thickness to a heat spreader, enabling unobtrusive integration close to the heat source.

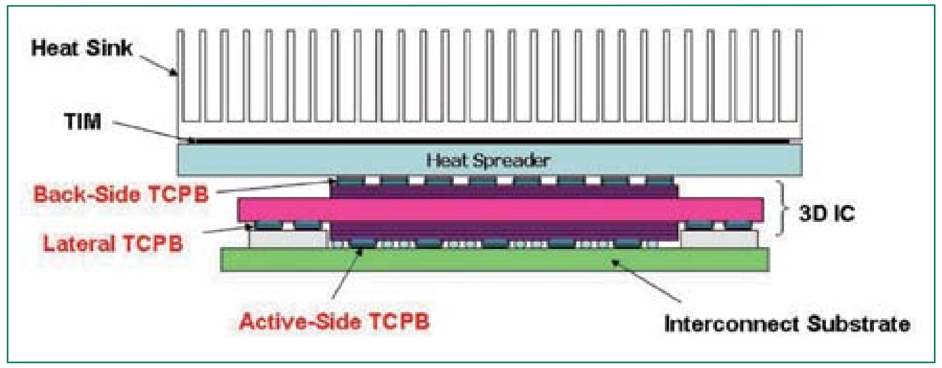

Figure 2. Integrated 3D Thermal Management.

Thermal bumps have been shown to achieve temperature differentials in excess of 60ºC between the top and bottom headers and have power pumping capabilities exceeding 150W/cm^2. This makes thermal bumps ideally suited for applications involving high heat-fluxes.

Today, thermal bumps can be introduced into systems at the chip level or at the board level using discrete modules. Here are a few of the integration possibilities:

Die/Chip Cooling

Thermal bumps can be integrated for heat removal from the back- or, front-side of the die and even laterally, as depicted in Figure 2.

Back-Side Cooling

Back-side cooling can be enhanced by the introduction of thermal bumps either into the heat sink to form an active heat sink or into the heat spreader. Here, discrete devices are used to mitigate hot spots generated on the front side of a die. In fact, while the following example demonstrates the feasibility of hot spot cooling using integrated thermoelectric cooling, it also reveals the limitations of cooling the hot spot from the backside of the die.

The hotspot is on the active side of the die while the cooling device is attached to the copper heat spreader. The heat spreader is flipped onto the backside of the die so that the cooler is located near the backside of the die, behind the first level thermal interface material, or TIM1.

Lateral Cooling

In the lateral cooling concept, current flows from left to right but the heat flows from the center of the module outwards. For a 3D chip stack, this lateral heat removal concept can be combined with an interposer through which the heat can be removed. Here the thermoelectric material is underneath the substrate and the heat is pulled from the center segment to the side.

In this example, the center of the platform will cool and the sides will become hotter as is shown. With this approach heat is dissipated laterally into the walls.

Active-Side Cooling

The last approach is active-side cooling. In Figure 3, an artist's rendition depicts the active side of a microprocessor. The smaller structures represent conventional copper pillar bumps next to the larger thermal bump. There could be as few as 10-20 or as many as 600-1200 thermal bumps strategically placed on the chip only in the vicinity of the hot spots. For this application it is not necessary to use a large amount of thermoelectric material – and in fact as little as 1mm x 1mm per hot spot – would be consumed to achieve the desired cooling effect   Placement of this material so close to the heat source would lead to a higher TEC efficiency.

Board Cooling

Hot spots on printed circuit boards can be cooled by the introduction of discrete modules strategically placed near the source of the heat. Metal traces, which can be several microns thick, can be stacked or interdigitated

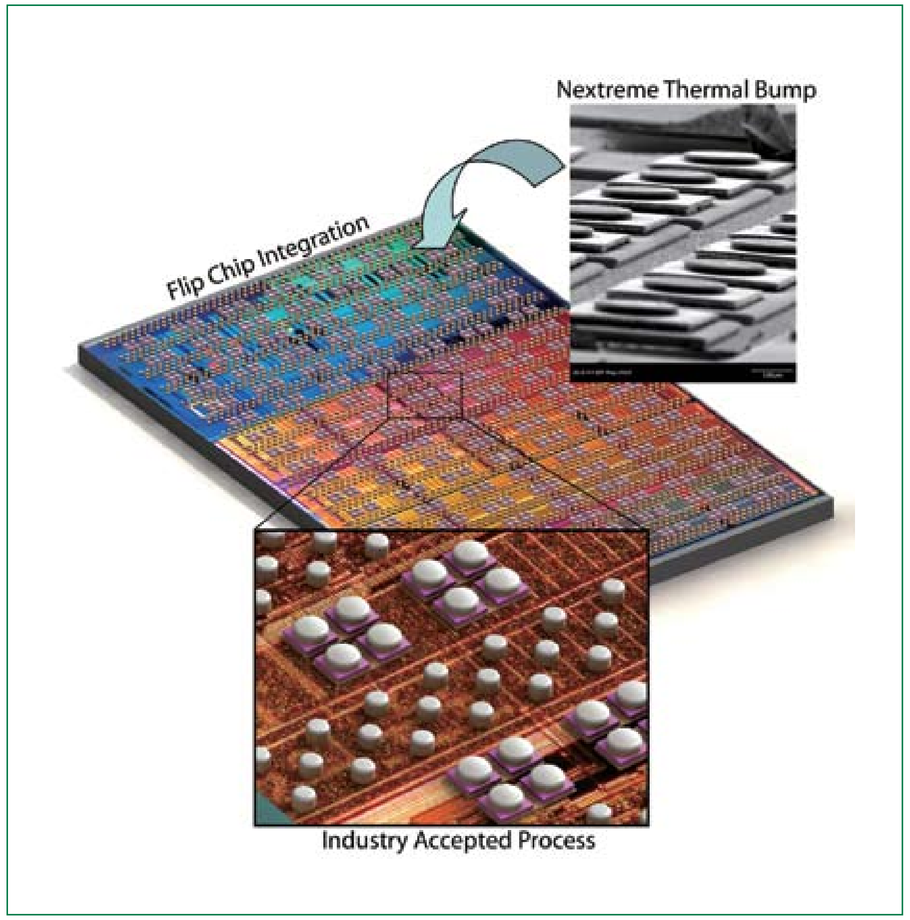

Figure 3. Thermal and electrical bumps integrated on a single substrate.

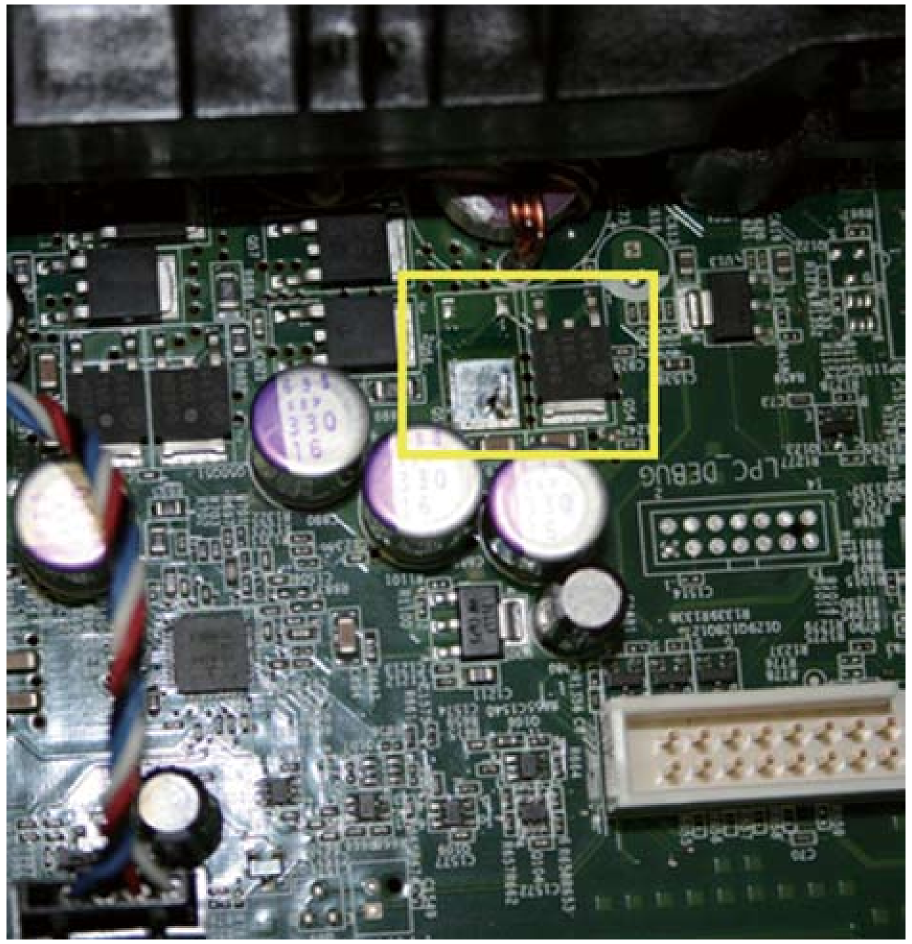

Figure 4. MOSFET replacement.

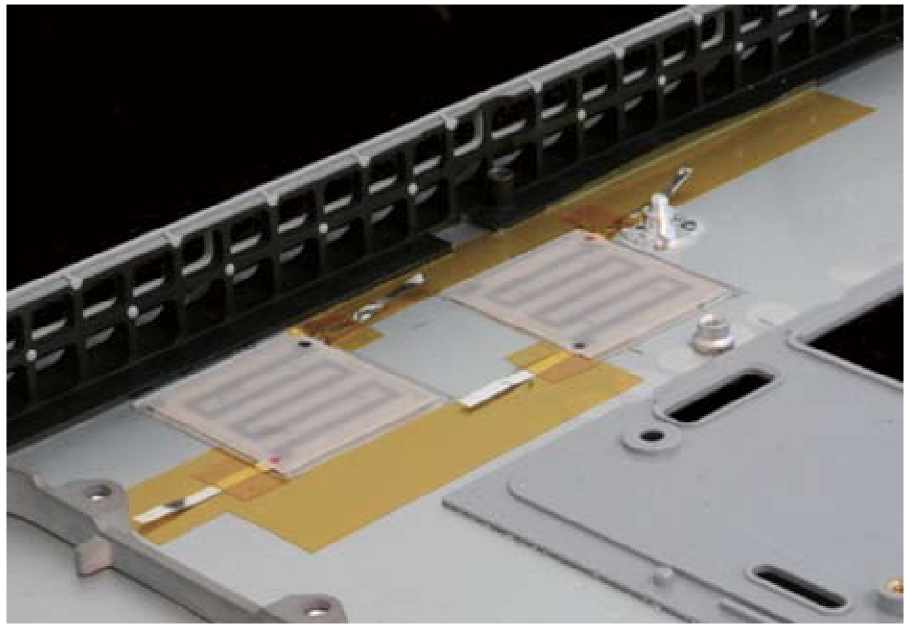

Figure 5: Two thermal barriers integrated into the chassis of a server.

to provide highly conductive pathways for collecting heat from the underlying circuit and funneling that heat to the thermal bump. Additionally, adding thermal vias (e.g., copper filled vias) would be required to provide pathways for the rejected heat.

In Figure 4, two MOSFETs were replaced by one eTEC cooled MOSFET. The ~0.5 W input power for the eTEC module translated to a ~3W increase in MOSFET output power.

Managing the heat flow in systems is also a problem for many manufacturers of mobile devices. Unlike electromagnetic energy, which can be isolated or confined, heat is mechanical in nature and hence can flow in any direction. This may include flowing towards sensitive components such as LCD displays. Thermoelectrics may be used to create a thermal barrier to the flow of this energy.

A thermal barrier creates a small temperature inversion that channels thermal energy away from the barrier and in a more desirable direction. A thermal barrier (Figure 5) may be constructed using several discrete thermoelectric devices but loosely spaced and powered only at a very low level.

The overall design, number of modules, their spacing, and the heat spreader materials and dimensions determine the characteristics of the thermal barrier. In most cases, a 3 to 5°C temperature inversion is all that is necessary to cause the heat to flow away from a surface, in essence creating a mirror or thermal reflector. The thermal barrier can be activated when the temperature of the board reaches a critical point, thus creating an "on-demand" thermal management solution.

Summary

The use of thermal bumps and discrete devices to provide a thermal management solution does not obviate the need for syste m-level cooling or for a reasonable means of rejecting heat out of the system. Rather, it offers the system design engineer a new set of tools with which to shape and enhance the performance of their system. Ultimately the focus should be on cooling what you need to cool and nothing else and then manage the removal of this heat in a controlled fashion.

www.nextremethermal.com

Dynamic & Static Power Management with SmartReflex™

High frequency buck converters conserve energy

As cellular phones and other portable electronics become more complex, more power is consumed by systems in both active and standby mode. Consequently, power-management design for portable devices imposes new challenges in the areas of core voltage, energy management and battery lifetime.

By Christophe Vaucourt, Portable Power Systems Engineer, Texas Instruments

Battery capacity simply cannot keep pace with the exciting new functionality on mobile handsets. While consumers demand new applications, they also want smaller, sleeker mobile devices, accelerating the trend toward higher levels of silicon integration and smaller digital submicron process geometries.

Increasing the microprocessor complexity increases its power consumption and with the smaller transistor structures responsible for higher achievable clock rates and increased performance, comes an inevitable penalty, increasing the leakage currents.

Leakage currents are present in any active circuit, independently of clock rates and usage scenarios. This static power consumption is mainly determined by transistor type and process technology. Higher clock rates also increase dynamic power, the power used when transistors switch. The dynamic power depends mainly on a specific usage scenario, clock rates, and I/O activity.

Texas Instruments' SmartReflex technology is used to decrease both static and dynamic power consumption while maintaining the device performance. SmartReflex in the OMAP™ devices is a feature that allows the core voltage to be optimized based on the process corner of the device.

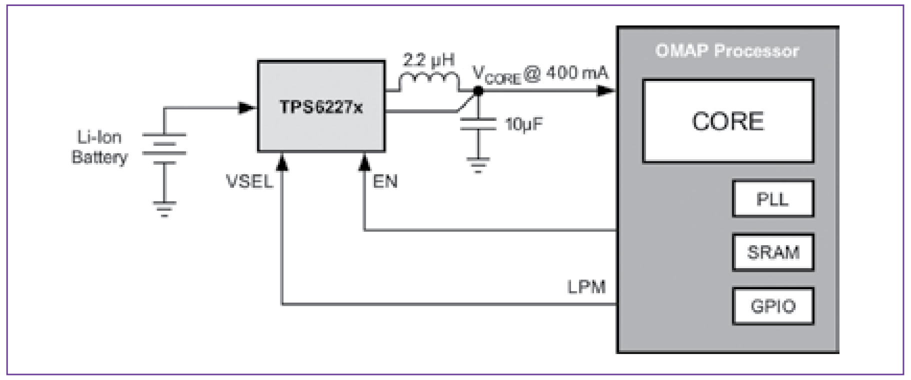

Figure 1: TI SmartReflex- Simple Voltage Scaling System Overview.

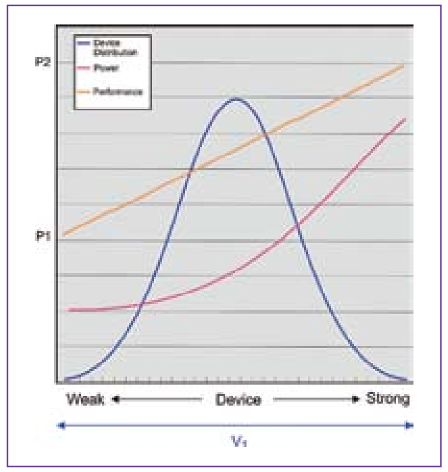

Figure 2: Performance and Power at Constant Core Voltage.

SmartReflex 1: Simple Dynamic Voltage Scaling

Power consumption of the processor can be reduced by lowering the internal clock frequency and/or even more by lowering the core supply voltage. Dynamic Voltage Scaling (DVS) is used to reduce core supply voltage to minimize power consumption.

Depending on the operating frequency of the processor, the core voltage can be dynamically and very accurately adapted to its lower limit in order to minimize power consumption. This principle can be used not only to reduce power consumption in active mode but also to extend standby time through a reduction of leakage currents effects in deep-sleep mode.

The following relationship describes the power consumption of a digital processor:

$P_C \approx V_C^2 \times f$

P_C: Core Power Consumption

V_C: Core Supply Voltage

f: Core Clock Frequency

As can be seen, the power consumption can be reduced by lowering the clock frequency and even more by lowering the supply voltage.

The TPS6227x device features an output voltage selection input pin (VSEL). The DC/DC output voltage is set internally by the means of a high precision feedback divider network. No further external components for output voltage setting or compensation are required, thereby enabling for smallest solution size.

Connecting the VSEL input to an external logic control signal allows simple dynamic voltage scaling for low-power processor core operation. For best performance, the DC/DC output voltage can be changed "*on-the-fly*" without restrictions.

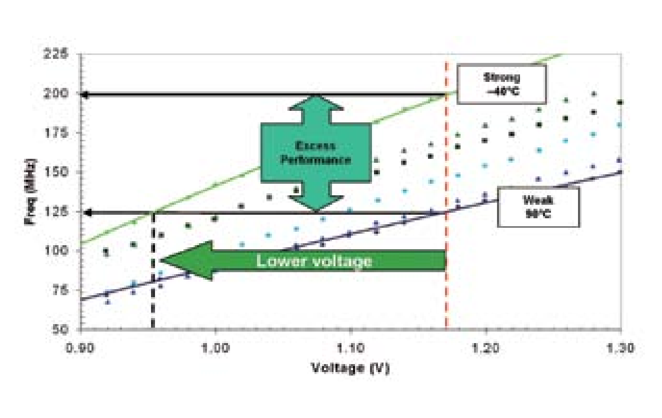

Figure 3: Performance vs. Process, Temperature and Voltage.

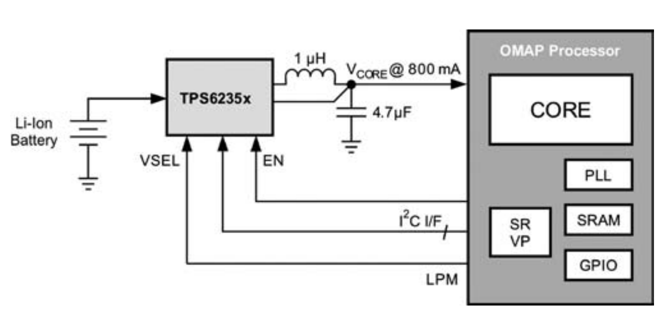

Figure 4: TI SmartReflex 2 - System Overview.

SmartReflex 2: A More Comprehensive System-Level Solution

For high-performance, power-sensitive applications, power reduction is only half the challenge. Providing higher performance while consuming less energy per function is imperative.

In addition to dynamic power (the power that is consumed when transistors switch), modern processors are encountering new standby leakage power challenges caused by shrinking component geometries. Unfortunately, moving down the process scale from 90 to 65 to 45 nanometer (nm) has an exponential effect on leakage power; leakage thus becomes an increasingly significant percentage of a device's total power.

While digital processors are getting more and more powerful, their active power consumption tremendously increases translating into new heat dissipation challenges.

It is desirable to minimize the power

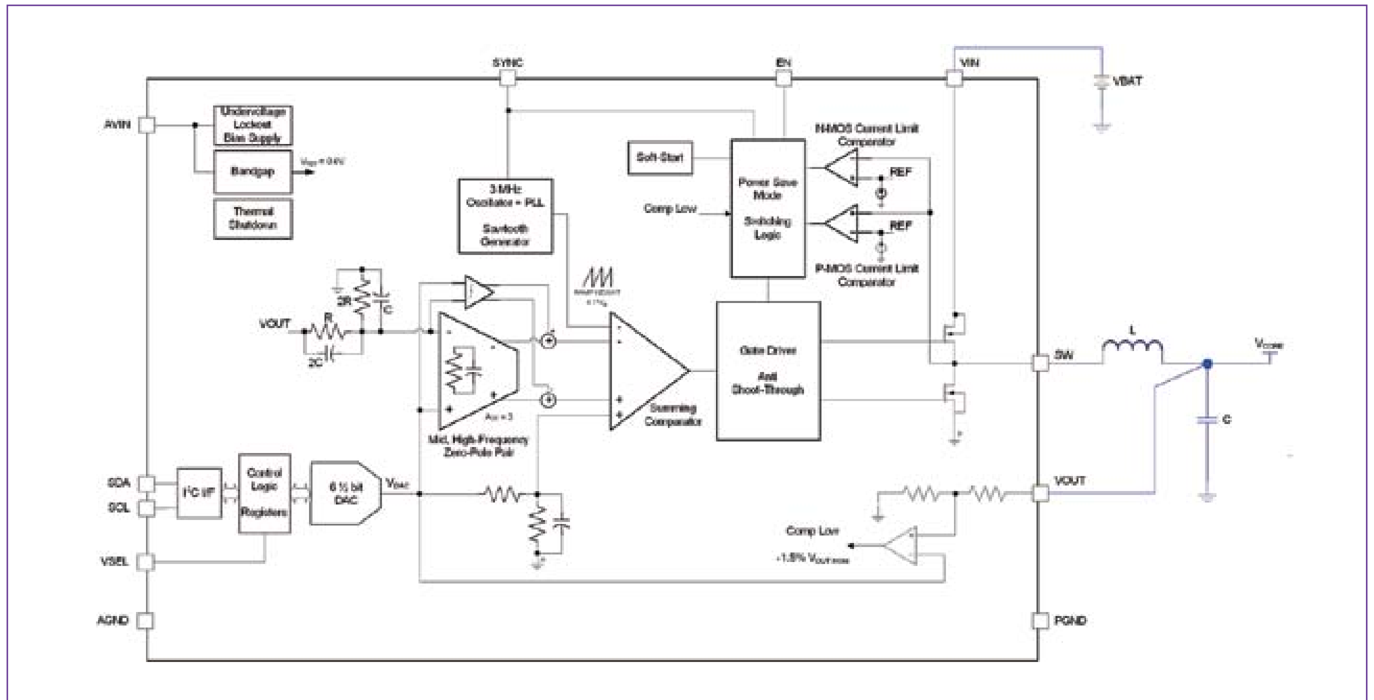

Figure 5: Fast Response SmartReflex 2 Compliant Regulator Block Diagram.

consumption while maintaining the target performance. The baseline power is the power consumed independent of the processor activity, and it is dominated by leakage power. The active power is the power consumed by active parts of the processor; this power can be separated by the major modules within the digital device. If a module is not enabled, there is no active power consumption from that module.

The theoretical performance and power consumption for a general bell-curved manufacturing distribution is shown in Figure 2, with (P1, V1) representing the nominal OPP (Operating Performance Point) and P2 representing the performance for the strong device at V1.

The extra performance margin cannot be utilized and a significant amount of extra power (both leakage power and active power) is consumed for strong devices operating at (P1, V1).

In the case of this particular TI OMAP^{TM} device, the nominal OPP for the core is (125MHz, 1.15V); a strong device is capable of running at the same speed with a much lower supplied voltage or running at a much higher speed with the same supplied voltage.

SmartReflex 2: Hardware Implementation

SmartReflex 2 is a technology that uses adaptive voltage scaling (AVS) to reduce active power consumption. The voltage is adjusted within the defined range and SmartReflex^{TM} voltage processor assures that the voltage applied is sufficient for each device (of different strength) to operate at the nominal OPP frequency.

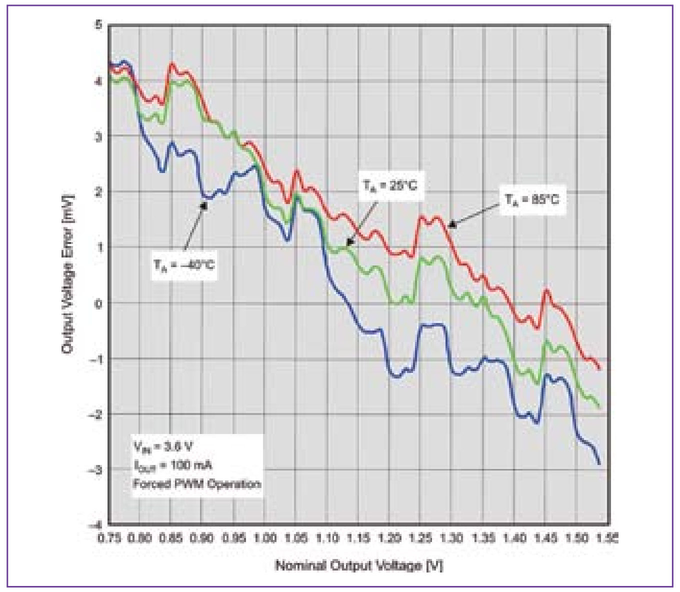

Figure 6: Output Voltage vs. Digital Code.

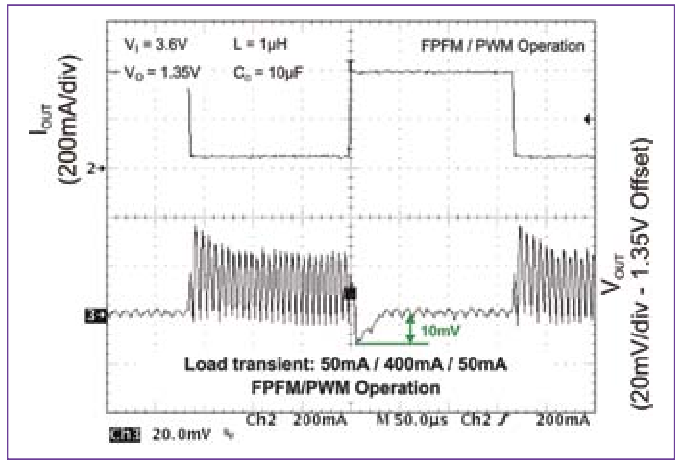

Figure 7: FPFM Load Transient Response.

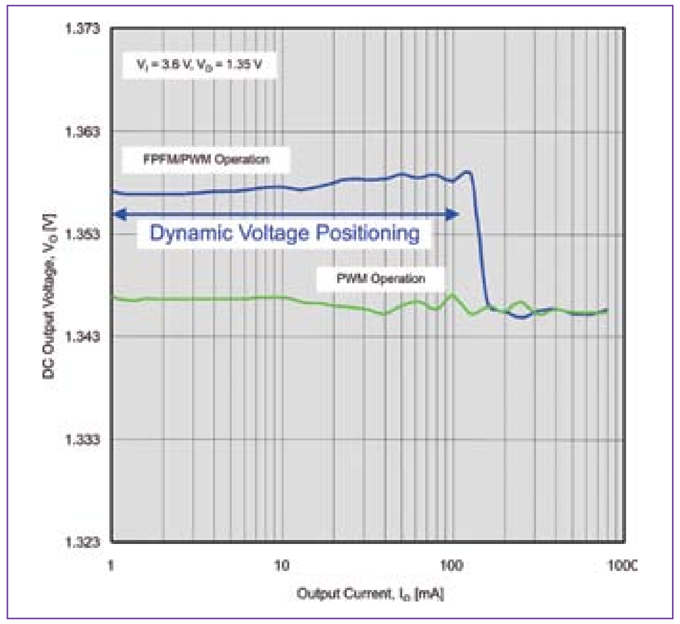

Figure 8: Dynamic Voltage Positioning DC Regulation Accuracy.

In the simplest approach (SmartReflex 2 Class-0), the processor performance is measured at manufacturing test and the required operating voltage for that device is determined. This information is permanently stored into the device. During boot-time, the SmartReflex 2 control output (e.g. simple logic signals or I_2C I/F) is sent to the power supply to select the appropriate core voltage level.

Modern regulators aim not only to provide state-of-the art electrical performance but also small solution size. To address TI's SmartReflex requirements, a dedicated high switching frequency converters operating at 3MHz nominal fixed frequency has been developed.

With an output voltage range adjustable via I_2C interface down to 0.6V, the TPS6235x series supports low-voltage DSP and OMAP processor core power supplies in smart-phones and handheld computer. The communication interface is used for dynamic voltage scaling with voltage steps down to 12.5mV, for reprogramming the mode of operation (Light PFM, Fast PFM or Forced PWM) or disable/enabling the output voltage.

With increasing SmartReflex 2 implementation class comes increasing power savings benefits, but also increased system complexity. In Class-2 and -3 implementations, either software or a hardware voltage processor (VP) continuously adjusts the supply voltage to changing environmental conditions.

The AVS system offers optimal voltage scaling for a given processor. By virtue of closed-loop performance regulation, the lowest voltage for a given operation condition is always selected.

The voltage processor contained in the digital processor further reduces system integration complexity by providing an automatic handshaking between voltage scaling and frequency scaling. Through closed-loop control and configurable gains, the maximum system energy efficiency is achieved.

To support closed-loop operation, the TPS62350 device features a 6.5-bit resolution monotonic output voltage response vs. digital voltage code.

To maintain correct functionality on digital processors embedding SmartReflex technology, the power supply must be designed to provide a core voltage with a maximum 5% error (covering DC accuracy and AC transient response).

To address these very tight regulation requirements, the TPS6235x device converter uses a unique advanced summing comparator fast response, voltage mode, controller scheme with input voltage feed-forward. This achieves “best-in-class” load and line response and allows the use of tiny inductors (1µH) and small ceramic input and output capacitors (4.7µF).

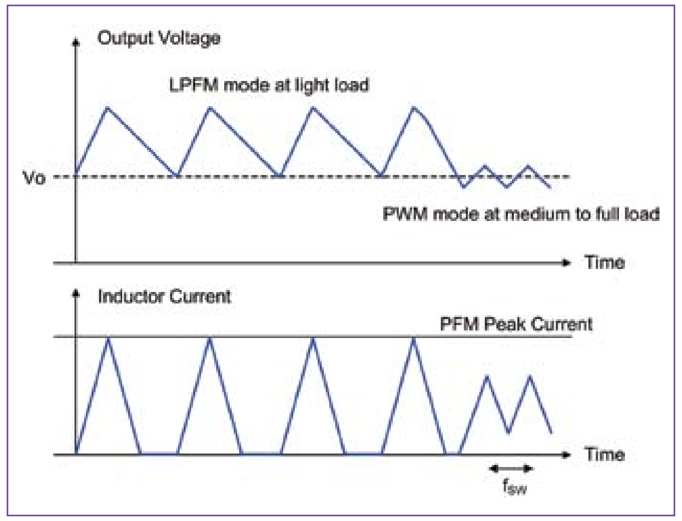

Figure 9: Single Pulse, Variable Peak Current PFM Principle (Light PFM).

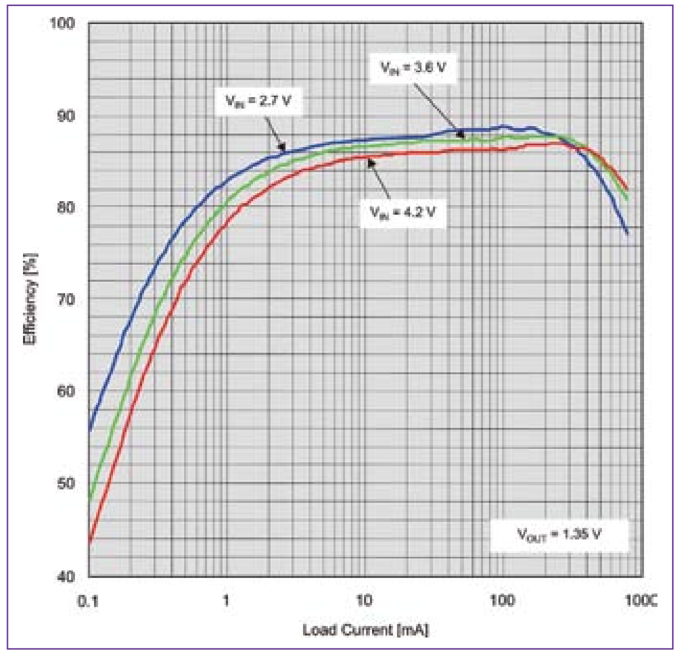

Figure 10: Light PFM Efficiency.

During light-load conditions, the TPS6235x converter includes a complementary Fast PFM (FPFM) mode to enhance efficiency without compromising on the transient performance. Fast-PFM mode helps to shorten the wake-up time of the inner regulator circuit. At the expense of larger quiescent current consumption (ca. 90µA), the regulator's activation time can be dramatically reduced thereby transitioning smoothly between FPFM and PWM modes.

“Dynamic Voltage Positioning” regulates the output voltage in PFM mode slightly higher than the nominal value (PWM mode). The output voltage is set higher in the magnitude of 1% typ, thereby giving additional headroom to minimize the absolute voltage sag.

Figure 7 shows the load transient performance of a Fast-PFM scheme. In a nutshell, the Fast-PFM mode reduces the transient voltage drop by a factor of two compared to other switched mode regulators.

Fast PFM mode offers the excellent transient response performance during large load swings, at the expense of the ultra-light load efficiency (i.e. sub 10mA). Light PFM (LPFM) mode features lower quiescent current (c.a. 30µA), reduced output ripple voltage giving-up a bit on transient performance.

In light PFM mode, the converter only operates when the output voltage trips below a set threshold voltage (i.e. nominal output voltage). It ramps-up the output voltage with a single or multiple pulses and goes back into power-save mode. As a consequence in power-save mode, the average output voltage is slightly higher than its nominal value in PWM mode and the light-load efficiency is dramatically improved.

Conclusion

The solid foundation for SmartReflex technologies now extends outward with the second-generation features of SmartReflex 2: adaptive power supply to reduce digital processor leakage and active power consumption.

Each SmartReflex implementation class has different advantages. With increasing SmartReflex 2 implementation class comes increasing power savings benefits, but also increased system complexity.

Each design must choose the class of SmartReflex 2 implementation that best suits its requirements. TI's discrete solutions for dynamic voltage management supports fast and accurate voltage scaling as required by today's and tomorrow's processor cores. The small package of TPS62270, TPS62350 and the limited amount of external components makes them an ideal choice in real estate sensitive applications.

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Making Sense of Power Specifications

Putting the data into power supply data sheets

Why is it that seemingly similar power supplies have significantly different performance and reliability characteristics? The answer may lie in the specification detail that can be missing from some data sheets, available only in the long-form data/application notes or may even be due to “specmanship”.

By Gary Bocock, Technical Director, XP Power, UK

Let's look at typical data for an AC/DC power supply, though many of the issues may equally apply to DC/DC converters.

Input Characteristics

Input voltage range

AC/DC power supplies are typically universal in nature, meaning that they operate over a wide range of input voltages, normally from 85 or 90VAC up to 264VAC. This feature allows a single product to operate world-wide without changes in configuration of the input stage. Some products utilise automatic input voltage range selection giving two operating ranges; typically 90 to 132VAC & 180 to 264VAC. Universal input power supplies provide better immunity to supply disturbances in some circumstances and this may be a benefit.

If the power supply is to be used close to its full power capability within the application it is important to check the specification details on the available output power in the low input voltage area, where some products de-rate by as much as 20 or 30%, meaning that they may be operating outside of specification when operating from nominal 100VAC or 115/120VAC supplies or at the very least may infringe the design margins of the end equipment. Ignoring this de-rating in the available output power will seriously affect the reliability and life time of the power supply and therefore the end equipment.

De-rating the power supply output power at low input voltages is common in lower cost universal input power supplies and is normally due to the limitations of the active power correction boost converters employed.

Earth leakage current

Earth leakage current is a parameter which varies widely from product to product. The earth leakage current is largely a consequence of EMC filtering within the power supply and is normally only a key consideration in medical applications or in installations or equipment using multiple AC/DC products or where external EMC filters are utilised to reduce overall system noise.

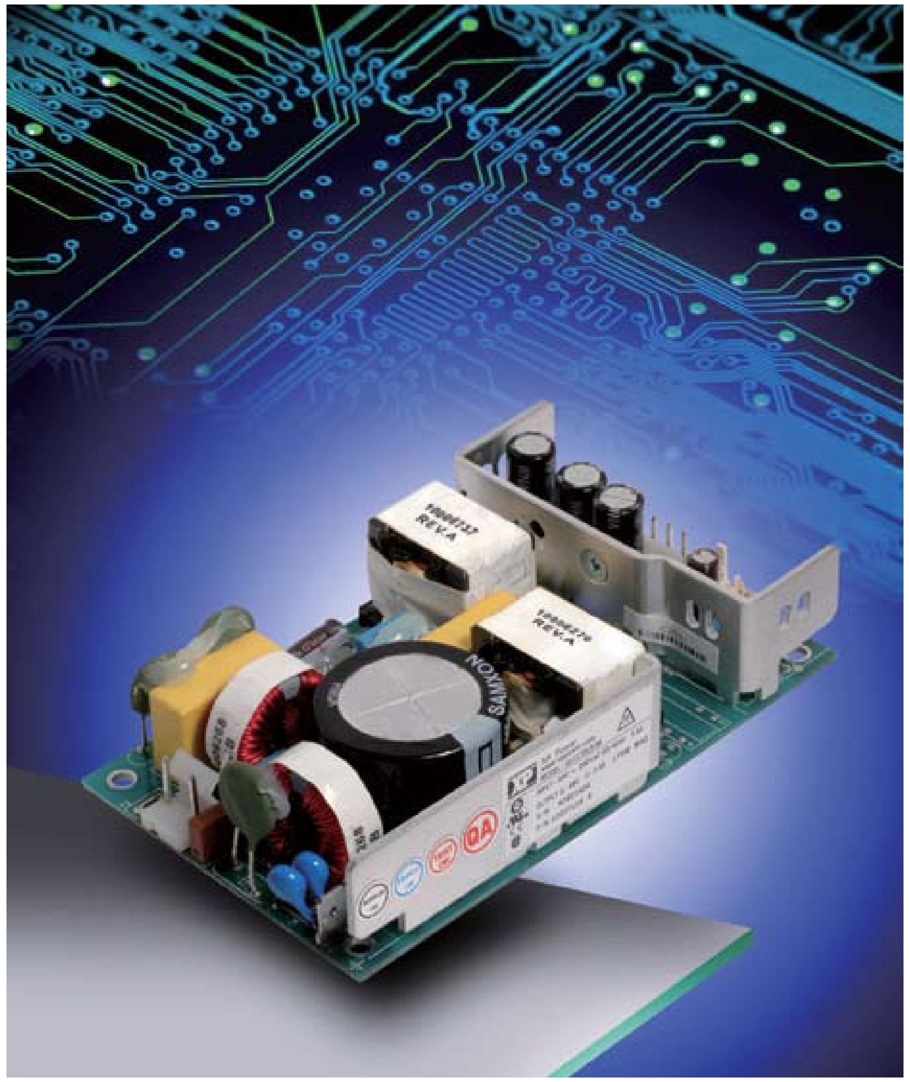
Inrush Current

A key consideration affecting the selection of fuses, filters and switchgear is the inrush current at the point of application of the AC power. The maximum inrush current is usually specified in the data sheet however there is more to this than a simple maximum value.

In lower power, lower cost products the inrush limiting is typically via a simple NTC thermistor which will provide protection from a “cold start” but may take a minute or more to return to its initial value following the initial switch on. This results in an inrush current many times the specified maximum during an off/on cycle even with a relatively long delay. The inrush current is also likely be specified at 25ºC and may be significantly higher even for a cold start in higher ambient temperatures.

In products above a few hundred watts, this thermistor is likely to be taken out of circuit once the output voltage is established, to remove unnecessary power dissipation, removing this as an issue.

Inrush current is an important factor to be considered to avoid nuisance tripping of fuses and circuit breakers as well as reliability of switches and filtering. The fuse rating given in some data sheets is usually the rating of the internal fuse which is designed to operate only in the event of catastrophic failure and is not user replaceable. Determining the value of the equipment fuse needs to take into account the normal maximum running current, the inrush current and the effects of aging. The equipment fuse should also only be required to operate under catastrophic failure conditions as the electronic power supply overload protection will cater for any problems on the DC side.



The 3" x 5" CLC175 AC/DC power supply from XP Power is capable of delivering its 175W full load output with only 10CFM airflow.

Output characteristics

Overload protection

All power supplies offer overload protection to protect both the power supply and the load tracking and wiring from overheating. This may come in a number of different guises or characteristics.

In low power products a trip and restart or "hiccup" mode is common as this helps to keep costs down by utilising primary control schemes. Trip & restart overload schemes are generally unsuitable for loads involving high start up currents such as electromechanical equipment, lighting equipment or applications which have a high capacitive element, as start up may be unreliable and variable even from unit to unit. This overload characteristic is also unsuitable for direct battery charging applications. With these types of load a constant current overload characteristic is desirable.

Remote Sense

Low voltage high current applications will benefit from products which offer remote sense where the output voltage can be measured at the point of load. This feature is particularly desirable where the load is variable. If the load is relatively constant then a simple user adjustment of the output voltage will be adequate and more readily available though may result in other voltage rails also being adjusted by the same percentage in multiple out supplies where the additional rails are often semi-regulated.

Output accuracy and minimum loads

Output accuracy or regulation is specified in many different ways by various manufacturers. It should encompass line regulation, load regulation, cross regulation (for multiple output supplies), transient response, initial set accuracy and temperature coefficient. These parameters can be specified over differing input ranges, load ranges, load step changes and temperature ranges etc. While these items can be presented in many ways the majority of single output supplies will have comparable performance. Perhaps the most important consideration is for multiple output units where the performance can be very different.

Single output power supplies rarely require a minimum load but multiple output units often require minimum loads on one or more outputs and this should be made clear on the product data. Minimum loads are normally specified to reduce the effects of cross regulation between outputs and to maintain the output accuracy within the specified limits. These minimum loads will need to be considered in the system design and where necessary components added to ensure that they are met.

As standby/no load power consumption requirements reduce, the addition of minimum loads is becoming a real system performance issue and other solutions are required, particularly in low power applications where features such as inhibit are rare due to market cost requirements and the primary control systems in general use.

Output ripple & noise

Ripple & noise is one of the product performance specifications which is most open to interpretation, making comparison from the data sheet difficult if not impossible. The main variables are the measurement bandwidth and the use of various external components and measurement techniques. The only real way to compare performance is to measure the products under the same measurement regime.

Efficiency

Most data sheets will offer a figure for efficiency allowing the user to quantify the waste heat generated within the end equipment. The efficiency of a power supply will vary dependant on the load and input voltage applied, so it is important to understand the unit's efficiency under the operating conditions of the application. Efficiency during operation at low line is typically lower than at high line and may vary by as much as 6-7%. The most important parameter is the worst case efficiency in order to understand the maximum waste heat generation by the supply.

The drive in power supply development is to increase efficiency in order to reduce the physical size of the product and reduce power consumption. This is also being driven by the standby/no load power and average active efficiency requirements set out in legislation such as Energy Star, CEC, EISA and EUP.

Power density specifications are being increasingly used by power supply and DC/DC converter manufacturers to convey advancement in power technology & efficiency. If these watts per cubic inch specifications are compared it is essential to ensure that the products have similar specifications and do not require external components to meet various specification requirements.

Reliability, Temperature & Cooling

The normal measure of reliability of power converters is given as Mean Time between Failure (MTBF). The MTBF is normally calculated based on the predicted failure rate of the components utilised within the product, a so called parts count method. When comparing the MTBF of various supplies there are a number of key parameters to check to ensure that the specifications are indeed comparable. Firstly the methodology needs to be identical; typical methods are MIL217 at its various issue levels and Bellcore RPP (now managed by Telcordia Technologies). These two methodologies will give very different results and cannot be compared to one another. Where the MTBF is given to the same specification then in order to be compared it must also be stated under the same environmental conditions to prove a useful tool to the system designer.

The most influential factor in terms of reliability and lifetime is the ambient temperature and effective cooling of the power supply. Convection cooled products need adequate space to cool effectively and forced cooling requirements need to be carefully considered to ensure that the product is adequately cooled in the specific application. Manufacturers are increasingly providing key measurement points within the sub assembly to ensure that the product will be both safe and reliable and to ensure adequate lifetime. Thermal de-rating data is normally provided up to ambient temperatures around 60 to 70ºC. Careful consideration of this data is required since some products de-rate from as low as 40ºC. For example, most power supplies from XP Power de-rate from a minimum of 50ºC, some from 60ºC. Also, be aware that while a unit might be specified to operate at an ambient temperate of, say, 40ºC, when the unit is enclosed within end-user equipment the internal temperature can be much higher than that.

Airflow is another important consideration. Be aware that some products may specify an airflow rate that might be difficult to achieve in practice e.g. 20 – 30CFM. As a guide, look for a required airflow less than 15CFM. Typically, XP's products require 10 – 13CFM.

EMC

Datasheets include EMC specifications. Open frame products include conducted emissions and conducted immunity specifications with some providing information on radiated emissions and radiated immunity, some may require additional components to meet the stated performance so these should be considered when selecting the product for the application. External power supplies must provide specifications for both conducted and radiated EMC performance as these are considered stand alone products. Typically the products are evaluated using passive loads in an ideal test set-up which is unlikely to be replicated in the end application so choosing a supply with local engineering support and test facilities will be an advantage during the end product development.

In summary, power supply and DC/DC converter data sheets contain a lot of information which needs careful consideration when applied to the end application. The data is generated with the power supply or converter in isolation and in some instances additional components are required to meet the various parameters. Cooling and de-rating information may differ significantly between products though this is not always apparent in short form data and efficiency data is normally given under best case rather than worst case conditions. How well the power supply performs in the end application is the key consideration and a study of the long form data and application notes will often provide the detail required to select the best power solution for your system.

XP's Power Supply Technical Guide is a free 148-page guide to power system technology. It is available to download free-of-charge from the XP website.

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PSDE Green Power ENERGY EFFICIENCY

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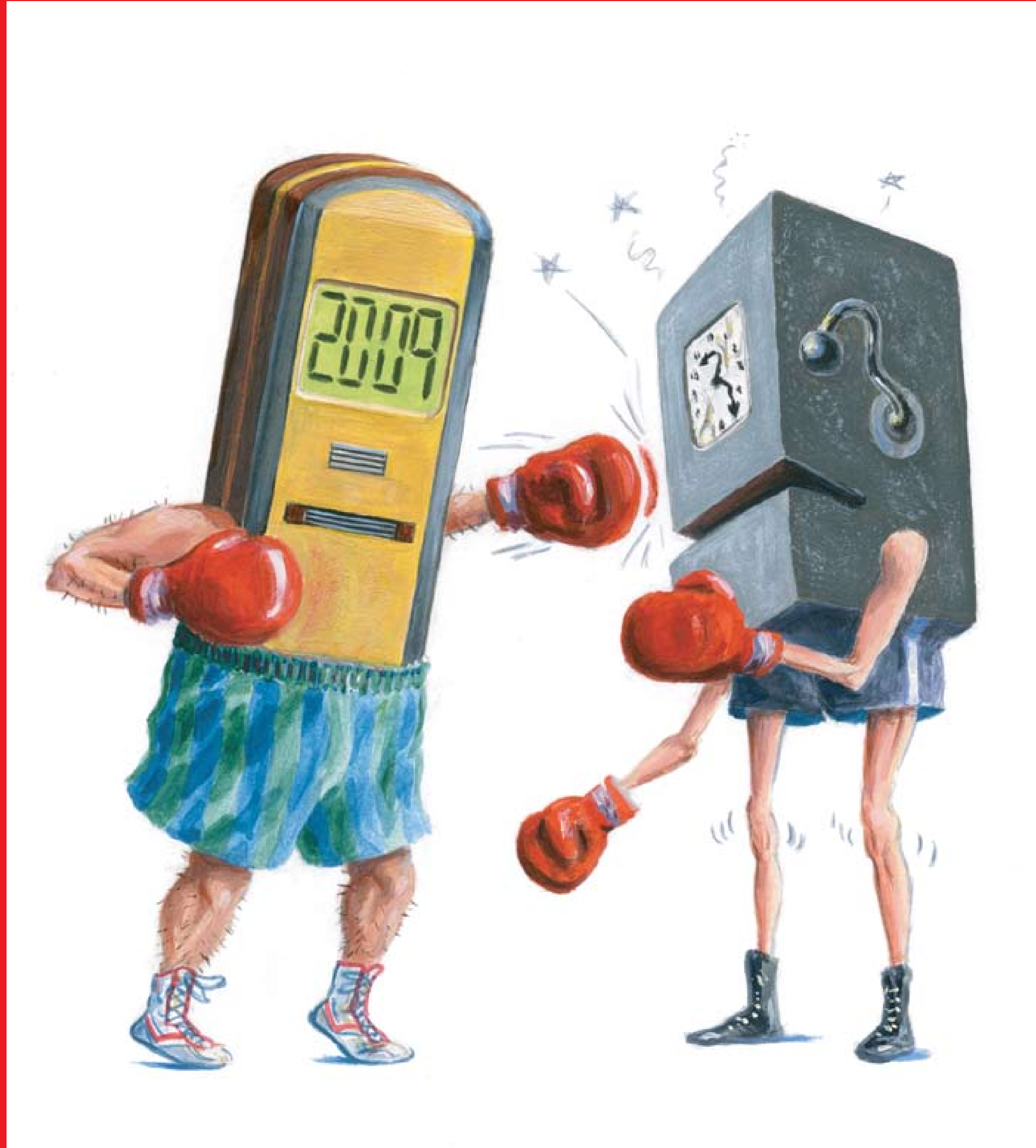

Digital Power Eases Designer's Burden

DC-DC conversion with Auto-control™

Regulation of supply rails, from a control perspective is traditionally the domain of analog integrated circuits. But current trends in power conversion are moving the industry to smaller and more efficient power architectures. The requirement to intelligently manage the multiple power rails under these constraints of space and efficiency is driving the industry towards research, development and adoption of digital power control and power management solutions.

By Anthony Kelly Ph.D. MBA, VP Digital Control, Powervation, Limerick, Ireland

The economics of IC design support the adoption of digital power control because the cost reduction of digital circuits is more rapid over time, leading to cost parity of digital and analog power control ICs, with digital solutions ultimately being cheaper. Factoring in the requirement for advanced power management, which is a digital function, the economics of IC design point to increased demand for digital power controllers and therefore they are expected to be a very significant proportion of the market (greater than 40%) by 2011.

Taken together, these trends indicate that there is significant potential for the development of power control technologies which harness uniquely digital techniques in order to deliver improvements in power system design. Indeed, such improvements have been looked forward to for some time. Now it is time to deliver.

We will examine DC-DC conversion from a control perspective, introducing key differences compared to analog techniques, looking at key control issues such as robustness and finally introducing truly adaptive Auto-controlTM technology which uses digital processing to deliver improved control.

Overview of Digital Power Control

Figure 1 illustrates a typical digital DC-DC converter, comprising of the power stage, output voltage V_{OUT} (y) sampling ADC, digital error amplifier / compensator, and digital Pulse-Width-Modulation (PWM).

There are several differences between analog and digital DC-DC converters, some of the most significant are:

a) The output voltage (y) as seen by the control loop is quantized in voltage. This means the output voltage is known to the resolution and accuracy of the ADC.

b) The output voltage is sampled in time and therefore is only known at the sampling instants.

c) The Digital Pulse-Width-Modulation (DPWM) is quantized in time and therefore discrete quantized pulse widths are available. The interaction between the DPWM's quantized levels and those of the ADC can result in limit cycling whereby the DPWM's pulse width never settles to a steady state. This results in a limit-cycle on VOUT, the amplitude of which is dependent on several factors and is a function of the DPWM's resolution.

d) The ADC requires some time to convert the VOUT reading into a digital value, adding to delay in the loop.

e) The compensator adds to the loop delay because it requires some time to compute the duty-cycle following each ADC reading.

The delays inherent in a digital PWM control loop place a bound on the achievable control bandwidth which in turn affects the control response and therefore the deviation in the transient response to a load current step. The maximum control bandwidth achievable when a control loop has a delay of Td is approximately:

$$f_{\max} \approx \frac{1}{2\pi T_d}$$

Intuitively this makes sense; the control loop cannot react to a disturbance until the ADC has measured it and the controller has calculated a response. In the meantime the output voltage will continue on its trajectory giving a minimum achievable voltage deviation to the load transient and equivalently, a maximum achievable control bandwidth.

This means that in a typical digital DC-DC converter where the ADC sample rate is the same as the switching frequency, and there is a one cycle delay from ADC sample to DPWM update the maximum achievable control bandwidth is:

$$f_{\max} \approx \frac{f_{sw}}{2\pi}$$

In reality the delay inherent in PWM modulation must also be taken into account, reducing the maximum achievable bandwidth even further.

Clearly the transport delay is an important figure of merit for a digital DC-DC converter. It is as low as 400ns for Powervation's technology.

The Role of Control

Consider the controller depicted in Figure 2 where the compensator and plant are represented by C and G respectively. The role of control is to ensure the output (y), tracks the reference (r), in the presence of a) unknown disturbances and b) uncertainty regarding the parameters (or structure) of the power stage. Feedback control facilitates this through high loop gain.

However, the gain must roll-off at high frequencies in any physically realisable system. This is illustrated in Figure 3, where the loop gain is shown as CG. As CG rolls off we can see there are conflicting requirements between loop stability and robustness. For example, to ensure that the loop is insensitive to a high degree of plant uncertainty requires high loop gain up to a high bandwidth. However, the loop gain must roll-off at high frequencies in order to ensure loop stability, with lower bandwidth systems being more stable. Therefore there is a fundamental trade-off between loop stability and robustness versus uncertainty regarding the power stage. In practice control loops are designed with lower bandwidths so they are stable despite plant uncertainty. Robustness is achieved by ensuring a high phase margin.

Robustness

Loop phase margins, gain margins and crossover frequencies are typically designed conservatively when robustness is considered in physical systems. This comes about because the control loop is particularly sensitive to inaccuracies in the dynamic modelling of the power stage as the loop gain rolls off and crosses 0dB.

We can view phase-margin as a measure of robustness against delay uncertainty at the 0dB crossover frequency, i.e. high phase margin systems can tolerate more uncertainty in loop delay without being unstable. The amount of additional delay a loop can tolerate (Tmax), for a given phase margin (PM, in radians) and crossover frequency (ωc in rad/s) is given by:

$$T_{\max} = \frac{PM}{\omega_c}$$

Therefore, loops with higher phase

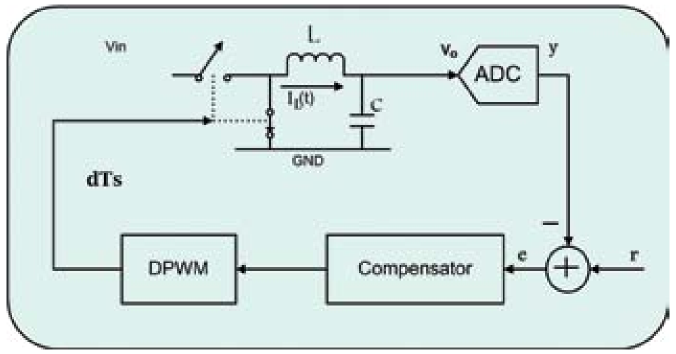

Figure 1: Typical Digital DC-DC Converter.

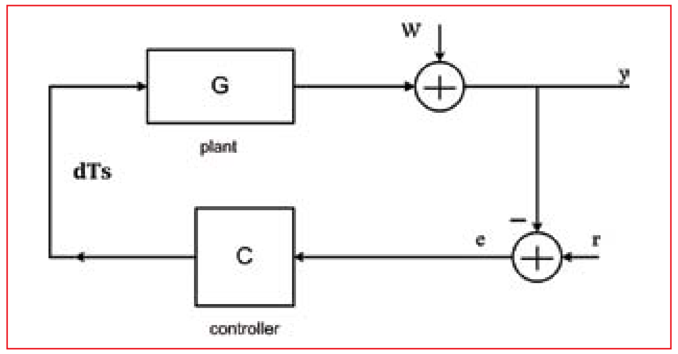

Figure 2: Representation of a feedback control system.

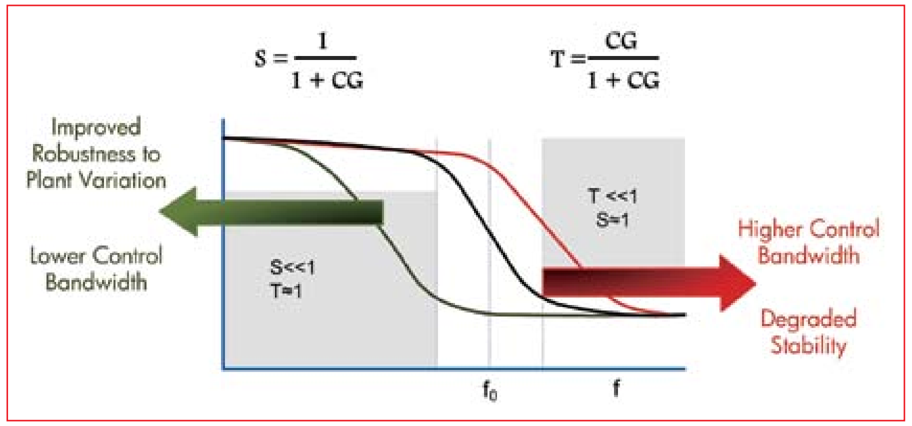

Figure 3: Conflicting requirements of Sensitivity and Robustness as the Loop Gain (CG) rolls off versus frequency.

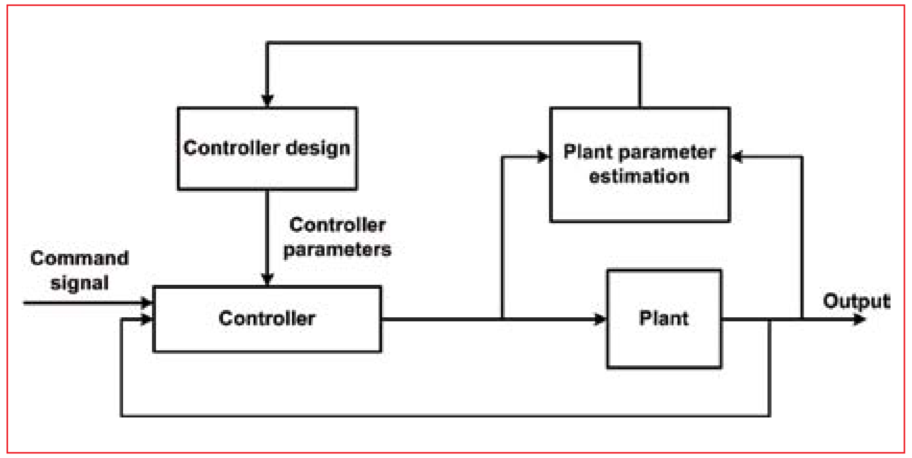

Figure 4: Typical adaptive self-tuning regulator.

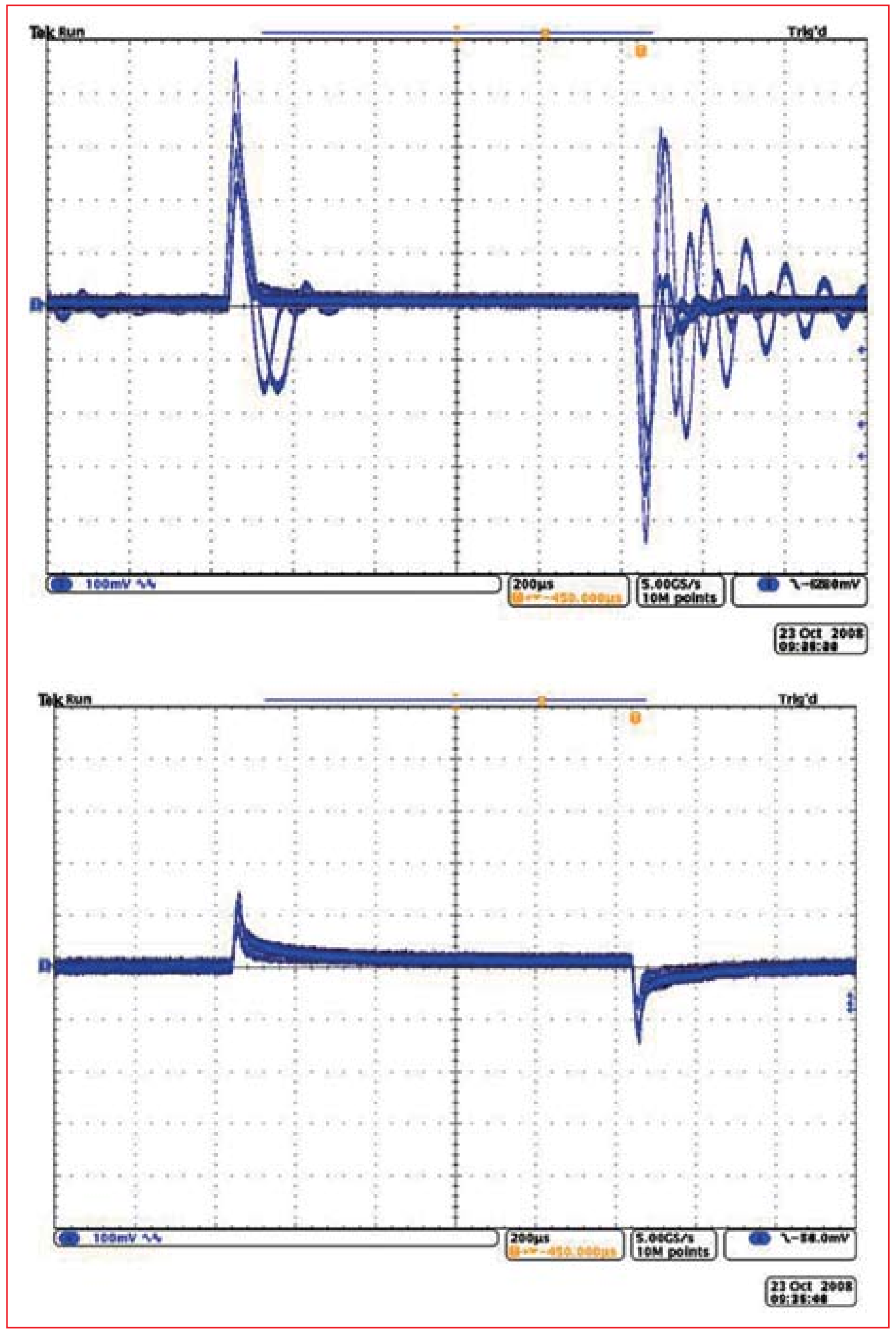

Figure 5: (a) Varying load step response as L and C vary in a DC-DC converter; (b) Improved robustness to variation when controlled with Powervation's Auto-controlTM technology.

margin or lower crossover frequency are more robust against uncertainty in loop delay. Similarly we can view gain-margin as a measure of robustness against gain uncertainty at crossover, i.e. high gain margin systems can tolerate more uncertainty in gain at crossover without being unstable.

Adaptive Control

A typical adaptive control system is illustrated in Figure 4, whereby the parameters of the plant are estimated by the 'plant parameter estimation' block and the controller is designed on-the-fly by the 'controller design' block to meet some pre-determined requirements such as closed loop pole locations.

One of the main advantages of adaptive control is that plant uncertainty is reduced by the parametric estimation. As the uncertainty in the control system is reduced it becomes more robust, and the limitations on control performance to achieve robustness are relaxed. As such the loop can maintain high gain up to as high a bandwidth as stability will allow.

Traditionally gain and phase margins are chosen to yield a compromise between performance and stability. By using adaptive control high gain margins and high phase margins are not required in order to ensure loop stability. Therefore, higher performance control is possible.

Powervation has developed Auto-controlTM technology which brings true adaptive control to DC-DC conversion for the first time. The benefits of Auto-control such as improved robustness, maximum performance and ease of design are all made available through this technology.

Figure 5 illustrates the improved robustness compared to a fixed controller which is achieved automatically with Auto-controlTM.

Summary

As trends in power conversion move the industry towards power architectures which are smaller and more efficient, the requirement to intelligently manage the multiple power rails under these constraints of space and efficiency is driving the industry towards the adoption of digital power control and power management solutions. There is significant potential for the development of power control technologies which harness uniquely digital techniques in order to deliver improvements in power system design. Using traditional control techniques gain and phase margins are chosen to yield a compromise between performance and stability. By using Auto-controlTM, high gain margins and high phase margins are not required in order to ensure loop stability. Therefore, higher performance control can be achieved and unprecedented ease of use can be delivered as designers are freed from the burden of loop compensation.

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Ease of Implementation with Digital Techniques

Revolutionizes DC-DC converter design

The need for high power together with high availability for telecom and other demanding applications drives designers to adopt distributed power architectures that partition subsystems to spread the power load and accommodate redundant elements. Such systems typically comprise one or more ac-dc front-ends that isolate and convert utility power to an intermediate dc level. Each system board carries at least one intermediate bus converter (IBC) that isolates and down-converts this distribution voltage to a local level that suits down-conversion by point-of-load (PoL) regulators.

By Patrick Le Fèvre, Director Marketing & Communications, Ericsson Power Modules

The IBC is a crucial system element that is especially challenging to design. As well as tolerating worst-case voltage step-down ratios of 8:1 or more, the cascade nature of multiple high-current step-down stages makes conversion efficiency and power density crucially important factors. Minimizing conversion losses directly translates into lower energy costs within the converter and the cooling system, while the ability to handle high-power loads reduces the number of IBCs that are required. In addition, today's intelligent power-management strategies increasingly demand that the IBC has full system connectivity using the industry-standard PMBus protocols. Figure 1 shows an example board with two current-sharing IBCs and three PoLs running under the supervision of a power-system host via a PMBus interface.

The combination of electrical perfor-

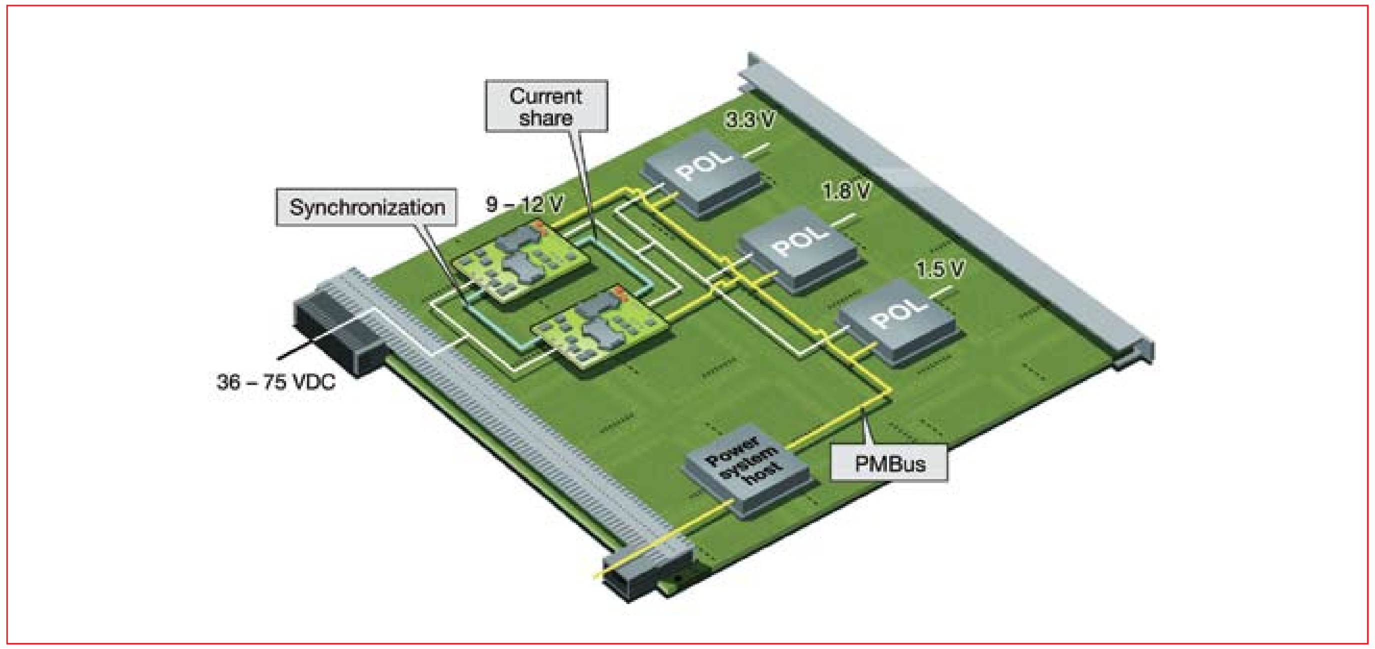

Figure1: Example board with two current-sharing IBCs and three PoLs.

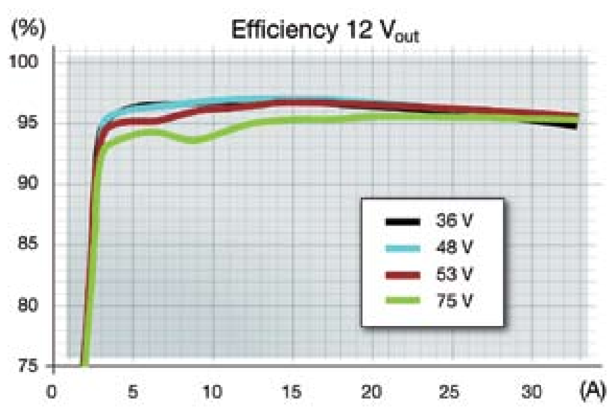

Figure 2: Comparing the BMR453 with its analog predecessor, the digital converter achieves 96% or better efficiency from about 3A upwards for a 48V input, and reduces losses at high input voltages by more than 2%.

mance and embedded control requirements led Ericsson to consider a digital approach to power-converter design that culminated in its BMR453 quarter-brick module. By comparison with the company's PKM4304BI module that uses analogue control, substituting a digital core results in as much as 2% efficiency improvement and approximately 5% greater power-handling capacity. Moreover, the BMR453's digital core includes a PMBus interface that integrates an unprecedented level of control and monitoring functions.

Adaptive operation maximizes efficiency

A prime advantage that a digital core offers is the ability to adapt to input-line and output-load conditions to optimize converter efficiency across the widest possible range of operating conditions. For instance, a digital core can vary the dead-time between a buck converter's upper and lower MOSFETs switching; by comparison, passive components establish the timing constants within an analog control loop, which are then fixed. While it is essential to prevent the upper and lower MOSFETs simultaneously conducting, it's also desirable to minimize the dead-time period during which the lower MOSFET is off and a relatively inefficient Schottky freewheeling diode conducts. Some literature claims as much as 5% efficiency improvement due to this adaptive ability, but with highly-developed converters such as the PKM4304BI, Ericsson's experience is that 1% – 1.5% is more realistic.

The BMR453's full-bridge converter uses four n-channel MOSFETs to switch the primary winding of a centre-tapped transformer that determines the basic step-down factor and provides 1.5 kV of galvanic isolation to meet EN60950 requirements - see figure 3.

The control block continuously varies the duty cycle of the pulse-width-modulation (PWM) stream that controls the MOSFET drivers to maintain constant output voltage. The core of the control block is a digital synchronous buck converter IC that achieves 175 psec resolution at switching frequencies of up to 1MHz. A set of constants determines the response of a proportional-integral-derivative (PID) filter that compensates the control loop - see figure 4.

This process is the digital equivalent of setting poles and zeros using capacitors and resistors in an analogue converter. Crucially however, Ericsson's firmware can adjust the digital constants on-the-fly to compensate for varying line and load conditions—and unlike analog components, digital values do not drift with time and temperature. In addition to controlling the dynamics of inner-loop operation and performing housekeeping duties, the firmware also allows the end-user control of key parameters such as output voltage, which can range between 8.1 – 13.2V. One application is to optimize conversion efficiency for the IBC and the PoLs that follow.

At the transformer's secondary, six n-channel MOSFETs perform synchronous rectification. Their gate drivers operate in inverting mode to avoid pulling down the output rail during converter initialization if a pre-bias voltage is present. The default switching frequency is 140kHz, which minimizes gate-charge losses and eases filter design - a simple external LC filter enables the converter to meet the class-B requirements of EN 55022, CISPR 22, and FCC part 15J. Clock synchronization logic allows users to lock the switching frequency to an external reference, or to ensure

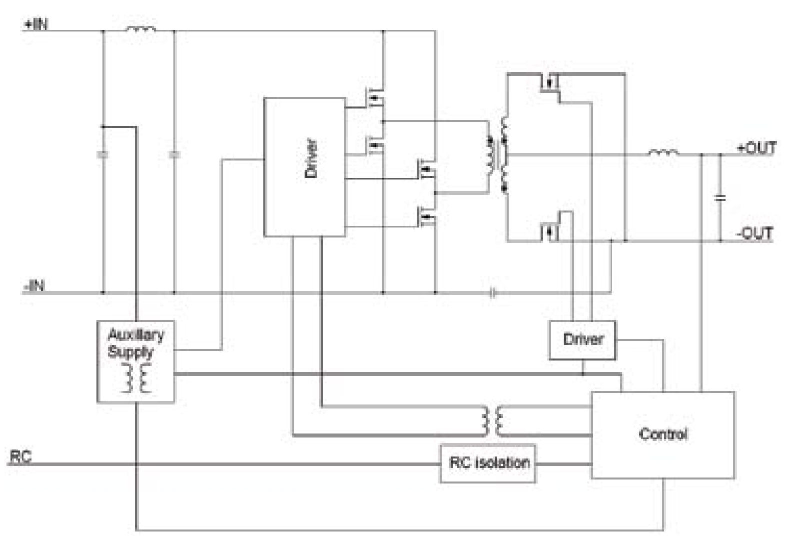

Figure 3: The underlying topology that achieves these results consists of a full-bridge converter, where two pairs of MOSFETs hard-switch the primary winding of a centre-tapped transformer.

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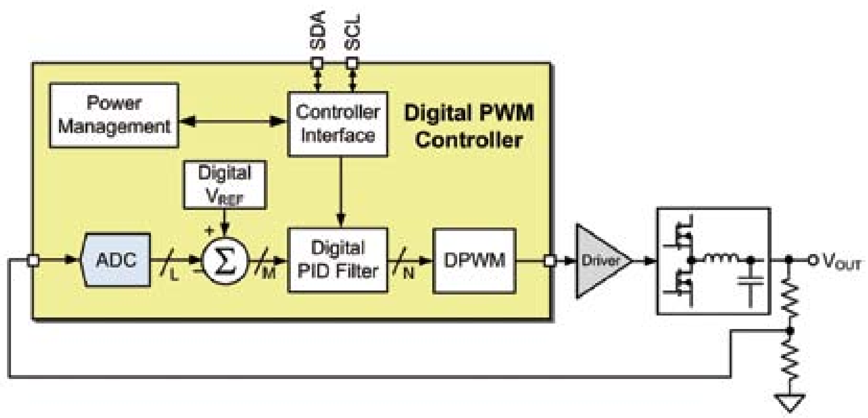

Figure 4: A set of constants determines the response of a proportional-integral-derivative (PID) filter that compensates the control loops.

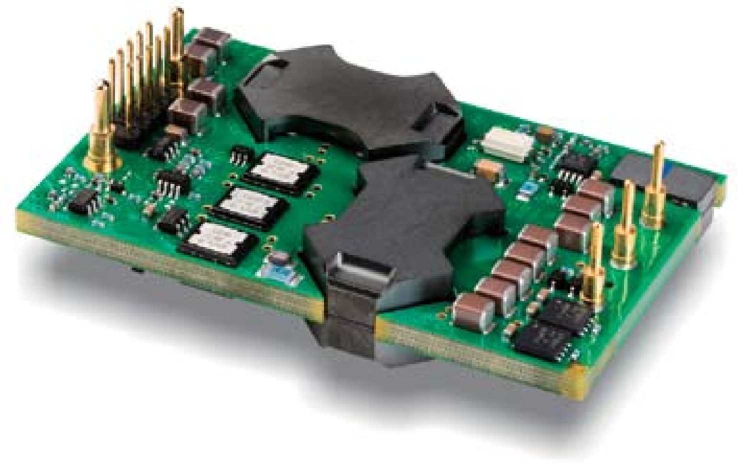

Figure 5: Innovative through-board mounting helps facilitate the converter's quarter-brick format.

that multiple converters operate at exactly the same frequency. Users can also adjust the switching frequency via PMBus commands within a useful range of about ±10kHz. These features ease filtering in some situations.

Secondary-side control tightens regulation

One major architectural difference between the BMR453 and the analogue PKM4304BI is the relocation of the control circuitry to the secondary side. This strategy requires precise secondary-to-primary side gate-driver signal control across an isolation barrier, together with a primary-side auxiliary supply for the driver stage. The transformer that couples drive-control signals is a proprietary design that uses a trifilar winding to minimize leakage inductance. Low-capacitance diodes peak-rectify these control signals prior to amplification by the high-side gate-drivers. A flyback circuit that includes its own start-up logic, power switch, and under/over-voltage lock-out functions forms the auxiliary supply. These changes tighten the +4%, -9% voltage regulation that's typical of competing analogue converters to ±2% with no degradation to noise or transient response.

Numerous additional design features help the BMR453 achieve its electrical performance while assuring a calculated mean-time-to-failure period of 1.1 million hours. For example, the transformer and output-filter inductors are proprietary planar designs that maximize magnetic flux to constrain their footprints to approximately 23.0x15.3x9.7mm. As figure 5 shows, these parts utilize through-board mounting to help facilitate the converter's quarter-brick format.

Also, the converter dispenses with failure-prone electrolytics in favour of chip capacitors, while the twelve-layer, 3-mm thick PCB carries extensive copper areas with thermal vias and micro-vias aiding heat dispersal. A baseplate option is available to maximise thermal conductivity.

Ease-of-use is paramount

By slashing component count, digital control lowers cost-of-ownership while supporting traditional analogue functions such as remote sensing and protection mechanisms. In addition, the BMR453 has an active current sharing facility that ensures equal load-current distribution between modules operating in parallel, making it easy to implement load-sharing or redundancy schemes—no OR-ing diodes or MOSFETs are necessary, greatly improving efficiency in parallel operation. Furthermore, digital supervision and control makes it possible to enable and disable paralleled converters to maximize conversion efficiency for loads that one converter can supply

But from the user's viewpoint, the digital core's major advantage is easy integration with digital power-management schemes that require additional support circuitry when using an analog converter. Compatible with any standard two-wire I2C or SMBus hardware, the BMR453's PMBus interface allows users to set numerous operating characteristics, including soft-start ramp times and voltage margining thresholds. A system controller can interrogate the module to extract a wealth of data such as input and output voltages, output current, internal junction temperatures, switching frequency, and duty cycle. For evaluation and development, Ericsson's CMM software provides a graphical user interface that allows users to "see inside" the running converter. An evaluation kit is available with a board, operating manual, a CD that includes the GUI, and cabling.

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Designing for High Efficiency

Selecting the right topology for energy-saving power supplies

Initiatives to reduce energy wastage by electronic systems are forcing designers of single-phase AC input power supplies to use newer power supply technologies. For higher power levels, these initiatives call for efficiency levels of 87% and above. Traditional power supply topologies such as the standard flyback and the two-switch forward do not support these high efficiency levels and are gradually being replaced by soft-switching, resonant and quasi-resonant topologies.

By Jon Harper, Market Development Manager, Power Conversion & Industrial Systems, Fairchild Semiconductor Europe

Principle of Operation

Figure 1 shows the voltage and current waveforms seen on the switches used in three different topologies: the quasi-resonant flyback topology, the LLC resonant topology and the asymmetric half-bridge topology which uses soft-switching techniques.

All three topologies use different techniques to reduce the turn-on losses of the MOSFETs. The turn on losses are given by:

$$P_{TurnOnLoss} = \frac{1}{2} V_{DS} I_D \cdot t_{ON} \cdot f_{SW} + \frac{1}{2} C_{OSSeff} V_{DS}{}^2 \cdot f_{SW}$$

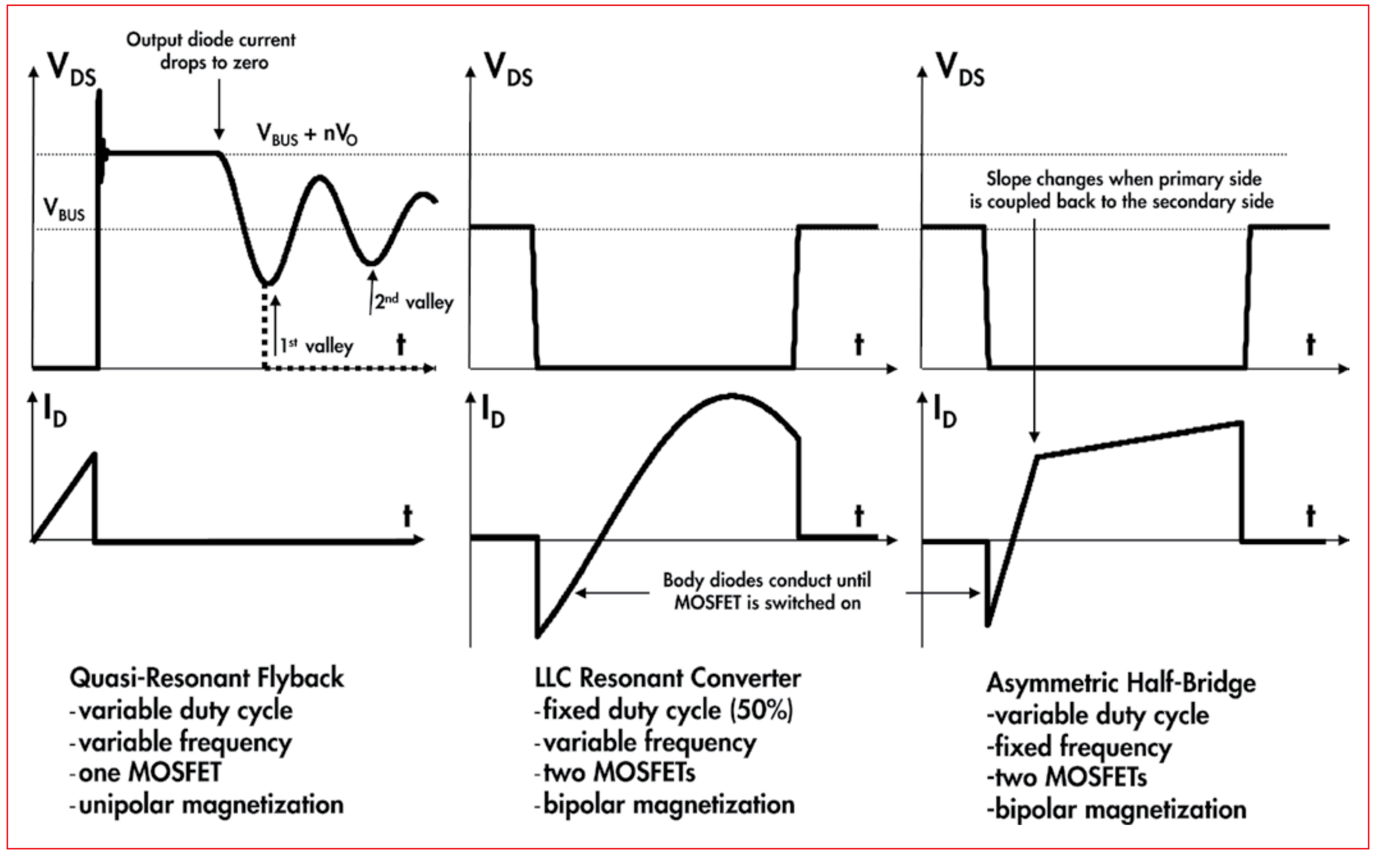

Figure 1: Comparison of quasi-resonant, LLC and asymmetric half-bridge topologies.

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where ID is the drain current immediately after turn on, VDS is the voltage across the switch, COSSeff is the effective value of the output capacitance including stray capacitance effects, tON is the turn-on time and fSW is the switching frequency.

Figure 1 shows that the MOSFET in the quasi-resonant topology will have a zero drain current immediately after turn on, as the converter operates in discontinuous conduction mode. The switching losses are therefore determined by the voltage at the turn on time and the switching frequency. The quasi-resonant converter turns on the MOSFET at one of the minima in the drain voltage to reduce switching losses. This means that the frequency of switching is not constant: at lighter loads the first minimum on the drain voltage will come earlier. In older designs which always switched on the first minimum, the efficiency suffered at light loads as the switching frequency increased, offsetting the benefit of switching on at a lower voltage. In Fairchild Semiconductor's e-Series™ quasi-resonant power switches, the controller waits for a minimum time (therefore setting an upper limit on the frequency) and then turns on the MOSFET at the next minimum.

The other topologies use zero voltage switching. In this case, the voltage VDS in the above equation is reduced from the bus voltage, typically around 400V, to around 1V. This effectively removes the turn on switching losses. Zero voltage switching is achieved by forcing a current to flow through the MOSFET in a reverse direction through the body diode, then turning on the MOSFET. The voltage drop of the diode is typically around 1V.

Resonant converters achieve zero voltage switching by generating a sinusoidal current waveform which lags the phase of the voltage waveform. This is achieved by applying a square wave voltage to a resonant network. The fundamental frequency component of the voltage forces a sinusoidal current to flow (the higher order components can generally be ignored). Above resonance, the current lags the voltage, permitting zero voltage switching. The output of the resonant network is rectified to provide a DC output voltage. The most popular resonant network consists of a transformer with a specific magnetizing inductance, an additional inductor and a capacitor, hence the name LLC.

Asymmetric half-bridge converters achieve zero voltage switching by using a soft-switching technique. Here the voltage generated by the bridge is a rectangular waveform with a duty cycle of well under 50%. A coupling capacitor is required to remove the DC component before applying this voltage to a transformer, and additionally serves as an energy storage element. When both MOSFETs are switched off, the energy in the leakage inductance of the transformer forces the voltage on the half-bridge to the opposite polarity. This voltage swing is ultimately clamped by the relevant MOSFET body diode, which suddenly takes on the primary current.

Selection criteria

These energy optimization efforts result in excellent efficiency. A quasi-resonant converter design can achieve over 88% efficiency for a 75W/24V power supply. With synchronous rectification, requiring an additional analog controller and a PFC front end it is possible to increase this to over 90% efficiency at 90W/19V. Higher efficiencies can be achieved by the LLC resonant and asymmetric half-bridge converters at this power level, but they are more expensive to implement. Quasi-resonant converters are therefore generally used up to this power range. The e-Series range of integrated power switches is effective for applications ranging from small 1W auxiliary power supplies, through 30W set-top box power supplies right up to 50W industrial power supplies. Above this power level, the use of the FAN6300 quasi-resonant controller with external MOSFET is recommended. This brings in the extra flexibility of handling unusually high system input voltages, or optimizing cost versus efficiency by being able to select a wide range of external MOSFETs.

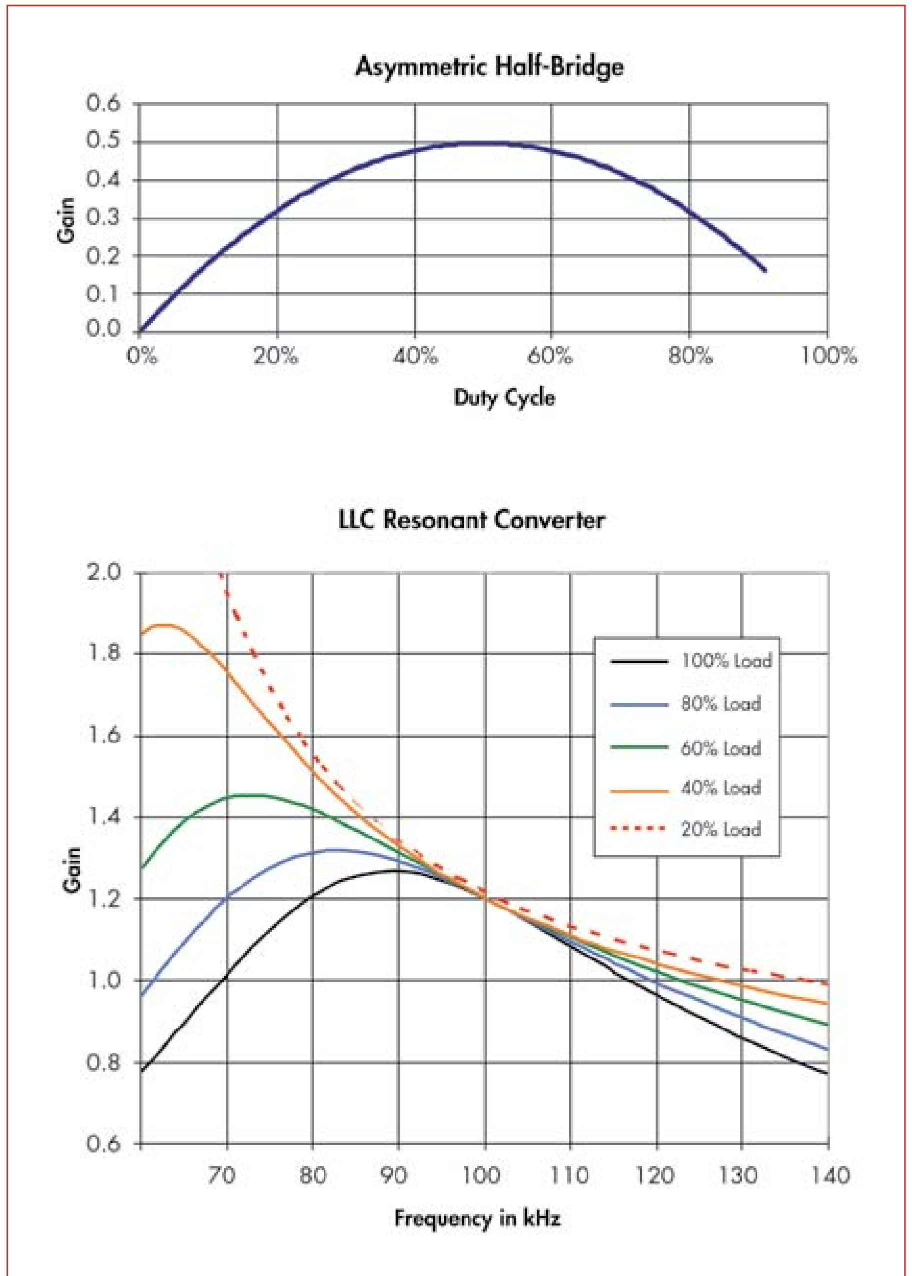

Figure 2: Gain curves of asymmetric half-bridge and LLC converters.

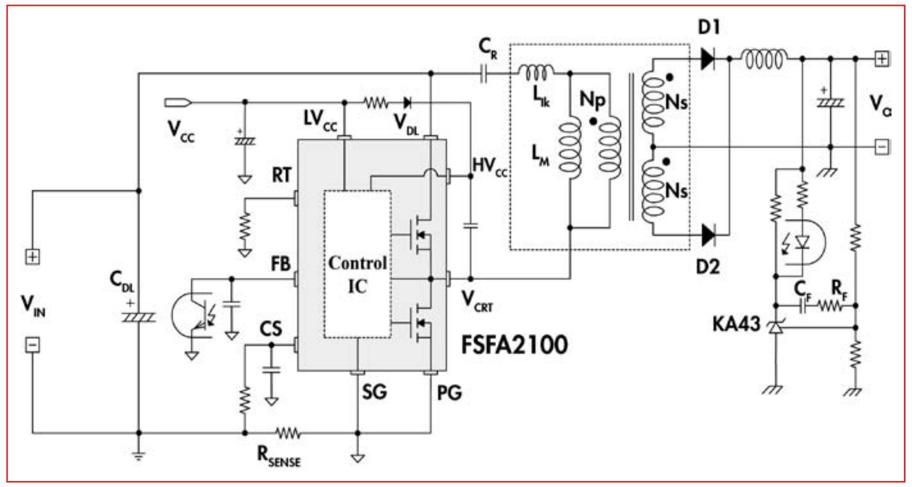

Figure 3: Asymmetric half-bridge converter based on the FSFA2100.

The quasi-resonant flyback uses one low side MOSFET, while the other topologies require two MOSFETs in a half-bridge structure. This makes the quasi-resonant flyback the most cost effective topology at lower power levels. At higher power levels, the transformer size increases which reduces both efficiency and power density. At this stage the two zero-voltage-switching topologies can be considered.

Four factors influence the design: the input voltage range, the output voltage, the ease of implementing synchronous rectification and the implementation of the leakage inductance.

Figure 2 compares the gain curves of the two topologies. For illustration, let us assume we need to support input voltages of 110V and 220V. For the asymmetric half-bridge, this is not a problem. We can set the operating conditions such that the gain is 0.2 for 220V and 0.4 for 110V. The efficiency would be worse at 220V as the magnetizing DC current increases as the duty cycle decreases. For the LLC resonant converter, the maximum gain is 1.2 noting how the full load curve is close to resonance. A gain of 0.6 would result in a very high frequency, resulting in poor system performance. In conclusion, an LLC converter is not suitable for wide range operation. With external adjustment of the leakage inductance, it is possible to operate it for the European input range, at the cost of higher magnetizing currents. It works best with a PFC stage in front. While an asymmetric half-bridge benefits from having a PFC stage on its input, it is possible to operate the circuit over a wide voltage input range.

For output voltages above 24V, an LLC resonant converter is recommended. The high output diode voltage stresses on the asymmetric half-bridge worsen efficiency because diodes with higher voltage ratings have higher forward voltages. Below 24V, the asymmetric half-bridge converter is recommended. The LLC converter has a far higher ripple current on the output capacitors, which increases with lower output voltages, resulting in a more expensive, bulky solution.

Synchronous rectification is possible for both topologies. It is very simple to implement for the asymmetric half-bridge (Fairchild Application Note AN-4153). For the LLC controller, a special analog circuit is needed to detect the current flow in the MOSFETs, the technique being simpler if the switching frequency is limited to the second resonant frequency (100kHz in Figure 2).

Finally, both designs rely on the leakage inductance of the transformer: in the LLC converter to control the gain curve (Figure 2) and for the asymmetric half-bridge to ensure soft-switching at light loads. For most applications we recommend using two separate inductors for this purpose. The leakage inductance is a poorly controlled parameter of a transformer. Additionally, the implementation of an unusual leakage inductance requires a non-standard coil former, increasing cost. Finally, for the asymmetric half-bridge, the resonant switching speed is at least ten times the switching frequency, resulting in higher losses if a standard transformer is used. In conclusion it is recommended to use a second inductor using normal ferrite for an LLC converter, and one using high frequency ferrite for an asymmetric half-bridge converter.

Figure 3 shows the circuit diagram for an asymmetric half-bridge converter. The circuit diagram is very similar to that of an LLC resonant converter, except that an LLC resonant converter does not require an output inductor and that the controller needs to be set up for frequency rather than PWM control.

The efficiency of a 192W/24V asymmetric half-bridge converter is around 93%. The 360W/12V current doubler version in AN-4153 also has a full load efficiency of over 93% between 20% and 100% of rated load.

The efficiency of LLC resonant converters are around 93% for 200W/48V power supplies, including the PFC front end. With synchronous rectification it is possible to raise the efficiency into the range 95%-96% for this power level.

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Power Factor Correction Techniques

MCU based digital feedback loop control

Power supplies in large systems that have input power of over 1KW typically use PFC for various reasons. Recent advances in PFC include interleaving of two out-of-phase circuits to gain many system level advantages. Enough has been discussed about the advantages of interleaved PFC; in this article we will focus on a comparison of the analog approach to the digital approach.

By Vipin Bothra, Application Manager and Robert Ortmanns, Application Engineer, STMicroelectronics.

The interleaving of PFC converters using analog controllers requires very sophisticated ICs that are dedicated for this purpose because of multiple loops within the system. A system based on analog controllers is forced to achieve a balance between complexity of the system and flexibility for adoption to various application needs. On the other hand, using an MCU to manage the feedback loop and management of peripheral functions provides utmost flexibility with only a slight increase in complexity.

Digital approach has two different meanings. One is the management of peripheral functions, which is commonly referred to as “digital management”, and the other is feedback loop control, which is called “digital control.” Digital control compared to analog control (of a feedback loop) does not really offer huge advantages; it is the combination of a digital control loop with digital management that creates a value that is more than a complete analog system.

MCU-based converters can measure and report the input power. The same input power measurement data can also be used internally to alter and optimize output voltage and switching frequency. Hence, with MCU-based converters, efficiency is optimized to the highest level and the efficiency curve can be flattened. Also, when demand for power is less than a certain threshold, one or more phases can be shut down to improve low load efficiency.

The cost of power components such as magnetics, MOSFETs and diodes, in higher power SMPS, is significantly higher compared to the cost of controllers. Hence, any saving in power components is easily paid off even if it requires higher cost in control components. Design for short circuit, power-up and power-down sequencing sometimes stresses power components beyond their normal operating level leading to the over-design of such components. With the help of the fuzzy logic of MCUs, it is very easy to implement timing and controls to minimize this over-design and reduce the overall cost of the system.

An MCU-based system also allows management of other functions in the SMPS that are beyond the realm of PFC, such as inrush current control and communication with the external world. A simple and cost-effective inrush current control can be implemented by using a resistor to limit the inrush current at start-up and then jumping the resistor out by means of a relay. A thermistor in contact with the resistor can be used to detect relay failures and prevent false startups of the circuit.

One or more thermistors in contact with major power components can be used to sense internal temperatures of the system which can then be reported to the external world. Moreover, the same information can be used to implement a precise fan speed control system by means of a simple lookup table. With digital control it is very easy to set boundary conditions to set operating limits for the converter and reduce waste of over designing in the system for taking care of abnormal operating conditions. An MCU-based system also reduces variations in the control module from one platform to another platform, compared with their analog counterparts, reducing engineering development time of future projects.

A functional block diagram of a typical interleaved PFC circuit with 2 phases based on ST’s STM32F103 MCU is shown in figure 1.

Output of the system is a gate drive signal for the MOSFETs of the two phases of the interleaved converter. Inputs to the system, from the external world, are Voltage reference (V_{ref}), Output voltage (V_{out}), and AC input voltage (AC in). Internally generated inputs to the digital

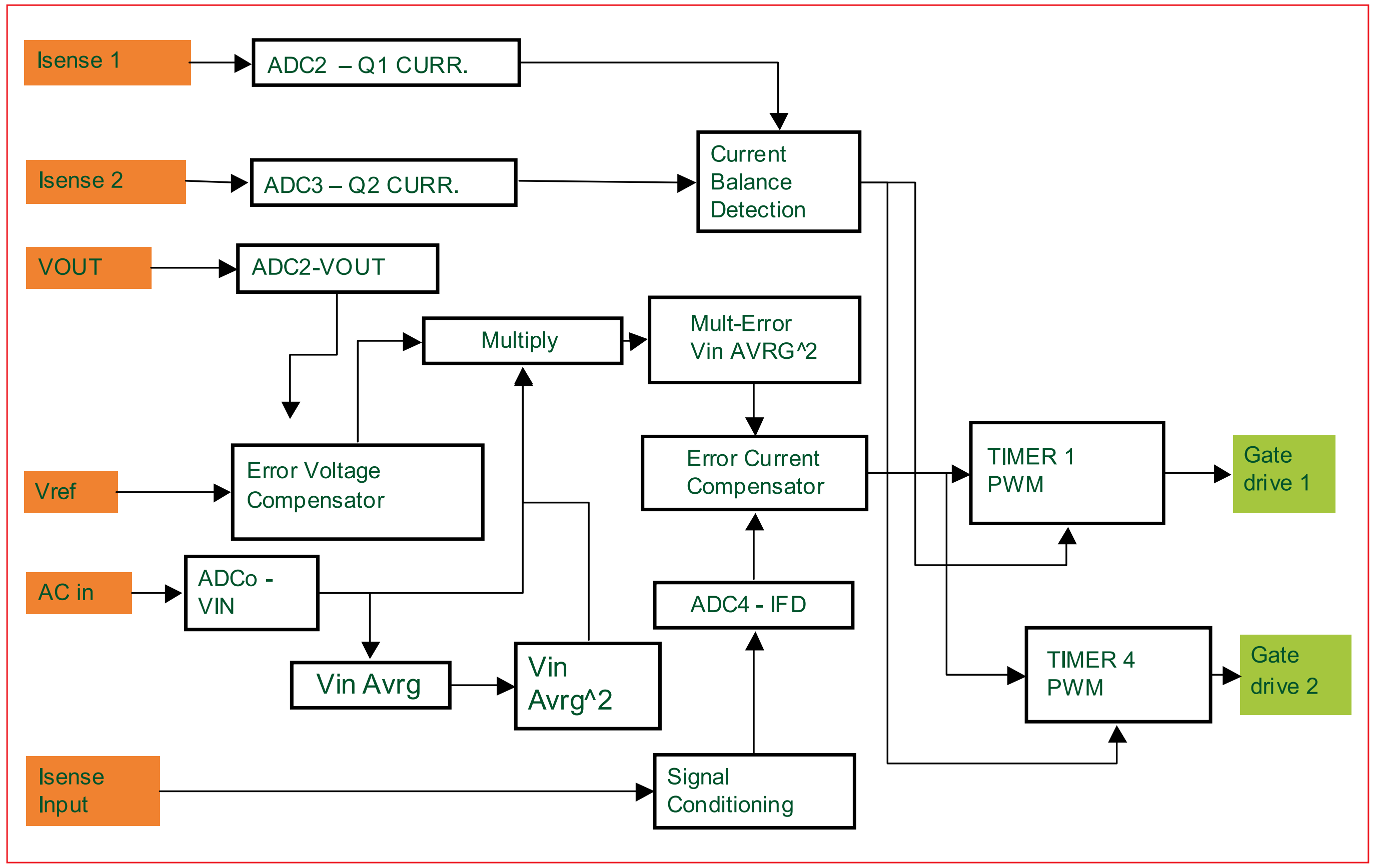

Figure 1: Functional block diagram.

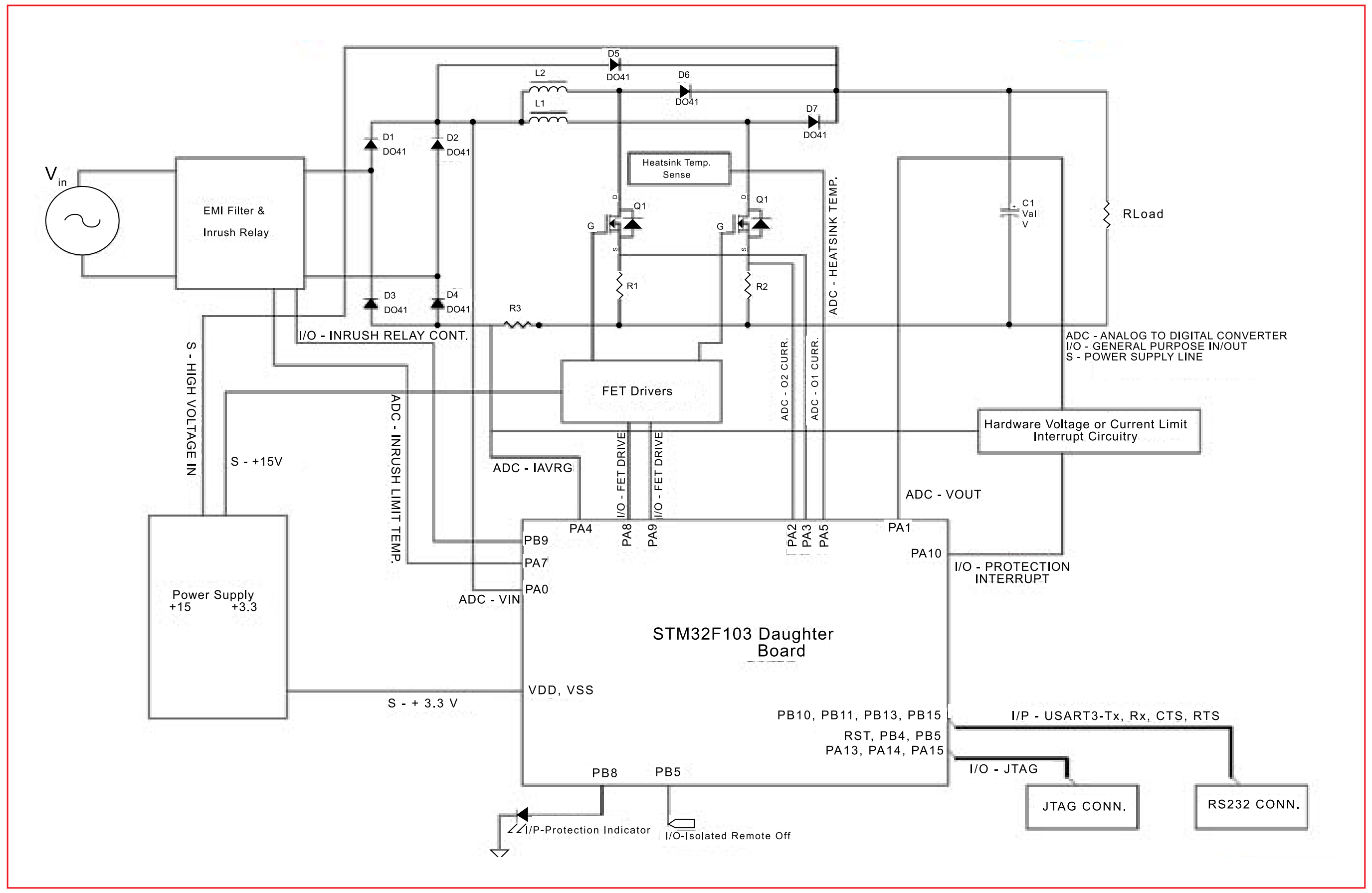

Figure 2: Component level block diagram.

control loop are Input AC current (Isense input), Instantaneous current of phase 1 (Isense 1), and Instantaneous current of phase 2 (Isense 2).

The block diagram shows the three critical inputs used in the control blocks of the PFC circuit. These three inputs include voltage on ADC0, the boost output voltage on ADC2, and the current feedback signal on ADC4. The measured input voltage is used in two control functions: the first one is used as one of the inputs of the multiply calculation that along with the error term is used to shape the current waveform. The second one is used to determine the average input voltage used in figuring the maximum allowable current so that the maximum allowable power can be kept constant as the input voltage range changes. The output voltage is sensed by an ADC and compared to a numerical constant in the code. Based on that, an error term is calculated and multiplied with the instantaneous input voltage to shape the current waveform to match the input voltage wave form. By further dividing this by the square of the average input voltage, a current reference (Iref in the diagram) is established and is used to program the current compensator. The current compensator uses the last critical input, which is the current feedback level converted on ADC4. Implemented as a PID loop, the current compensator uses the Iref level as the set point and the ADC4 level as the process variable. The output of the loop programs the duty cycle of the MOSFET switches via peripheral timers one and four.

The inputs ADC2 and ADC3 measure the currents flowing in the boost MOSFETs of the two phases. With both converters being fed from the same voltage source, having equal value inductors and driven with the same value duty cycles, the average currents in the two phases share the output current almost equally. The measured values are compared relative to each other and if there is a large difference between the two currents, indicating trouble, the outputs are shut down and an error is reported via the communications link.

A test board based on ST's STM32F103 was designed to run at the 100W power level, 100 KHz switching frequency, with universal input range, and an output voltage of 400V. Because the timers of the STM32 can be triggered from one to the next with a precise time offset, it is possible to do interleaving, with as many phases as needed, limited by the number of timers on the device. Our testing showed good efficiency even with the overhead of start-up power regulators needed to boot up the MCU first. Based on the design value of power components, including boost capacitor, we see a significant cost saving at a typical power of 1000W.

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Economic and Ecological Energy Prevails

Reported by Cliff Keys, Editor-in-Chief, PSDE

Will the momentum of 'going green' be maintained in the financial downturn? This surely will be the 'litmus test' for commitment. During my recent visit to APEC in Washington DC, I saw that although the financial crisis is certainly real and painful, the commitment to the development of higher efficiency products and systems, many utilizing digital power techniques, in our industry remained reassuringly strong.

Reuters recently reported that the credit crunch is making an impact on smaller European green energy projects, but cash-rich utilities and the larger lending institutions will continue to get deals done, green power experts say. The European Wind Energy Association (EWEA) attributes the main problem for the smaller developers to the short-term freeze on lending, adding that the credit crunch could lead to consolidation in the sector.

A ring of giant wind turbines connected by underwater cables is a central part of the European Commission's plan for bolstering energy security and curbing unreliable imports of fossil fuels. The

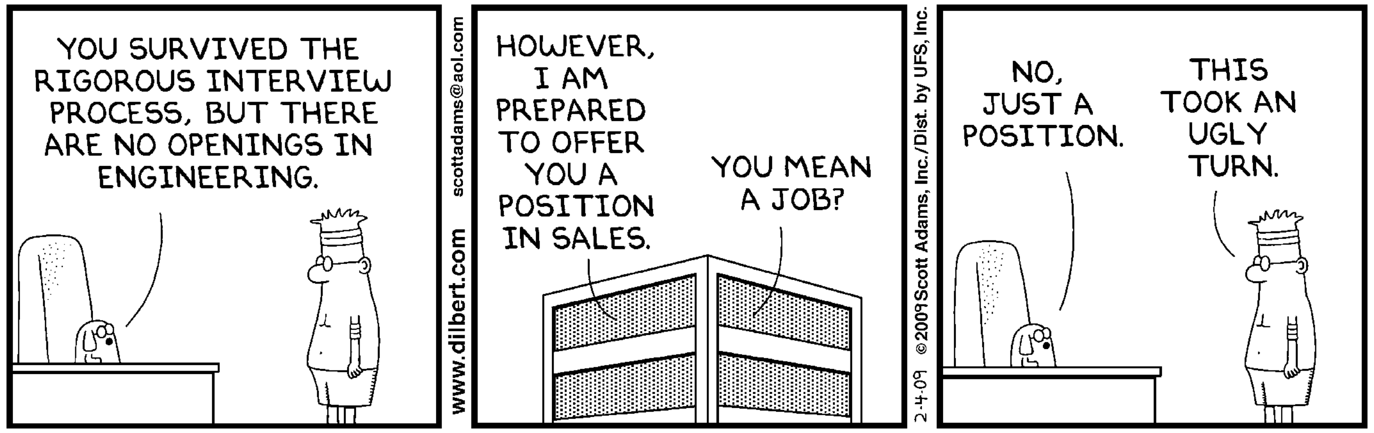
European Council recently endorsed the European Commission's Strategic Energy Review (SER), which contained its commitment for a blueprint for a North Sea grid. The Council described work on this offshore grid as a priority action. EWEA considers the development of offshore wind and its integration into the electricity network key to achieving the EU's 20% renewables targets by 2020.

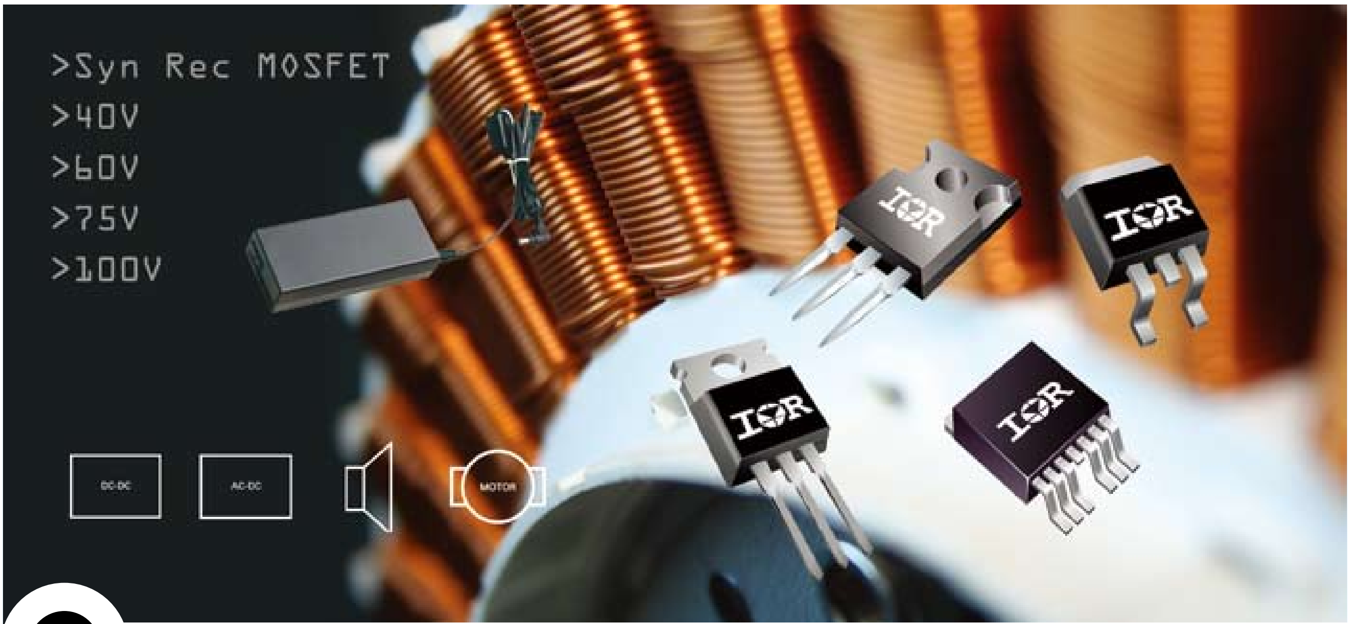
There is currently 1,471 MW of installed offshore wind capacity, all of it in European waters. There is enough wind blowing over the seas to supply all of our power, yet without an offshore grid and increased interconnector capacity to transport power to consumers, this vast potential will remain untapped.

EWEA Chief Executive Christian Kjaer said. "In its conclusions, Council confirms the EU's need to turn to an indigenous energy supply and to 'promote renewables and tackle barriers to energy from renewable sources'. These actions are essential for increasing our use of renewables and so boosting the EU's energy security, reducing our fuel imports, avoiding CO_2 emissions and carbon costs, creating jobs and putting money to work at home rather than spending it on importing fuel from unstable regions abroad."

In its conclusions, the Council also proposed that the Commission prepare a Sustainable Energy Financing Initiative with the European Investment Bank to mobilise large-scale funding from capital markets for investments in renewable energies.

www.powersystemsdesign.com/greenpage.htm





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IRFB3206PBF	60	210	3.0	120	TO-220
IRFS3206PBF	60	210	3.0	120	D²PAK
IRFP3206PBF	60	200	3.0	120	TO-247
IRFB3306PBF	60	160	4.2	85	TO-220
IRFP3306PBF	60	160	4.2	85	TO-247
IRFP4368PBF	75	350	1.8	380	TO-247
IRFB3077PBF	75	210	3.3	160	TO-220
IRFP3077PBF	75	200	3.3	160	TO-247
IRF2907ZS-7PPBF	75	180	3.8	170	D²PAK-7
IRFS3207ZPBF	75	170	4.1	120	D²PAK
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IRFP4110PBF	100	180	4.5	150	TO-247
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IRFP4310ZPBF	100	134	6.0	120	TO-247

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