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PSDE Green Power
ENERGY EFFICIENCY

Special Report – Digital Power

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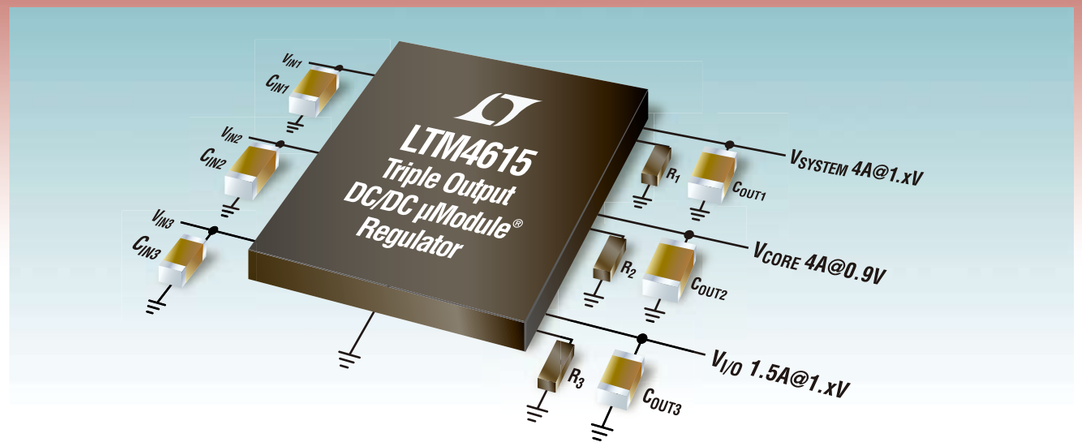
Multiple Output µModule Regulators



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Multiple Output Step-Down DC/DC µModule Regulator Family

Triple	Output Current Configurations		V_{IN} Range	V_{OUT} Range	LGA (Land Grid Array) Package Size (mm)
Low Voltage: ≤5.5V_{IN}					
LTM®4615	→ 4A → 4A → 1.5A	→ 8A → 1.5A	V_{IN1}: 2.375V to 5.5V V_{IN2}: 2.375V to 5.5V V_{IN3}: 1.14V to 3.5V	V_{OUT1}: 0.8V to 5V V_{OUT2}: 0.8V to 5V V_{OUT3}: 0.4V to 2.6V	15 x 15 x 2.8
Dual					
LTM4614	→ 4A → 4A	→ 8A Also see LTM4608A	V_{IN1}: 2.375V to 5.5V V_{IN2}: 2.375V to 5.5V	V_{OUT1}: 0.8V to 5V V_{OUT2}: 0.8V to 5V	
LTM4616	→ 8A → 8A	→ 16A	V_{IN1}: 2.7V to 5.5V V_{IN2}: 2.7V to 5.5V	V_{OUT1}: 0.6V to 5V V_{OUT2}: 0.6V to 5V	
High Voltage: ≤26.5V_{IN}					
LTM4619	→ 4A → 4A	→ 8A Also see LTM4601A	V_{IN1}: 4.5V to 26.5V V_{IN2}: 4.5V to 26.5V	V_{OUT1}: 0.8V to 5V V_{OUT2}: 0.8V to 5V	

Info & Free Samples

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LINEAR TECHNOLOGY

Power Systems Design EUROPE


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The Digital Power Marriage

With the upwardly spiraling desire for energy efficiency in almost all things, we are now seeing a revolution in technology and products hitting the market. This is not restricted to the super-spins of existing products or the tuning of power systems to hit the sweet spots, but radical changes are quietly taking place. It wasn't so long ago that the fiercely contested 'intrusion' of digital power techniques almost looked like succeeding. Some of the more traditional, although highly experienced and talented, analog engineers rejected the idea that digital power techniques could add value to power systems arguing that analog techniques could do everything the industry required and at that time, they were probably right. But not any more.

Most now agree that the contribution already made by the skillful implementation of digital power has helped the engineer or system designer in automating design processes such as loop compensation that earlier could take an engineer a considerable amount of highly skilled work.

At the APEC conference held recently in Palm Springs, California, there was great evidence of this. I visited as many companies as I could in the three day trade fair attached to the conference and was impressed by the volume and quality of new products and by the utilization of new technology on display. The economy may still be down, but innovation is certainly up, alive and flourishing. For those who could not get to this wonderful event, I am pulling together a roundup of the reports I made from my meetings which will be posted on our website.

Coilcraft, Rogers Corporation and Power Systems Design hosted a golf day for participants which proved to be a hugely popular event and will, by popular request, be repeated at APEC 2011 in Fort Worth, Dallas, Texas.

But in our expanding industry, it's not just the products that make a success. Firms are nurtured, guided and driven by their management. I talked to several senior managers at the conference and it was good to see that creativity and good strategic thinking is alive and well. There will always be the spreadsheet folks, but the ones that can motivate their people forward in a common direction that will bring success have to be experienced leaders. This does mean the desk-thumping or super-dynamic egotist, most likely quite the opposite. It is very easy to see the companies that have developed a culture of genuine belief and trust in their leadership, a common goal and a passion to succeed. You can see it in their eyes.

I hope everyone is receiving the Power Systems Design 'PowerSurge' online news blast. We are running this on a weekly basis with content to keep our readers up-to-date in real-time on the latest products, industry news and my industry interviews.

I hope you enjoy the issue, keep the valuable feedback coming and check out our fun strip, Dilbert, at the back of the magazine.

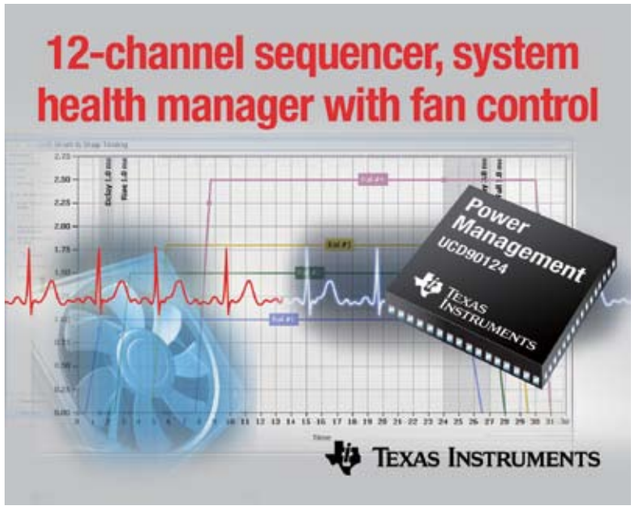
All the best!

Cliff Keys.

Editor-in-Chief, PSDE
Cliff.Keys@powersystemsdesign.com

TI's Intuitive Fusion Digital Power™

Designer tool speeds configuration



Texas Instruments has launched the industry's first 12-channel sequencer and system health manager with fan control and multiphase PWM clock generator. The UCD90124 integrates system power management and system thermal management into one device, which reduces board space and eases design, while providing highly intelligent system health monitoring. The sequencer features power supply margining and comprehensive non-volatile error logging, allowing customers to diagnose power supply failures in their systems.

The UCD90124 is a 12-rail PMBus/I2C addressable power-supply sequencer and system-health monitor. The device integrates a 12-bit ADC for monitoring up to 13 power-supply voltage, current, or temperature inputs. Twenty-six GPIO pins can be used for power supply enables, power-on reset signals, external interrupts, cascading, or other system functions. Twelve of these pins offer PWM functionality. Using these pins, the UCD90124 offers support for fan control, margining, and general-purpose PWM functions.

Fan-control signals can be sent using PMBus commands or generated from one of two built-in fan-control algorithms. PWM outputs combined with temperature and fan-speed measurements provide a complete fan-control solution for up to four independent fans.

TI's easy-to-use Fusion Digital Power Designer Graphical User Interface (GUI) allows the designer to configure the UCD90124 via a PMBusTM/I2C interface. The free, downloadable tool simplifies the development process and speeds time-to-market by allowing the designer to configure all device parameters in minutes.

To download the Fusion Digital Power Designer see: www.ti.com/fdpd-pr.

Key features and benefits of the UCD90124

- Sequence and monitor up to 12 power supplies while simultaneously margining up to 10 rails.
- Manage power and monitor and control up to four fans with a single device.
- The UCD90124 has a built-in temperature control algorithm that automatically adjusts fan speed based on five configurable temperature zones. Alternatively, designers can use their own temperature control algorithm running on an external host and communicate desired fan speed via I²C commands. This level of intelligent system thermal management helps reduce audible system noise and extend the operating life of the fans.
- The auto-calibrate function automatically determines the turn on, turn off and maximum duty cycle for the fan, which allows the designer to think in terms of operating speed and also accounts for environmental variables in fan speed.
- The UCD90124 can generate up to eight clocks with configurable frequencies from 15.259kHz to 125MHz and phase shift from 0 to 360 degrees, easing synchronization of switch-mode power supplies.

Find out more about TI's power management supervisor and sequencer portfolio at the links below:

- TI's complete supervisor and sequencer portfolio: www.ti.com/supervisors-pr
- TI's complete power management portfolio: www.ti.com/power-pr
- TI's supervisor and sequencer E2E online community: www.ti.com/svsforum-pr

www.ti.com

AEG Delivers Expanded Portfolio

I had the opportunity to talk with Laszlo Lakatos-Hayward, CTO of AEG Power Solutions (AEG PS) about the company's proud history and achievement throughout the world. He gave me an insight into where the company is now and its powerful strategic direction going forward.

Reported by Cliff Keys, Editor-in-Chief, PSDE

AEG Power Solutions is already a renowned and well respected company for its work in providing European and Asian-Pacific markets with a wide range of AC & DC power systems. The company has launched an intensive program to raise its US portfolio to match this achievement. The company, formerly Saft Power Systems, has a distinguished heritage in North America going back over half a century, with many of its systems operating reliably over decades of continuous trouble free service.

As part of its planned expansion, AEG Power Solutions is expanding its corporate operations in the US, specifically in Dallas, Texas and Markham, Ontario.

The company is headquartered in Amsterdam, Netherlands, with offices established in Texas in 2001. Its products are spread over the whole gamut of Industrial and commercial organisations.

With the growing need for energy efficiency around the world AEG PS is adapting its offerings accordingly. Renewable energy solutions will be a big focus in the North American market where the company is establishing design and applications engineering teams to strengthen its service capability. Solar systems solutions for the commercial and industrial sectors are to be found at the top of the company's target list.

Laszlo explained to me further that in today's business environment, most firms are acutely aware of the energy and pollution issues and are now taking responsibility in holding themselves accountable for their carbon footprint and the contribution they can make to humanity as well as to their bottom line. With the huge worldwide awareness and sensitivity to these issues, it is a great time to join the good guys, improve

operating efficiency and profit - and get a boost in image.

But achieving all this takes a highly concerted and determined effort. In North America as well as in Europe, there is a shortage of good, well qualified engineers. Over the past decade or so, the number of students enrolling into engineering degree courses in universities has declined. The more appealing Law and Medical courses have attracted more students simply because of the elevated prestige and earning capability they offer in the real world.

But all this is in a state of flux now. Engineering excellence is the route to energy efficiency and engineering creativity and wisdom in its generation and application will improve our lives. History will certainly show that the contribution to the quality of our environment as well as that of future generations will be greatly enhanced by the pioneering achievements by skilful and talented engineers, led by visionary and committed management.

AEG PS is, quite rightly, proud of its heritage and in its reputation for the very highest standards in quality and service. With these exemplary attributes the company is confident in the planned global expansion and especially in delivering its capability and system solution strategy to the North American market. It is currently seeking out and recruiting the very best in engineering talent.

For the world of engineering, this is indeed good news. The power engineer now has the noblest of tasks that will certainly over time elevate the status and hopefully remuneration of the role.

AEG Power Solutions also looks forward to enabling smart grid applications with its intelligent and rugged power electronic solutions. The company can now offer to its customers a complete power electronic system solution for the newly expanded North American market that provides the same high level of innovation and reliability that AEG PS has been providing to European and Asia-Pacific markets for decades.

Its combines the engineering advancements made by Saft Power Systems and AEG that led to a product quality that is hard to match in the power systems industry. Taking into account the commitment to invest in smart grid technology, now ongoing in North America, the timing is perfect for AEG PS to provide the enabling power electronic technology required for this energy transformation.

AEG Power Systems is ideally placed to become the ideal partner for the Industry and Commerce sector's total energy needs.

www.aegpowersolutions.com

Digital Conversion & Control ICs Power Strong Growth

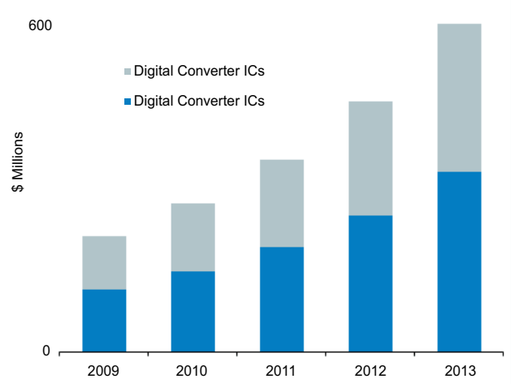
By Ryan Sanderson, Market Research Analyst, Power & Energy Group, IMS Research

With many power IC suppliers reporting strong results for the fourth quarter of 2009 and underlying drivers looking much more positive, it seems safe to assume the market is now well into the recovery phase. Inevitably though, some areas of the power IC have a much more positive future projected than others. Of all the power IC markets IMS Research studies, digital power management and conversion ICs are forecast to see one of the highest growth rates over the next few years.

Latest projections from IMS Research's report on power management and driver ICs predict revenues of digital controller and conversion ICs are set to more than double over the next four years to around $600 million. Despite this, opportunities for digital controllers and converters today are still very much limited to infrastructure and datacom equipment such as high-end servers, routers and base stations, though penetration of digital controllers in power supplies is growing. Digital converters are targeted at applications where space is very constrained and where customers are willing to pay a premium to get the smallest footprint; however prices of digital solutions are now becoming much more competitive as economies of scale are realised.

So are more competitive prices of digital converters and controllers driving adoption? In essence the answer is yes, though a fair comparison can't be made on a chip-to-chip basis and there are other factors to consider. Digital controllers and converter ICs still have a much higher average selling price than their analog equivalents, but the overall system cost of an application can still be reduced using a digital solution. This partly comes down to the typical integration model, whereby if you can provide all of the power management functions in a single IC and save board space, you can produce a cheaper solution. However, there are other benefits of a digital solution which can lower costs further down the line. Improving energy efficiency is often easily achievable using a digital approach, and using integrated diagnostic feedback in order to assess and solve problems faster, can minimize system downtime which is particularly important in datacom/infrastructure applications.

The World Market for Digital Power management & Conversion ICs



Source: IMS Research

The downturn may also act in favour of digital power vendors, as customers have had a chance to step back and assess their designs and consider using digital solutions whilst demand was reduced. Growth is, however, also attributable to the increased time digital power vendors have spent working very closely with end-equipment manufacturers to provide the most effective designs.

IMS Research predicts that these factors will fuel adoption in applications outside of the server/datacom markets such as high-end consumer driving penetration of digital products to more than 10% of the total controller and regulator market by 2014. There is therefore a substantial threat to analog technology in the future. The analog industry powerhouses are already preparing themselves however, developing and releasing products in the digital market space. IMS Research believes that there will be more mainstream analog suppliers following suit in the next few years. The transition to digital solutions is now inevitable and is set to gain momentum. Digital power remains an extremely interesting market – and we will be watching it very closely!

www.imsresearch.com

Power Supply Development Diary

Part I

This article begins a new series in which Dr. Ridley shows the multiple testing and revision steps needed to get a power supply from concept to a fully-working prototype.

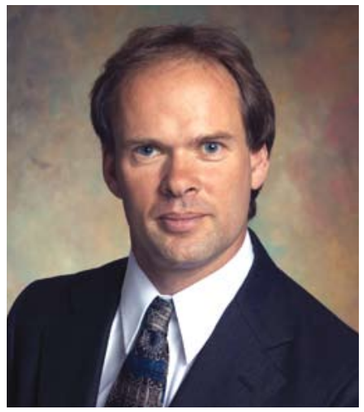
Power Supply Development Time

Whenever I look at doing an off-line power supply development, I have a formula for calculating how long it will take. I lay out each step of the process, and estimate the maximum amount of time that each step might take. Then I double the result. After this, I am normally hard-pressed to finish on time.

Why does this happen? It's because there are always unforeseen events that can drastically slow down the development process. After many years of working with switching power supplies, you learn that parts seldom behave as expected. When designing for a rugged environment of line variations, surges, short-circuits, and temperature variations, you can never be certain how long it will take.

It is hard to explain to those new to power supply design exactly what can go wrong. It is also hard to explain to management why the project schedule estimate is so long, and why we might need three or more board turns to get such a "simple" circuit right. Part of the reason for this difficulty is that when solving the problems of a power supply, we are often in a hurry and rarely have time to fully document the steps involved in fixing problems. Later on, we forget exactly what happened during that accumulated time.

I am guilty of following the same process. When working on a consulting design, or on a design for my own



projects, the main objective is to be done as quickly as possible. Recently, however, I had a unique opportunity to take time to fully document the process from a power supply that was already laid out and ready for testing, to achieving full power. In following this process, I encountered many events I had seen in the past, and never documented.

Power Supply Requirements

The specification for the power supply was as follows:

1.Output 1 – 35 VDC @ 10A isolated

2.Output 2 – 35 VDC @ 10 A isolated

3.Maximum power 350 W (only one output fully loaded at a time, application is for audio.)

4.Input – 180 – 265 AC

5.Power Topology: Two-switch forward

6.Controller: Digital controller from TI

The project was launched for several purposes. Firstly, I needed a bulk supply for an audio product which is currently running from a linear supply. Secondly, I had a digital designer who was eager to work for me for four months to try and learn some real-world power supply design. I have watched the promise of digital for over 20 years now, and felt is was finally time to see whether it could really work in a real-world product. And finally, I have always recognized the two-switch forward as the most rugged topology available, but never actually built one from scratch. It was time to learn the details of the topology first hand.

The optimistic goal of the project was to finish in plenty of time so that a second converter with the same specifications could be built to run from the one digital controller. I didn't really expect this to happen in the given time frame, but it was kept as a goal. At the end of the project, I hoped to have a working prototype, learn a lot about digital controllers and their quirks, and to impart some knowledge on analog power design.

As is often the case in the power supply world, things didn't quite work out as planned. At the end of the four months, I found that I still couldn't program a digital controller (although I learned a lot), and a digital designer couldn't possibly learn enough about high-voltage analog design in such a short time. However, I learned a tremendous amount about our analog design process and why

it remains a challenge after so many years. The digital designer returned to the world of low-power offline work, and he learned more about his digital algorithms but not, unfortunately, what makes the analog world go round.

Separation of Power and Control

The first major lesson when working with a digital controller is that the layout needs are totally different from the needs of the analog power stage. The digital part of the board requires fine-pitch traces, and at least a four-layer board. On the other hand, the power stage requires heavy copper for high-current traces, large trace separation for voltage breakdown requirements, and plenty of allowance for thermal management, and bulky magnetics. And, as we shall see later in this series, you must be able to rework the power board manually to arrive at a well-designed converter in the shortest amount of time.

I always work with just two layers for power supplies. I like to be able to see all of the traces on the top and bottom sides to ensure proper spacing for all components. I also like to have the ability to move a trace if necessary, and relocate critical components without needing to layout a new circuit board.

In early development, the most practical thing to do is separate the controller and power stage into two boards with a connector between them. Digital control forces you to this approach. This is also an approach I have always taken for analog power development. A controller from one project is often very applicable for your next project, and can be taken as a partial pc board and interfaced with a new power stage. This can save a tremendous amount of time, and is easy to do if you have a clear delineation between power and control.

During the development of most power converters, the control and power stage delineation becomes blurred with more and more communication from one to the other. The addition of ground planes confuses the line even more. This can lead to multiple problems with noise.

Ground and other PCB planes should be completely separate between the control board and power board. This is naturally achieved when the two boards are built separately, as is recommended for the early stages of digital control. This proper separation of the power and control boards will be discussed in more detail in the next article of this design series.

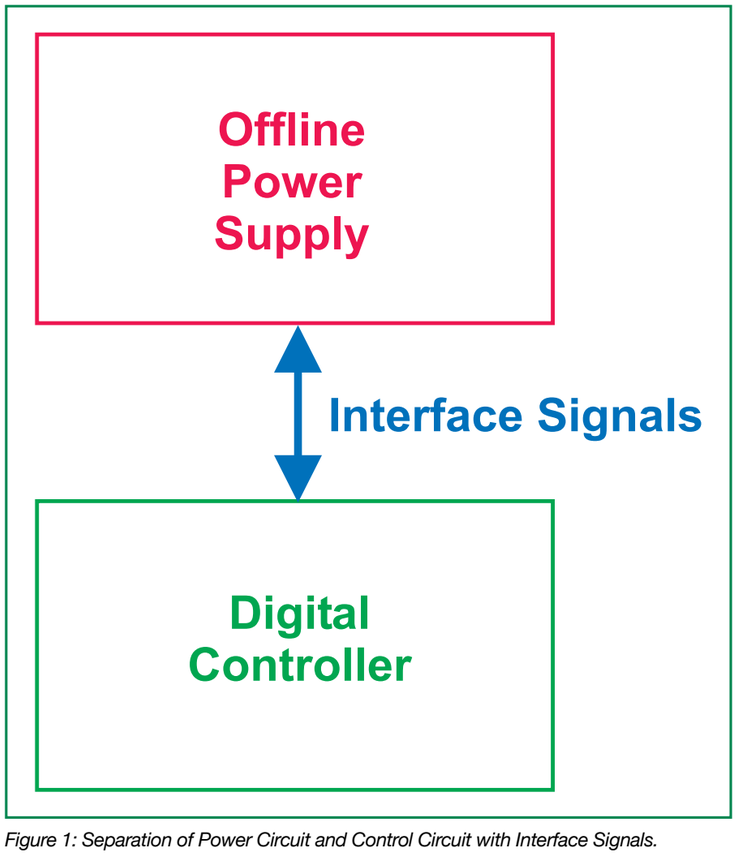


Figure 1: Separation of Power Circuit and Control Circuit with Interface Signals.

Full Schematic and Layout

The full schematic of the forward converter will be presented in the next article of this series. The power layout took about 1 month to complete, including the entry of all component footprints and placement of parts and traces. When working with existing parts databases, I usually expect this process to take me about two weeks. Less experienced designers can easily spend eight weeks on this process if starting from scratch.

The layout alone is a topic worthy of a complete series of articles. I won't go over that in full detail in this series, and will concentrate instead on the issues involved in completing the design after the first layout was complete.

Debugging the Power Stage

The question that has troubled me the most about digital control has been the issue of debugging. After many years of solving power supply problems where you must capture fleeting events and track them down through power stage and controller waveforms, I have always wondered how this can be done in conjunction with the development of software and digital controllers, which may also have bugs.

Finally, I think I have resolved "how" this must be done. The answer is simple – the power stage must be fully debugged with an analog controller before the digital control is implemented! This is not a comfortable answer for the advocates of digital control. You must go through a complete analog design first, and then implement the digital and software aspects. It's clear that the development time of this approach will be considerably longer than just analog control. So the digital control implementation must offer significant advantages to justify this extra time.

An important item I learned about the difference between analog and digital designers is the way they think about their circuits and components. There is a fundamental divide between the two. Digital controllers, and microprocessors in general, have millions of transistors in their circuits. They are all expected to work within their specs, and work perfectly. When the software is complete, there should be no surprises. Designers do not expect the individual transistor circuits to misbehave.

In the analog power stage, however, you learn to expect almost every aspect of the circuit to misbehave. Nothing is exactly as documented in the textbooks or datasheets.

This will be clearly illustrated in the following parts of this series. There are many steps involved in the process, most of which involve events not to be found in any book or datasheet. There were several categories of problems to be resolved:

1. Failed components
2. Misconnected components
3. Component values
4. Unexpected operation in regions outside of the component specifications.
5. Layout
6. High-frequency parasitics and noise
7. Snubbers and clamp circuits
8. Mechanical
9. Magnetics
10. Control stability

In all, in moving the converter from the initial board layout to a full power prototype, there were a total of 85 process steps. That does not include full characterization of the power stage and control optimization. The work is ongoing, when I have time to get back to the bench. I would expect in excess of 200 steps by the time the converter is done and ready for production.

For me, with 30 years experience, these steps moved very rapidly since I had seen many of the phenomena before. It took a total of approximately two weeks to implement them all. For the inexperienced designer, many of these steps can take days or weeks to solve. Quite often, the project can never be completed since the solutions are hard to find without experience.

Summary

The key points learned of the first stage of the project:

1. There must be a clean separation of power stage and controller, whether using analog or digital control.
2. A tremendous amount of analog experience is needed to implement a digital control system.
3. If you want your power supply to work with a digital controller, you must first debug it with an analog controller. You cannot take on both problems at once.
4. Resolving the power stage issues alone can be a very long process, and design experience is essential to expedite this.

In the next article of this series, I will begin describing the full schematic and the initial problems with the converter.

Gallium Nitride Hits the Market

Has silicon reached the end of the road?

I had the pleasure to talk with Alex Lidow, CEO of EPC, Efficient Power Conversion Corporation. Alex is a true veteran of the power business dedicating his life to the pursuance of energy efficiency. He told me about his new company and the amazing products it will bring to the marketplace.

Reported by Cliff Keys, Editor-in-Chief

I talked to Alex about the company's drive, mission and purpose. He gave me a clear response, "We enable industry to benefit from the most efficient energy conversion using superior semiconductor materials. EPC designs, develops, markets, and sells Gallium Nitride based power management devices".

When I asked about the background for this strategy, I was reminded that industry in general and power management in particular, is a large and growing market that is constantly in need of higher energy efficiency.

Silicon has now reached performance limits in power management and further improvements can only bring small incremental gains. Now the industry needs to go to the next level. Companies such as those running huge server farms to provide their services not only need to find a way of drastically cutting down on the losses that turn expensive and precious power into waste, they have to deliver ever higher levels of performance.

Gallium Nitride (GaN), which is grown on top of silicon, enables a game-changing price/performance ratio. This is a step-function improvement and not another incremental gain. These devices work like a power Mosfet, designers can get used to the design rules transferring their skills without having to relearn their craft. The advantages

Alex Lidow, CEO of EPC, Efficient Power Conversion Corporation

are clear. These devices can handle higher step down ratios in converters for instance. Not just an incremental gain, but by a hefty 10x in performance. As an example a laptop power supplies are normally fed by a 20V source. The required step down can be done in one single step with GaN to reach the processor voltage.

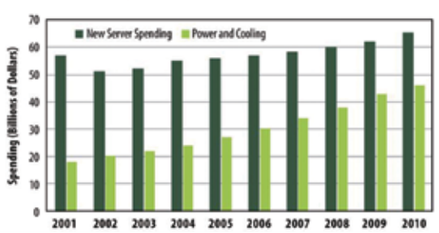
EPC's served available market of $7B is forecast to grow at a rate of 11.1% between 2009 and 2015. With aggressive pricing and a strong team in place, EPC intends to capture its fair share of the market.

In the now highly scrutinized Served Market, a dual processor server card consumes approximately 450W of power. Approximately 160W are consumed by power conversion. EPC's GaN technology can reduce total server power requirements by about 18% which could save $8.1B in annual power usage. Server power supplies using EPC's GaN transistors have power losses that are more than 50% less than the cloest silicon solution available.

But servers are by no means the end of the story. The market possibilities are almost without limit and here are just a few examples:

- Class D Audio can achieve unprecedented sound quality while lowering cost
- Laptops can reduce power consumption, save space, and lower cost
- Flat-screen TVs can incorporate 5.1 or 7.1 surround sound at a lower costs and with reduced space
- Cell phones can significantly in crease battery life and reduce costs

Power consumed by servers is almost as costly as the server itself



All this is not just theory though. These are real, fully supported products to revolutionize our industry. EPC's initial products are targeted at the Server, Switch, Hub, and Audio markets and will cover 90% of the existing power MOSFET market by the end of 2010.

Gallium Nitride technology from EPC can provide significant benefits to new designs with the smaller die sizes and lower on-resistance involved. As accepted by manufacturers the on-resistance ($R_{DS(ON)}$) for a given device area is a key determinant of product cost. The big groundswell of news in the media in the last few years regarding the attributes of Silicon Carbide devices has yet to gain the wide adoption predicted, probably due to the specialized fab requirements and resultant normally prohibitively high cost.

EPC's products have the same on-resistance and are significantly smaller than the best silicon parts available on the market.

EPC is a brand new company consisting of a management team that is the most experienced in the power industry. The company's focus on GaN concentrates the whole design support and manufacturing on what is for sure a disruptive technology.

The available market open to EPC is $7B and is forecast to grow at an annual rate of 11.1%. With a mature supply chain – EPC is using well established and respected players in semiconductor manufacturing – the future looks very bright indeed. The company has enormous capacity already in place and is well prepared for the predicted adoption as manufacturers take advantage of the differentiation that GaN enables.

This was a brief insight into what EPC are driving to achieve. It is not the full story and I am sure we'll be hearing more from this newly established company. According to Alex, Silicon has reached the end of the road.

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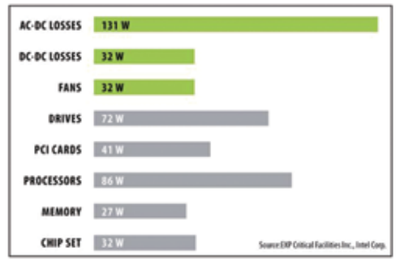
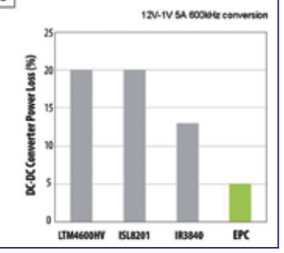
A dual processor server card consumes approximately 450W of power. Approximately 160 W are consumed by power conversion.

EPC's GaN technology can reduce total server power requirements by about 18%. This could save $8.1B in annual power usage



Lowest Power Losses

Server power supplies using EPC's GaN transistors have power losses that are more than 50% less than the closest silicon solution. This could save $8.1B per year in energy costs.



Gallium Nitride products reduce the considerable power loss experienced with conventional silicon solutions.

EPC's initial products are targeted at the Server, Switch, Hub, and Audio markets

$R_{DS(on)}$ mOhm	Voltage				
	40	60	100	150	200
7		EPC1005	EPC1001		
25	EPC1014			EPC1011	EPC1010
30		EPC1009	EPC1007		
100				EPC1013	EPC1012
Intro Dates	April 2009		September 2009	December 2009	
EPC #	1001 - 1005		1007 - 1009	1010 - 1014	

EPC's products will cover 90% of the existing power MOSFET market by the end of 2010

$R_{DS(on)}$ mOhm	Voltage						
	40	60	100	150	200	400	600
4	EPC1015						
7		EPC1005	EPC1001				
25	EPC1014			EPC1011	EPC1010		
30		EPC1009	EPC1007			EPC1017	
100				EPC1013	EPC1012		EPC1019
200						EPC1016	
500							EPC1018

GaN - A New Era Begins

Commercial introduction of GaN based power electronics

The initial commercial introduction of GaN based power conversion solutions by International Rectifier repre-sents the culmination of significant engineering efforts to resolve several fundamental barriers to achieving practical cost effective high performance packaged power devices.

By Michael A. Briere, ACOO Enterprises LLC, USA

Introduction

As has been previously discussed [1], significant advances in the performance/cost figures of merit (FOMs) for power devices (e.g. Rdson*cost or Ron*Qsw*cost) are required in order to improve the power delivery system FOM of efficiency*density/cost. The reduction of total system costs can be substantially enabled by intelligent power electronics which optimize performance/cost, in turn promoting the wide spread adoption of more efficient working loads, leading to a potential reduction in worldwide energy consumption by some 25%.

Over the last 3 decades significant engineering efforts have driven the improvement in the performance figure of merit of silicon based power devices by more than an order of magnitude. However, as this technology approaches maturity, it becomes increasingly expensive to achieve even modest improvements in the device FOM. It is estimated that less than a factor of two improvement will be economically feasible to achieve for 30 V FETs [3], with perhaps a factor of five possible for 600 – 1200V silicon IGBTs [4]. Necessary further advances in power device performance must be achieved through the use of alternative materials. One of the most promising alternatives to silicon is gal-lium nitride based power devices.

Even though the basic GaN HEMT transistor was first invented over 15 years ago by M. Asif Khan [5], significant development efforts on practical power devices using GaN-on-Si technology have been fairly recent, predominantly in the past 5-7 years. GaN based power devices are expected to improve rapidly over the next 10 to 20 years. In fact, it is expected that an order of magnitude in improvement in the key device performance FOMs will be achieved over the next 5 years.

Barriers to Commercialization

There have been however, several significant barriers to the commercialization of GaN based power devices. Chief amongst these is the cost of production. The production of power devices includes the costs of substrate, epitaxy, device fabrication, packaging, support electronics and development.

The viable economic based limit of about $3/cm^2 for substrate and epitaxy cost set by the power device marketplace is exceeded by all substrate choices except silicon wafers. Multi-wafer MOCVD tools provide the required through-put and cost of ownership.

Next to the cost of substrate and epitaxial layers, device fabrication costs are the most critical. In fact, currently, sub-strate diameters of at least 150mm are required to achieve widespread commercial viability for power device fabrica-tion. In addition, the device fabrication costs are only acceptable if high volume, high yielding standard (silicon compatible) semiconductor fabrication lines are used. Similarly, the volume necessary to support the broad power device market (10 million 150mm wafer equivalents per year) requires scalability in device manufacture provided most readily by existing silicon device fabrication facilities.

It is for these reasons that International Rectifier has developed its GaNpowIR technology platform using GaN-on Si hetero-epitaxy and device fabrication processing that can be performed in a standard modern silicon CMOS manufacturing line with little modification to equipment or process discipline. It is this approach that allows this technol-ogy platform to provide power devices with compellingly superior performance/cost FOMs compared to silicon which will promote widespread adoption.

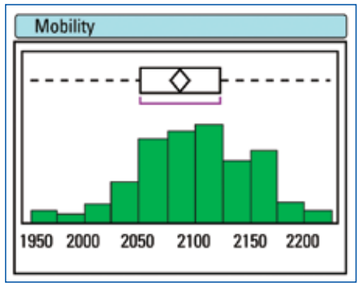


Figure 1: Measured Hall Mobility (cm^2/Vs) for GaNpowIR III-Nitride HEMT epitaxy.

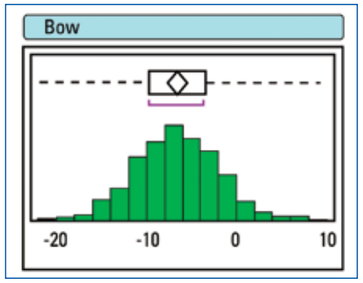


Figure 2: Measured wafer bow in microns after III-Nitride HEMT epitaxial deposition on 150mm silicon.

Initial GaNpowIR Device Focus

As has been previously reported [2], the initial GaNpowIR products from International Rectifier will be low voltage (30V) dc-dc power stage modules. This approach is different from many commercial efforts which focus on the obvious advantages of GaN based power devices at higher voltage ratings above 600V [3,6,7]. Though the distinct ad-vantage of low voltage GaN based HEMTs is not as obvious in terms of specific-on-resistance, it is important to note the it is the R(on)*Qsw FOM which is critical to many of the low voltage applications. In this regard, the GaN HEMTs are expected to achieve more than an order of magnitude improvement over state of the art silicon devices within the next 5 years [2]. Quantitatively, this means a R(on)*Qg device performance of less than 4 mohm*nC compared to next generation silicon FOM of 45 mohm*nC.

Barriers Overcome

One of the most fundamental challenges to the commercialization of GaN based power devices is the development of cost effective, high yielding, high throughput III-Nitride epitaxial processes on large diameter silicon wafers. It is well established that silicon is the substrate of choice for commercial GaN based power devices. The intrinsic mis-match in both lattice constant and thermal coefficient of expansion with the requisite III-Nitride epitaxial films causes threading dislocations, as well as significant macroscopic film stresses, which result in excessive wafer bow and plastic deformation (cracks) in the films. These issues have been addressed by engineering the proprietary epi-taxial film growth on standard thickness 150mm <111> silicon wafers to both eliminate most of the threading dislo-cations, resulting in 10^9cm^{-2}, predominately edge dislocations for 2µm thick films (comparable to similar thickness films grown on SiC), as well as compensating for the stresses due to thermal coefficient mismatches. These result in a high quality device layer, as demonstrated by the excellent electron Hall mobility of >2000cm^2/Vs achieved in the 2 dimensional electron gas formed at the interface between the thick GaN buffer layer and the overlying AlGaN bar-rier layer, as shown in Figure 1.

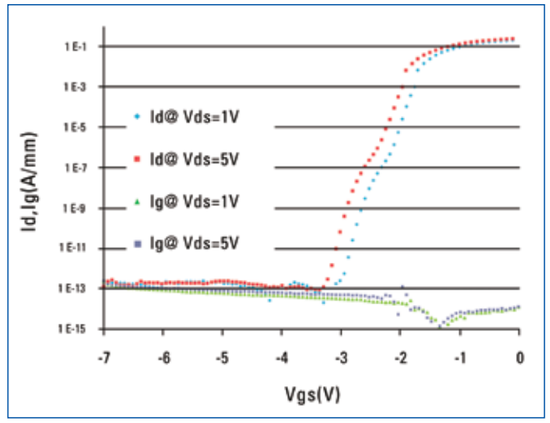


Figure 3: Measured Id normalized to gate width (850mm) as a function of Vgs for Vd= 1 and 5V, Lg=0.3µm.

In addition, the resulting wafer bow is well within the required limit for device fabrication of < 60µm, as shown in Figure 2 (bow in µm).

It should be noted that truly crack free material to within 0.5mm of the wafer edge are consistently produced by this process in manufacturing volume. Further, the occasional crack that is found

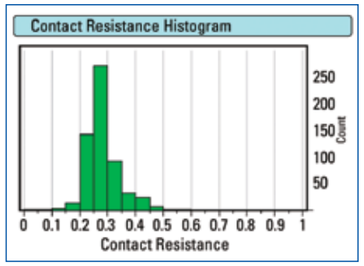


Figure 4: Contact resistance measured using standard transmission line technique in ohm-mm for initial GaNpowIR platform.

within 0.5mm of the wafer edge has been shown not to propagate during subsequent device fabrication.

Much of the reported constructions for GaN devices to date utilize Schottky gates and subsequently exhibit device leakage in operation of mA/mm of gate width. For a power device, which often has an effective gate width on the or-der of 1 meter, such gate leakage would result in an unacceptable power loss/heating. Similarly, the maximum oper-ating voltage has often been specified at reverse bias source-drain current densities of mA/mm of gate width. Another challenge, therefore, is the reduction of these leakage currents to less than 1uA/mm. This has been achieved through the combined use of a proprietary insulated gate construction and improved III-Nitride epitaxial film quality. This has resulted in gate and drain-source leakages of <10pA/mm, as shown in Figure 3. The resulting ratio of Ion/Ioff of 10^{12} is substantially better than reported elsewhere for GaN based devices and even exceeds that of comparable sili-con based power devices.

Figure 5: Topside view of a flip chip GaNpowIR device.

Though the principle challenge to develop high voltage GaN on Si based devices which substantially exceed the per-formance of silicon based devices appears met to a large degree [e.g. 3,6,7], substantial challenges existed to produce low voltage devices to exceed silicon device performance. One such challenge is the reduction and control of source-drain contact resistance. Though this component to the Rdson of a high voltage device (e.g. > 300V) is negligibly small, it can dominate the FOM for low voltage devices (e.g. <100V). In fact, in order to be competitive, the contact resistance for low voltage devices must approach 1micro-ohm cm^2 or <0.35ohm mm. This has been achieved in a cost effective, high volume manner within the IR GaNpowIR technology platform, without the use of gold metallurgy, as shown in Figure 4.

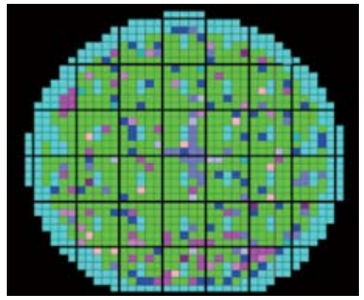


Figure 6: Wafer yield map for production GaNpowIR fabrication process for 15mm^2 die (green = good die).

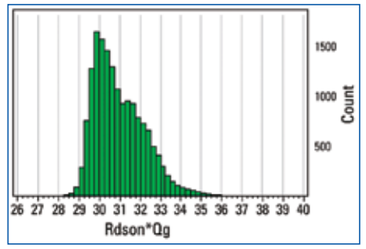


*Figure 7: Measured Ron*Qg product for initial GaNpowIR technology platform.*

Another challenge for the realization of commercially viable low voltage GaN devices is the effective conduction of the source-drain current from the internal to the external device terminals. This has been accomplished through the use of planarized multi-level metallization, common to silicon ULSI device fabrication. In addition, the use of a proprietary solderable front metallurgy (SFM) has been used to produce a flip-chip die, eliminating wire bonding and minimizing other package related parasitics. Figure 5 shows such a flip chip GaN power device.

Device yield is an important challenge for the commercialization of large area power devices. Unlike RF devices, with active areas < 1mm^2, power devices often have active areas >10mm^2. It is economically imperative that yields > 80% are commonly achieved for such large devices. Figure 6 shows a wafer map of device yield for 15mm^2 devices, demonstrating the necessary level of process maturity for commercialization.

It is interesting to note that much of the remaining yield loss is unrelated to the properties of the III-Nitride epitaxial layers.

Figure 7 shows the distribution for the RQ FOM for a typical wafer batch of low voltage product die, demonstrating that the target of 30mohm*nC for this first generation technology platform has been achieved [2].

Finally, the stability of device in-circuit performance is a prerequisite to commercialization. Figure 8 shows the Rdson stability for a random selection of low voltage GaN power devices.

As can be seen, the stability of this critical FOM is excellent under accelerated conditions for >4000 hrs. In fact, over 1,000,000 device hrs of reliability testing has shown performance in line with silicon based device specifications. Tests have included, gate stress, reverse bias stress, constant current (2x specification), temperature humidity bias, package testing for MSL and temperature cycling, high temperature operating life and intermittent operating life tests.

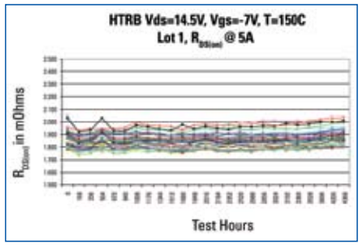


Figure 8: Measured stability of Ron for large (2.5 meter Wg, Lg=0.3µm) power device under constant reverse bias stress for >4000 hrs.

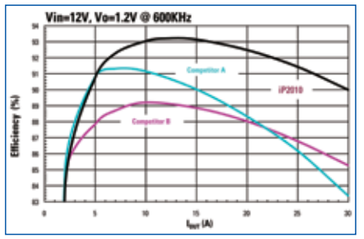


Figure 9: Measured power conversion efficiency for initial GaNpowIR product, iP2010, a 12V_{in} to 1.2V_{out} POL converter power stage operating at 600kHz compared to two silicon based alternatives.

First Product

In order to realize the potential of the GaN based power devices, it is necessary to develop companion technologies such as high speed drivers, low duty cycle capable PWM controllers and low parasitic packaging [1]. For example, the transition times (and dead time) are on the order of 1ns [1], making it necessary to provide intelligent and fast deadtime control for the drivers in order to realize the optimal performance made possible by the GaN power device.

The first product release to production on the IR GaNpowIR technology platform is a 30A capable 12V buck converter power stage product. It incorporates the control and synchronous rectifying switches together with the intelligent gate driver in a low parasitic LGA package. Figure 9 shows the measured power conversion efficiency for this first generation GaN product compared to competitive silicon based solutions.

Here it can be seen that the GaN based power devices provide more than a 3% improved conversion efficiency over state of the art silicon FETs. In adition, by enabling this high efficiency at 600kHz, this GaN based power solution enables the use of all ceramic capacitors in the power converter, thereby enhancing system reliability.

As has been previously discussed [1] further improvements in LV GaN based power devices (e.g. RQ<5) will allow for truly revolutionary performance of efficient (85 to 90%) single stage power conversion (e.g. 12V to 1.2V) at >50MHz frequencies, eliminating much of the output filter components, significantly reducing costs, and shrinking the converter size by more than a factor of ten. Perhaps more importantly, this higher frequency operation enables the more intimate positioning of the conversion stage with the electronic load. This eliminates a significant amount of parasitic power losses in the output filter and PCB/ package. The resulting simultaneous improvement in power conversion density, efficiency and cost represents the true value of GaN based power device development for LV ap-plications, as it is unknown how to achieve such performance/cost using silicon based devices.

Perhaps even more importantly, the IR GaNpowIR technology platform represents a cost effective platform for true power integrated circuits, incorporating a range of voltage capable devices with best in class performance. This will allow system on a chip integration, such as complete AC-LV DC conversion and high power monolithic inverters for motor drives and power distribution. More than the replacement of silicon discrete devices with GaN based devices, this platform opens a new era for integrated power conversion.

Conclusion

The first commercially viable GaN based power device platform has been introduced, overcoming several significant barriers, particularly cost. First products focus on low voltage applications, resolving technical issues particular to these class of devices. General solutions of high quality, crack free III-Nitride epitaxy in a production environment as well as low contact resistance and low device leakage levels have been achieved. Excellent device stability as well as commercially acceptable device yields have also been achieved.

More than the replacement of silicon discrete devices with GaN based devices, this platform opens a new era for in-tegrated power conversion.

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EMC Filters

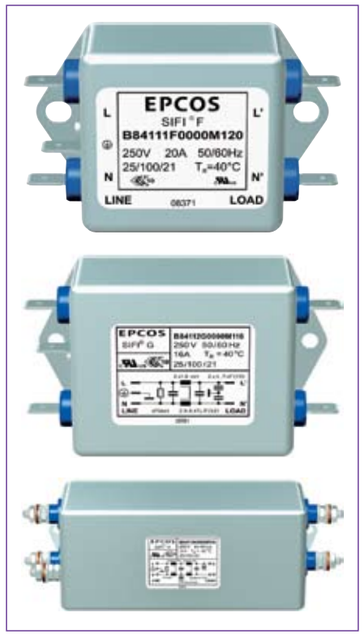
New applications through lower leakage current

The SIFI series of 2-line filters has proved itself in numerous applications over many years. The new SIFI® generation with reduced leakage current is now also suitable for medical engineering applications.

By Volker Scharrer, Product Marketing Manager EMC Filters, EPCOS

Increasing numbers of electronic appliances and their interaction mean that suitable EMC filters are more important today than ever before. They are needed not only to observe the EMC equipment limits (radiated interference) but also to ensure reliable operation of the equipment even under harsh conditions. This also means protection from interference coming from other equipment and from the power line (perturbations). Reliable EMC protection contributes significantly to assuring machine availability, thus also providing a useful sales argument for manufacturers of systems, machines and installations.

The 2-line filters of the new SIFI® series from EPCOS are now used successfully in the most diverse applications. Thanks to innovative materials, the dimensions of the new SIFI series have been reduced still further compared to their predecessor types while retaining the same current capability. In addition, constructional improvements have also led to cost reductions.



Modular concept

EPCOS currently offers three new SIFI families: SIFI-F (B84111F), SIFI-G (B84112G) and SIFI-H (B84113H). They were developed as standard modular filters for single phase systems (2-lines) with various attenuation characteristics.

Fig. 1 is designed as a selection guide so that EMC filters with correctly dimensioned properties and thus the most cost-effective solution can be found in a few steps.

All filters of the three SIFI families are now also available with a reduced leakage current of only 0.002mA, making them suited for applications in medical technology.

The new SIFI families differ mainly in their attenuation properties and dimensions. SIFI-F (B84111F) has the smallest dimensions and covers the range of normal requirements on interference suppression. Even a limited available space is usually sufficient for SIFI-F, as the package of the 10A version including terminals and attachment clips requires a footprint of only 60 x 60mm^2.

In the case of higher requirements on attenuation properties, SIFI-G (B84112G) is recommended. Especially at frequencies below 1MHz, it offers an improved asymmetrical insertion loss compared with SIFI-F. Fig. 2 shows the asymmetrical insertion loss (common mode) of the 3-A versions of SIFI-F (B84111FB30), SIFI-G (B84112GB30) and SIFI-H (B84113HB30) as a function of the frequency.

Asymmetrical insertion loss for 3A versions of SIFI-F, SIFI-G and SIFI-H, as a function of the frequency.

If the insertion loss of SIFI-G is not sufficient, then SIFI-H (B84113H) should be used. This is a two-stage filter with the highest insertion loss. Starting from as low as about 0.1 MHz up to about 50 MHz it reliably reduces the conducted symmetrical and asymmetrical interference voltages. Depending on the interference source, this allows high requirements such as the limits of class C1 to EN 61800-3 (2004) for conducted disturbance voltages to be observed even for strong sources of interference.

When the suitable SIFI family (F, G or H) has been selected on the basis of the attenuation requirements, the leakage current must be considered. All new SIFI filters are available in both standard and medical versions. The standard version has, depending on the type, a leakage current in the range from 0.5 to 3.5mA. In the version for medical technology, the leakage current was limited to a maximum of 0.002mA, as strict limits apply in this sector.

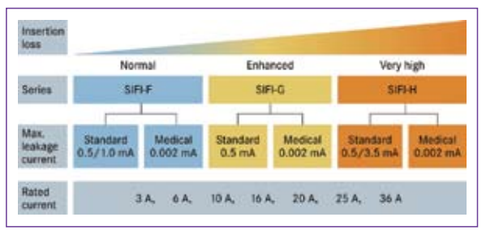


Figure 1: Selection guide for EMC filters of the SIFI family.

When selecting the rated current, filters are available from 3A to 36A. The rated voltage is 250V DC/AC for all types. Optimization of the components used allows the maximum ambient temperature to be increased to 100° C, corresponding to climate category 25/100/21 to IEC 60068-1. This leads to a reduced and thus improved current derating at higher temperatures. The complete SIFI range has naturally been approved to UL, cUL and ENEC. This facilitates the approval of the end product for the North American and European markets. The connections used for SIFI-G and H are tab connectors up to 16A and threaded stubs starting from 20A. SIFI-F has tab connectors up to 20A and threaded stubs from 25A.

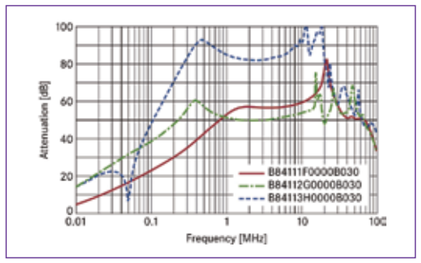


Figure 2: Attenuation curve of various SIFI types.

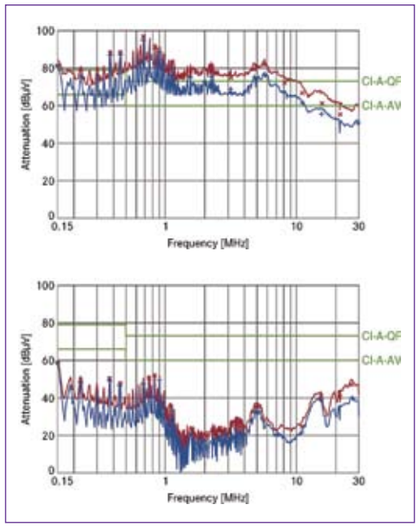


Figure 3: Disturbance voltage measurement.

Broad range of applications

The medical version is used wherever the leakage current must be kept low. This can be the case for X-ray equipment, computed tomographs, ultrasonic and other diagnostic equipment.

Effective and reliable EMC is particularly important in medical equipment, as patients come into close contact with medical diagnostic equipment. Accordingly, leakage currents must be kept low and equipment malfunctions must be excluded, especially in life-support systems. But the SIFI medical version may also be used in other applications where the leakage current must be limited – e.g. where a ground fault circuit interrupter is used.

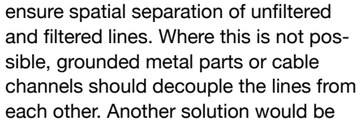
The standard versions of the SIFI are used in almost all areas of industrial electronics, both in AC and in DC applications. Thanks to their high performance and compact dimensions, SIFIs are incorporated into welding equipment, measuring equipment, machine control systems as well as fitness equipment and the telecommunications equipment. They have also proven themselves many times over in power supplies for small machines, switching cabinets and fan installations.

They are also used increasingly in solar inverters. Fig. 3 shows an example of a disturbance voltage measurement of a solar inverter. In the first case – without EMC filters – some of the values are significantly above the limits stipulated for class A (industrial environment). In the second case, a SIFI-G B84112GG125 (25A) with enhanced attenuation was used. It allows the noise voltages to be reduced to below the class-A limits to DIN EN 55011 (2007).

Disturbance voltage against frequency without EMC filter (above) and with EMC filter B84112GG125 (below). The blue curves show the measured average peak values, the red curves show the results of the quasi-peak measurement.

All SIFIs are now available from stock in small quantities. The ordering codes start with B84111F* (SIFI-F), B84112G* (SIFI-G) and B84113H* (SIFI-H). The predecessor SIFI product families, SIFI-A, SIFI-B, SIFI-C, SIFI-D and SIFI-E, are also still being manufactured. However, new SIFI versions should be preferred for new designs. In general, SIFI-A can be replaced by SIFI-F, SIFI-B by SIFI-G and SIFI-C by SIFI-H.

When mounting the filter, the package should as far as possible be connected with ground across a large area (surface without lacquer) of the other modules. This is particularly important for interference frequencies >1 MHz. At such high frequencies, a ground connection via a cable strand must absolutely be avoided (see diagram).



A cable of 10cm length has an impedance of about 140nH. This already results in an impedance of 17Ω with an interference frequency of 20MHz, for instance. This impedance is too high for a ground connection, so that practically no filter effect is achieved in the higher frequency range irrespective of the filter used. All filter concepts will fail in this case, whether they have one or two stages. Only a low-impedance wide-area ground connection will help in this case.

A frequently occurring fault source in practice is a lack of separation of interference-emitting and filtered lines. This can result in a coupling of interference and considerably reduce the filter effect. So care must always be taken to ensure spatial separation of unfiltered and filtered lines. Where this is not possible, grounded metal parts or cable channels should decouple the lines from each other. Another solution would be a right-angled crossing or twisting of the lines. This can reduce the magnetic coupling. When shielded lines are used, the shielding must be connected to the reference potential along a large area on both sides.

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Powering Agriculture

Tractor with AC/AC electric drivetrain

The world of power engineering finds its way into almost every application we come into contact. Now, even on the farm we can find up to the minute power technology in a piece of equipment that for almost generations has been a simple yet essential workhorse, the tractor. Our power colleagues in Russia send in this singular report.

By Florentsev S.N., RUSELPROM – ElectricDrive Ltd. General Director; Izosimov D.B. RUSELPROM – ElectricDrive Ltd. Vice-Director for Science; Uss I.N., RUE "Minsk Tractor Works" General Designer; Makarov L.N., RUSELPROM Corp. General Designer.

RUSELPROM Corp., a leading Russian electro-engineering development and manufacturing group jointly with Production Association (P/A) "Minsk Tractor Works" which is one of the world's largest enterprises for production of wheeled tractors, has developed an agricultural tractor "BELARUS-3023" featuring an AC/AC electro-mechanical drivetrain (EMD).

The application of EMD provides the following benefits:

- Improved technical and economical parameters of the tractor
- Reduces dynamic loads on the units of tractor and diesel
- Reduces slipping of wheels, reduces "fuel consumption – performed work" ratio by up to 30%
- Provides continuous step-less variation of speed of the tractor and aggregated tools
- Reduces cost of maintenance, repair and spare parts
- Increases total reliability, controllability and comfort

A prototype concept-tractor was created in 2007-2008 and has now successfully passed benchmark and field tests. In the timeframe 2008-2009 prototype series of the "BELARUS-3023" tractors have been manufactured and have passed tough trials in machine-test stations in Russia, Belarus and Ukraine. The tractor model "BELARUS-3023" was presented to a wide consumer audience at the largest agricultural exhibition AGRITECHNICA-2009 which took place at Hanover, Germany in November 2009 where the tractor was awarded a silver medal for innovation by the organizer of this display – German agricultural society DLG. RUE "Minsk Tractor Works" who have subsequently planned the release of the first serial party of tractors with complete traction electric equipment set (TEES) by RUSELPROM Corp. for the year 2010.

Figure1: Tractor "BELARUS-3023".

Parameters of the tractor "BELARUS-3023" of prototype series (Figure1):

- Type – general purpose
- Wheel formula – 4x4
- Nominal force at hook – 50kN
- ICE – Detroit Diesel S40E 8.7 LTA M146
- ICE power – 220kW (300h.p.)
- Engine nominal rotational speed – 1750rpm
- Engine maximum torque – 1457Nm
- Engine torque reserve factor – 40%
- Specific fuel consumption at diesel operational power – 249g/(kWh)
- Optimum fuel rate – 195g/(kWh)
- Fuel tank volume – 500liters
- Drivetrain – electro-mechanical CVT, AC drive, two mechanical ranges, 2-step automatic or compulsory switching within each range by frictional hydro-operated clutches, rear axle
- Speeds in ranges, km/h:
  - Field – 0…18
  - Road – 0…42 (50)
- Reverse riding ability – full
- Forward driving axle – with planetary final drives, self-blocked differential
- Rear axle – with differential with interlock friction coupling, planetary final drives
- Overall dimensions (length/width/height) – 6400/2630/3250mm
- Weight:
  - Design 11500kg
  - Operational 12500kg
  - Maximum admissible 18000kg
- Baseline – 3260mm
- Tyres (basic equipment, forward/rear) – 540/65R30 / 580/70R42
- Minimum turning radius – 5.5m

The complete set of a traction electric equipment of the electromechanical transmission (Fig. 2) contains:

- Asynchronous motor-generator (AMG)
- Asynchronous traction motor (AM)
- Power frequencies converters (inverters) of the generator and the motor
- High level controller (HLC), the managing director on CAN converters and a diesel engine
- Bidirectional converter DC-DC

The actual positioning of these elements on the tractor is shown in fig. 3

Parameters of the asynchronous motor-generator (MG) and traction asynchronous motor (AM) are given in the Table 1.

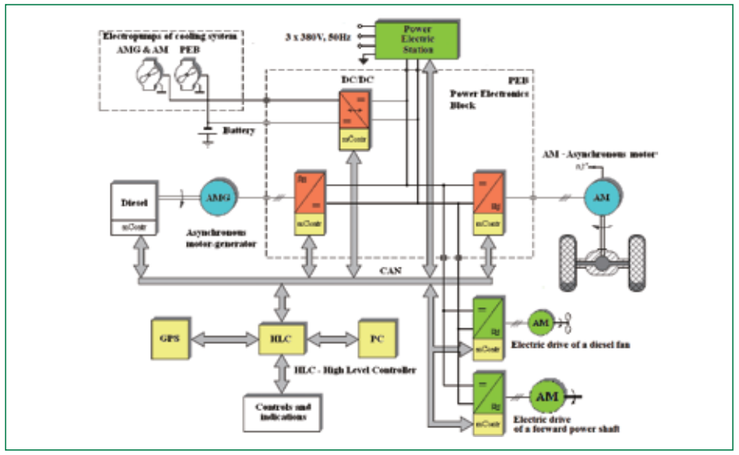


Figure 2: Block-diagram of the TEES of tractor "BELARUS – 3023" developed by RUSELPROM Corp.

Power converters of AMG and AM are integrated in the power electronics block (PEB). Power converters are mady on base of integrated 3-phase voltage inverter modules SKAI from SEMIKRON. Their maximum effective current per phase is 300A (continuously), nominal DC-bus voltage is 850V. Processor controllers TMS 320 are applied for vector control of electric machines. PEB is liquid-cooled; coolant flow is 20liter/min.

Information panel having seven modes of information display is located in the driver's cabin. It provides total control of various components and systems of the electric drivetrain and ICE.

The direction and speed of movement are controlled by joystick with mechanical interlock protecting from casual turning on. Movement is available within one of two ranges: operating (0… 18km/h) and traveling (0… 42km/h). For simplicity of aggregating with mounted implements, the tractor has a function for traveling at a low speed while fully pressed accelerator pedal.

For simplicity of diagnostics and service, adjustment and control of equipment parameters, RUSELPROM-ElectricDrive Ltd. has developed a service computing system (SCS) – special software for external PC. SCS allows adjusting settings of the control system, selectively visualizing current values of variables, saving and dynamically displaying them in operator-friendly form, providing navigation and visualization of emergency logs of the high level controller (HLC).

Additionally to the main equipment RUSELPROM-ElectricDrive Ltd. has developed and delivers are a set of options:

- Autonomous power station with rated power of 172,5kW (3x400/220V, 50Hz, η≥95%, 1200x800x300mm, 85kg, IP65)
- Electric drive of the forward PTO, mounted on tractor or on forward implements (55kW, 105Nm, η≥93%)
- Electric drive of the ICE fan with precise air-flow control and reverse mode

Parameter	MG, value	AM, value
Type	Asynchronous with squirrel-cage rotor	
Number of phases	3	
Power, kW	220	183
Nominal rotation speed, rpm	1750	1450
Rotation speed range, rpm	800…2200	-3600…+ 3600
Efficiency (with power converter)	0,93	
Dimensions (length/diameter), mm	630/545	
Cooling	liquid, 40liter/min	
Weight, kg	650	

Table 1: Main MG and AM parameters.

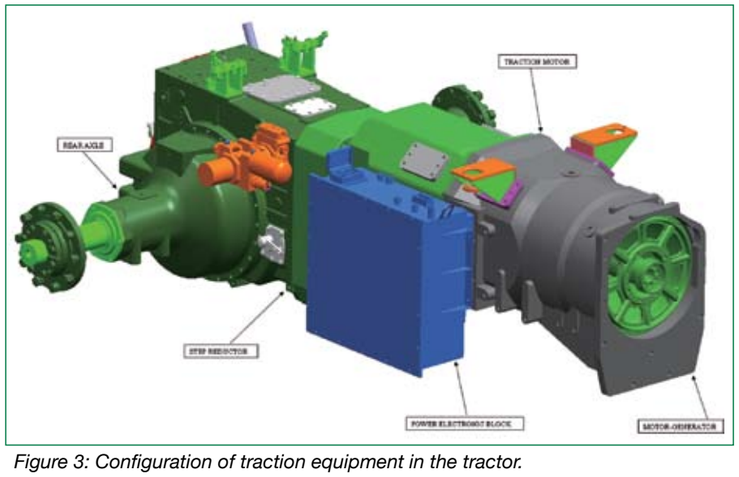


Figure 3: Configuration of traction equipment in the tractor.

for ventilation and cleaning of the radiator (max. 20kW)
• Options are fed from the PEB DC bus through controlled inverters

Advantages achieved in the tractor by application of the electric drivetrain:
• Effective, simple and reliable CVT
• Only 2 modes chosen manually (“field” or “road”)
• Automatic switching by a friction coupling providing effective acceleration in traffic mode
• Possibility of operation with high efficiency in the overall tractor speed range (see Fig.4)
• Efficient control of diesel operating mode depending on power demand
• Availability of modes of electric braking with motion energy transfer to diesel, tractor holding on ground ascents and descents, fixed moving for the pre-set small distance
• Effective liquid cooling of the electric drive

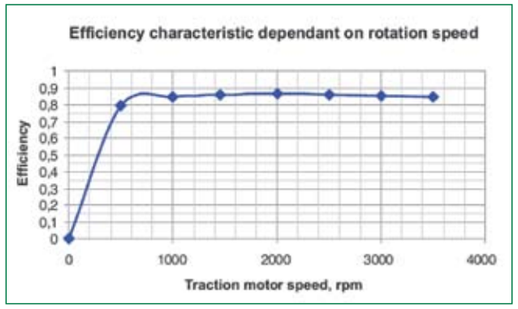


Figure 4: Dependence of the drivetrain efficiency on the traction AM rotation speed.

Advantages in the comfort and controllability:
• Simplicity and convenience of gearbox controls
• Availability of several drivetrain control modes:
- Speed setup from pedal,
- Speed setup from joystick with possibility of rough and exact adjustment,
- Tractor positioning with possibility of diesel RPM control from a pedal in this mode
- Exact tractor speed stabilization by GPS
- Possibility of automatic and compulsory diesel RPM control while working with PTO
- Ease of movement direction variation

Experimental characteristic of the total drivetrain efficiency (from the ICE shaft to the output traction motors shaft) dependant on the AM rotation speed at maximum torque and maximum power is given in Figure 4.

After the significant success with this design, RUSELPROM Corp. is ready to be a partner to vehicle manufacturers for development, manufacture, pre-production tests and serial production of TEES for stepless automatic EMD, both for on-road and off-road vehicles such as wheeled and tracked agricultural and industrial tractors, dozers, building/ road-building machines and other similar vehicles.

For further information contact florentsev@ruselprom.ru or visit the website,

www.ruselprom.ru

Variable Speed Motor Solutions

Increasing efficiency with power factor control

The words, “Global Warming, Carbon Footprint, and Energy Efficiency” are becoming mantras for the industrial manufacturing sector. With energy costs constantly rising leading to increased overhead costs, the need to use electrical energy in a more efficient manner by reducing the amount is at the fundamental basis of this crisis.

By Mark Steinmetz, Field Applications Engineer, Vincotech GmbH

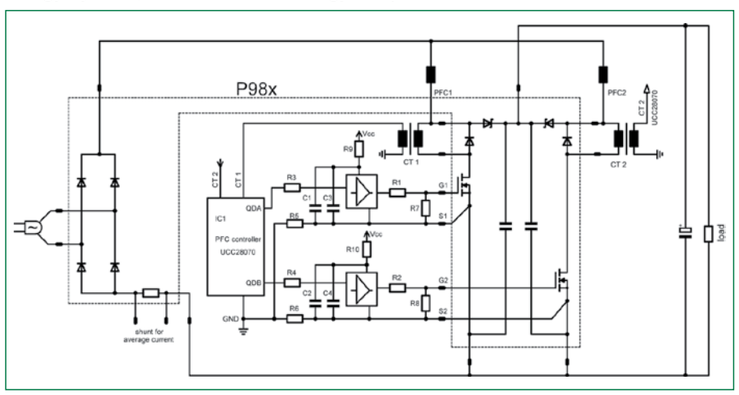
Over 40 million electric motors are used in manufacturing operations in the United States alone.[1] Electric motors account for 65 to 70 percent of industrial electrical energy consumption and approximately 57 percent of all electrical consumption worldwide.[2] Saving even a few percent of the world’s estimated 16,000-plus terawatt-hours (TWh) annual consumption of electricity[3] amounts to several hundreds of trillions of watt-hours per year.

Governments around the world are mandating regulatory pressure to increase motor efficiency. In the United States, EISA (aka Energy Independence & Security Act - Public Law 110-140) was signed by President Bush on December 19, 2007 and will become effective on December 19, 2010. From this date, motor manufacturers may not sell motors built after December 19, 2010 with a lower nameplate efficiency than EISA allows. EISA applies to both NEMA and IEC motors with features described in the details of the law. EISA allows motors that are considered “finished goods” or are shipped from the factory before December 19, 2010 to be sold after December 19, 2010. In March 2009, the European Union passed Minimum Efficiency Performance Standards (MEPS) for motors.

Brazil and China have current or planned mandatory electrical motor standards. Many motor applications will utilize an oversize motor for the required mechanical load. Some applications employ a motor’s full speed operation and control the output by mechanical means. These types of implementation for motor applications waste precious energy, since they are ran at full speed operation. Currently, the average motor in use today has an efficiency of 88 percent in converting electrical into mechanical energy. Even an efficient compliant motor can reduce energy by no more than 10%, even under optimum operating conditions (i.e. full line voltage). Industrial motor users are finding that further energy savings can be realized by using electronic speed controls (i.e. inverter based), which can reduce energy by 30%, and mechanical energy by 60%.[4] Numerous motors operate at light loads. According to a Department of Energy study, 44% of motors in industrial facilities operate at 40% or less of full load and are thus, operating inefficiently. A drive’s contribution to energy savings lies in its ability to allow you to manage motor operations to reduce output power by controlling its speed. Managing motor speeds, ramps, and available torque translates directly into managing power consumption.[5]

Power factor

Electronic designers of are now looking to maximize the energy efficiency of a motor drive application using Power Factor Control (i.e. PFC). Utilizing an electronic drive to regulating the output speed of the motor for the mechanical



Texas Instruments® has made designing much simpler using their UCC28070® controller.

load required, with the addition of Power Factor Control improves efficiency of the drive by correcting the out of phase voltage and current being used. Power factor is defined by the relationship between the instantaneous voltage and current waveform being applied. When the PF=1 (maximum), both the voltage and current are completely in phase with one another.

This happens when the load is purely resistive. If the current and voltage are out of phase, the power factor is less than one. This happens In the case of a motor. The load looks inductive, which causes an out of phase condition. Thus power being applied will not be used optimally, wasting energy. Since the voltage at the motor input is fixed, the current increases to compensate for this phase shift to supply the necessary mechanical power required. Not only does this situation cost more money to operate, it impacts infrastructure cost having to use larger conductors to power motors and larger circuit breakers. Finally, more heat is generated by the motor yielding a shorter operating life for it. Thus implementing a power factor design in a drive will yield less energy usage, lower implementation cost (size, mechanical, wiring, safety), flexibility (speed), and longer motor life.

Types of power factor control

Classic Power Factor Control (i.e. PFC) circuits used in many drive applications have been the single boost topology. Recently, Interleave Power Factor has gained much interest in the drive community. Each of these types of PFC topologies has distinct benefits. Let's take a closer look at what each has to offer the designer.

Cost

Inductors

The single boost PFC requires a single boost inductor and power switch. However, in high power motor applications (i.e. 3HP or greater), the boost inductor becomes quite large. In addition, this larger coil has increased losses, is bulky, and costly due to the large amount of copper being used.

The Interleave PFC has two parallel boost stages working180° out-of-phase with each other. This results in the requirement to use smaller boost inductors. Two small current sense transformers are also need for feedback control. The two smaller inductor sizes are the result of the two boost circuits working 180° out-of-phase. This unique technique reduces both the input and output ripple current. The results of this lower ripple current will reduce total inductor boost volume and the size of the EMI filter. Thus overall lower systems costs are realized.

Link Capacitors

Depending on the allowable motor ripple current, the single boost inductor will require a large amount of electrolytic capacitors to smooth the output from the PFC. The Interleave PFC has roughly 50% less high-frequency output capacitor current requirements compared to a single-stage topology. This reduction in current can result up to a savings of 25% reduction in boost capacitor volume.

Complexity

Single boost PFC circuits are supported by a wide variety of controllers. Thus as a mature technology, advanced designs by IC suppliers in reducing the amount of support circuitry (i.e. discrete components) required by integrating functionality into the controller have been realized. Therefore, these types of circuits are easily implemented.

Previously, designing an Interleave PFC circuit was rather complex requiring a lot of analog circuitry. However, Texas Instruments® has made designing this topology much simpler using their UCC28070® controller. Although more support discrete components are required over the single boost type of PFC, the two out of phase boost circuits are identical making the design simple.

Efficiency

Both the single boost and interleave will increase the drive's efficiency over the ±10% input voltage range. The TI UCC28070 Interleave Controller has additional provisions to improve light load conditions by turning off a phase under these conditions.

Increased Power Density & Size

Reduction in size and volume of the boost inductors, along with lower electrolytic capacitor requirements, give the Interleave a clear advantage over single boost PFC in both density and size of the drive. Thus, integrating both the drive and motor as a single unit is technically feasible.

Power module solutions

Vincotech® GmbH (www.Vincotech.com), a leading manufacture of both IGBT and Mosfet based power modules, has a wide variety of PFC module solutions for the motor drive designer to choose. Whether the choice is single boost or Interleave, the right module for the application is available for the design. Based upon these two power switch technologies, a designer can choose a module which is based upon performance using silicon carbide boost diodes, or stealth types for lower cost considerations. The selection of the type of power switch and diode combination will be based upon the designer's requirement of switching frequencies, losses, and cost.

Module versus Discrete Solution

With drives becoming a commodity product, especially in the lower horsepower ranges, cost is a driving factor. Many designers have utilized low cost discrete packaged power switches and have ignored using the benefits of a module solution. From a design standpoint, Vincotech's modules are designed to have very low inductance and extremely tight current loops. This keeps the effects of electrical noise to a minimum. Savings in using less noise components to counter these effects are realized. Modules, which are assembled and fully tested for conformity, offer a higher reliability component than multiple point to point connections for discretes.

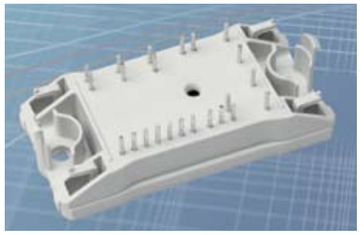
Using Vincotech's flowSIM simulator, a designer can determine the exact losses, die temperature, and other electrical characteristics for a given drive application. Each component that Vincotech qualifies, have numerous actual measurements taken under a wide range of electrical test conditions. This results in a very accurate model for each component used in the database's simulator. Thus, the results of any Vincotech module selected for an application's electrical parameters are true to real world results. This saves design time and guess work. Finally, assembly becomes much easier since a single component (versus many discretes) is used in the PCB. Reduced design time, increase reliability, and ease of assembly are thus realized. These overlooked facts lead to a much lower "total ownership cost" over discrete solutions.

Single Boost Type

Providing the designer with a diode bridge (D30) or ½ controlled inrush SCR (D40) front end plus a 500V CoolMOS power switch, the V2390-P802 will be the module choice for the application.

Interleave Type

In the case where small size and low losses are the driving factor, a PFC module utilizing advanced CoolMOS CP plus SiC boost diode will be the best solution. If the designer needs to keep the magnetics and capacitance small by using a high switching frequency, the FZ062TA99FH-P980D18 will give the designer the ability to switch up to 200 KHz. In applications where size or bulkiness is not a major consideration but cost is, the FZ062TA030FB-P983D18 using IGBT plus Stealth diode technology is available. As in the single boost type, either a full diode bridge or a ½ control SCR can be specified.



Ruggedized flow0 package.

Integrated with Inverter

If the designer wishes to take a more integrated approach such as incorporating a six pack inverter with a PFC solution, Vincotech has a broad range of modules to meet these types of applications. Available in a low cost but ruggedized flow0 package, the PIM [PIM (C +PFC) i.e. P37x series] will meet both performance and cost considerations for single boost PFC applications on motor sizes 2HP to 3HP range.

Conclusion

As the industrial market looks to replace old inefficient motors, and new equipment manufactures look to make use of better variable speed motor solutions, high efficient drives will be the solution. Manufactures that offer motor drives with power factor control will be able to work with OEM customers meeting the needs of energy efficiency, low installation cost, and flexibility.

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This PSR PWM controller achieves 30mW of standby power meeting ENERGY STAR® Level V standard and eliminates secondary side feedback circuitry, reducing component count.

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International Rectifier has introduced the AUIRF7739L2 and AUIRF7665S2 automotive DirectFET®2 power MOSFETs that deliver exceptional power density, dual-sided cooling and low parasitic inductance and resistance in a robust, reliable and AEC-Q101 qualified package for automotive applications.

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Special Report: Digital Power

The Future of Digital Power

A vital tool in the power-architect's repertoire

It is important to make a distinction between digital power management and digital power conversion. The former involves a microprocessor or microcontroller which monitors output parameters through an analog to digital converter (ADC) and modifies the reference, outside the control loop, through a digital to analog converter (DAC). This is often referred to as "digital assist". Digital power conversion on the other hand involves a digital PWM comparison in the regulator control loop.

By Benoit Herve, Vice President Marketing, Powervation, Mountain View, CA

Several concerns are driving the adoption of digital power conversion. Stringent energy-saving requirements for data-processing and networking equipment, deep submicron CMOS technology and the lifetime requirement for high-performance computing and networking systems. Conventional and digital implementations of current mode control are shown in figures 1 and 2 respectively.

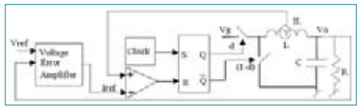

Figure1: Analog current mode control.

Figure2: Digital current mode control.

In 2006, during Digital Power Forum, two speakers in a conference session made statements that revealed the different perspectives of end-customers and those designing switch mode power supplies. The power-supply architect stated that "digital technology had already been deployed in all applications where it was prudent to do so". By this he was referring to digital assist and applications such as uninterruptible power supplies, multi-chemistry battery chargers and motion control; applications where the load time constants permit digital PWM techniques at modest clock rates.

Next, the high-performance computing architect spoke. His plea was for a digital power solution that was not merely a clone of analog control but a true adaptive solution capable of performance outside the realm of conventional analog techniques. A review of the capabilities and limitations of digital and analog signal processing can be seen in Table 1.

Analog Signal Processing	Digital Signal Processing
Computes with continuous values of physical variables in some range, typically voltages between the lower and upper power-supply voltages.	Computes with discrete values of physical variables, typically the lower and upper power-supply voltages, denoted by 0 and 1, respectively.
Primitives of computation arise from the physics of the computing devices: physical relations of transistors, capacitors, resistors, floating-gate devices, Kirchhoff's current and voltage laws, and so forth. The use of these primitives is an art form and does not lend itself to automation. The amount of computation squeezed out of a single transistor is high.	Primitives of computation arise from the mathematics of Boolean logic: logical relations like AND, OR, NOT, NAND, and XOR. The use of these primitives is a science and lends itself to automation. The transistor is used as a switch, and the amount of computation squeezed out of a single transistor is low.
Computation is offset prone since it is sensitive to mismatches in the parameters of the physical devices. The degradation in performance is graceful.	Computation is not offset prone since it is insensitive to mismatches in the parameters of the physical devices. However, a single bit error can have significant impact.
Noise is due to thermal fluctuations in physical devices.	Noise is due to round-off error.
Signal is not restored at each stage of the computation.	Signal is restored to 1 or 0 at each stage of the computation.
In a cascade of analog stages, noise starts to accumulate. Thus, complex systems with many stages are difficult to build.	Round-off error does not accumulate significantly for many computations. Thus, complex systems with many stages are easy to build.

Table 1.

An adaptive control system is defined as a form of control system in which parameters may be changed dynamically in order to adapt to a changing environment. For instance: changing power-source characteristics, changing load current profiles, ageing of components and ongoing system reconfiguration or enhancement. One unique benefit of digital power control is the ability to simultaneously optimize DC and AC parameters, for instance output voltage line/load regulation and load transient response/settling time.

Furthermore, CMOS load process technology is moving to smaller and smaller feature sizes below the point at which the transistors are useful from the analog performance point of view. Below 90nm the non-ideal VI and poor sub-threshold characteristics of the transistors are such that the analog peripherals have bad matching, low gain and poor common mode rejection. These analog blocks, particularly those in clock synthesis and recovery circuits are now very sensitive to supply voltage noise transients to the extent that supply voltage spikes or sags of the order of 10 to 20 mV cause spurious reset and data loss. In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of an analog signal Consequently, the time will come when digital control and regulation is the only acceptable solution for certain types of load, specifically loads at the forefront of the inexorable reduction in feature size predicted by Moore's Law.

Efficiency is a key consideration, as advisory standards become legislation worldwide. Digital control can improve powertrain efficiency particularly in multiphase regulators for high current loads. The load current versus efficiency curve may be broadened and flattened by

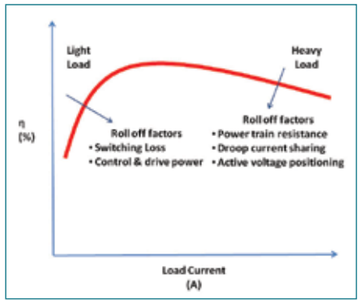

Figure3: Generic buck regulator efficiency characteristic.

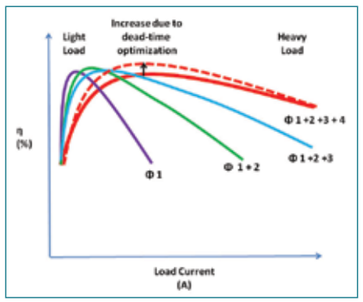

Figure4: Impact of load shedding & dead time optimization.

shedding phases at light loads and optimizing dead time for the full input voltage and load current range.

On the well-designed digitally controlled regulator an efficiency improvement of up to 2% is possible over the full load range. Bear in mind that the load current versus efficiency curve has three notable characteristics: a peak at the point of maximum efficiency, usually a duty ratio selected by the designer; a roll-off at light currents due to the effect of switching losses and the ratio of operating and drive power to load power and a decline after the peak at high loads due to resistances in the powertrain. Figure 3 shows the generic load current versus efficiency curve for a buck regulator with the characteristics identified.

Figure 4 illustrates the impact of load shedding and dead time optimization. More dramatic efficiency improvements up to 30% may be achieved through a combination of power-saving techniques in the load with those in its power supply. Smart computing algorithms, adaptive supply voltage positioning, substrate biasing, internal supply and clock gating may all be used to good effect linked with the increasing sophistication that digital regulator control brings. As there is such compelling evidence in favor of the digital regulation of power supplies why have these techniques not been adopted so readily? One reason is that many power-supply designers are not completely familiar with digital techniques and terminology. Added to that challenge is the expectation on the part of some customers that digital technology is a commodity compared with high-performance analog.

This is not the case; in fact the real paradigm change is that the intellectual property migrates from the physical circuit to the software or algorithm therein. Furthermore, many customers have completely dispensed with their analog design expertise in favor of the new digital panacea. For these customers, a turnkey solution is required. Powervation has introduced the Auto-control™ technology to deal with these opportunities. With Auto-control, the controller acts as a frequency response analyzer, measuring the magnitude and phase characteristics of the load over a frequency range. To put it simply, the designer presses a key and the control loop is optimized for the load. This may be repeated at any time during operation of the equipment to establish optimal control and stable operation. This type of approach is useful for system designers and architects who, by necessity deal with their designs from a modular or black box perspective.

In order to maximize system availability data centers are considering practices adopted in national electrical power generation and distribution systems. These techniques are facilitated by the introduction of digital power control and regulation. The term "smart grid" refers to hardware and software added to the electrical power system to achieve a) responsiveness to events that impact the electrical power grid, and b) operational efficiency of electrical power delivery.

Among the events that impact the electrical power grid are outages, (scheduled and unscheduled), load

balancing and peak shaving or sending power back to the grid when demand is high.

Smart grid hardware encompasses, a) metering and monitoring of the power system (telemetry), b) communicating the conditions of the grid in real time, and c) controlling the flow of power to maintain reliable service and stable direction. The term "smart grid" may also be applied to the power system feeding the racks and cards that make up a high-performance computing or networking system. Digital techniques can significantly improve availability, time-to-market and overall system efficiency.

Digital regulation employs comprehensive telemetry and real-time communication to be effective at the system level. Point of load regulator and load junction temperature measurement may be used to balance temperature rise in multiphase regulators or switch supplies off when overloaded. Failures may be predicted through temperature, ripple voltage or current logging. These measurements could have prevented the catastrophic failures in server systems in the past caused by the thermal ageing of iron powder cores. When a system determines that a card rack may likely fail due to excessive temperature rise or other factors, it can take measures to shed or balance loads, switch off such circuits and inform maintenance.

Time-to-market is reduced as the development and commissioning time of complex systems is reduced, especially in developments where ASICs are used. ASIC power, sequencing and noise immunity requirements are only available when first silicon is evaluated, late in the system development. Highly configurable power architecture is complementary to this approach, potentially eliminating months of cut and try. In-service upgrades may be applied by remotely programming the power system rather than servicing cards or racks.

Digital power conversion is here to stay. Many techniques that are commonplace in industrial and process control may now be applied to power supplies. Powering deep submicron CMOS loads may be the exclusive domain of digital power conversion in the future as analog performance degrades with feature size. Power consumed by a router or switch will vary in real time proportional to the traffic at the network's edge. Once power management is treated from the whole system point of view, digital power conversion becomes a necessary tool in the power-architect's repertoire.

Digital Power Matures

And greatly simplifies multiple rail management

Meeting customer demands means designers need to employ complex, high density ICs to provide differentiated features in many products now hitting the market. Increasingly these ICs and systems need multiple rails with a corresponding increase in the complexity of system power management. The use of digital power is thus becoming increasingly important.

By Patrick Le Fèvre, Marketing Director, Ericsson Power Modules

In terms of packaging and functionalities, the industry for board mounted power supplies (BMPS) - especially for the point-of-load - has been very conservative. But despite a number of individual or group initiatives, very few real evolutions have contributed to improve how those products interact with their environment. Digital power is now changing that.

Originally analog POL

When comparing the original analog point-of-load (POL) to the original microprocessors and considering where both products stand today, it is clear that without new packaging and additional functionalities, the microprocessor industry would not be where it is today. Now, comparing both industries may sound irrelevant and even extreme, but rest assured, the level of new functionalities offered by digital-power makes such a comparison very relevant.

For decades the evolution of analog POL has been driven by mechanical factors and little extra functionalities such as synchronization, sequencing, remote control or access to a compensation loop, whilst gradually shaping packaging and footprint. But despite adding those features, analog POLs have remained passive and their use has become difficult to consider for use in new applications that need to integrate energy management controllers without adding costly extra circuitry.

As reported by market analysts, analog POL will continue to develop to power standard applications. But with the increasing concern to manage energy better from component level upwards for sites such as radio-base station, data-centers or any other applications in Information and Communication Technology, this forces power supply designers to consider a new generation of digitally controlled POLs (Figure 1). These are able to communicate with energy management controllers, enabling systems' designers to optimize energy distribution throughout boards and systems down to single component level.

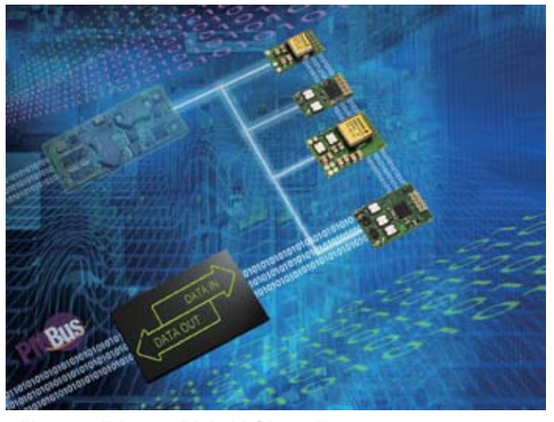

Figure 1: Ericsson Digital POL family.

Now we are back to comparing original POLs and processors, and as it has been for the processor industry, the POL will drastically evolve from being a passive-module with limited functionalities to an active-module talking and listening to its environment in order to optimize performance in real time to save energy.

From analog POL to digital

The benefits brought about by digital control and management have been described in many articles and in many places, and there is no doubt that this technology is changing the way systems' engineers are designing boards and considering energy management.

Moving from a component that has basic functionalities with limited flexibility to one that is fully configurable and re-configurable on a single command through a communication interface, is for a power designer comparable with a system designer moving from a 16 Bit processor to today's 64 Bits, requiring an increased number of inputs/outputs (I/O) and a new packaging and footprint that will make it easy and simple to operate and interconnect with the other digital components.

For many designers used to analog POL and the way in which those products have been designed for years, adding the digital dimension into

Figure 2a: 40A Digital POL BMR451.

Figure 2b: 20A Digital POL BMR450.

well established analog platforms is a challenge, especially in how to add additional I/O to products that are already full of pins.

In addition to the mechanical aspect, power designers have to consider new electrical constraints added by combining an analog power-train with a digital controller that includes an I/O interface, possibly resulting in analog and digital signal interference, with the risk of instability and a loss in performance.

In order to combine the new mechanical and electrical parameters that power designers are faced with, moving from traditional analog to digital will require a new way of thinking and more long term vision as it has historically been in the analog world for decades.

Historically the POL industry has been very conservative, and when new functionalities were needed, power designers used to add pins to an existing footprint as it is in the software industry adding a patch to existing software, aiming for a certain level of downward compatibility. This had previously been ok, but because of adding patches over patches, most of those products are not layout optimized for adding I/O connections, and definitely not ready for future functionalities that systems architects will require from POL makers.

To re-iterate, as mentioned earlier, adding the digital dimension into a well established analog world will require a new way of working when designing BMPS and especially when considering a new generation of POL.

Digital POL, think out of the box

As it has been for all industries when taking a major step forwards in evolution, the trend used to be to take an existing well-established platform (e.g. horse and cart), and add a new technology (an engine) to combine both, and then believe that you have designed a powered horse-car that will revolutionize transportation.

That is the way the car industry started but as for other industries, today's cars do not look like horse and carts, and visionary engineers are predicting that future cars will look even more different, will consume less energy, be safer, environmentally friendly and simpler to drive.

Learning from that story, from what designers knew from previous analog designs and including end-users' input, the 'think out of box' way of working makes it possible to develop a new generation of POL that are highly efficient (optimized power train), compact (high power density), easy to monitor and control (I/O and communication interface) and ready for additional functionalities.

Adding the end-users' dimension at the start is very important, especially because when systems' designers are developing new applications, they often face a paradox to power a function that might need to be upgraded, requiring more power because of increased functionalities, or less power because upgrading ASIC, FPGA or others to the new generation of components that are less energy consuming.

To achieve all the desired electrical and mechanical features, from the start, power modules designers have to consider a way to interconnect POLs to both worlds; digital and analog. All this, with the highest efficiency, greatest stability and freedom to add I/O when products embed new functionalities.

Thinking out of the box in three steps:

- Analog and digital should cohabit without disturbing each other
- I/O connector shall have room for additional functionalities
- Footprint must be simple and easy to use

From learning, to product

Behind those three steps that might seem simple and basic, in close collaboration with end-users, Ericsson's designers have driven a large project to predict how digital POL will evolve in coming years, and how to deliver a product that is ready to power today's applications whilst they simultaneously, and rapidly evolve to something that will require new features.

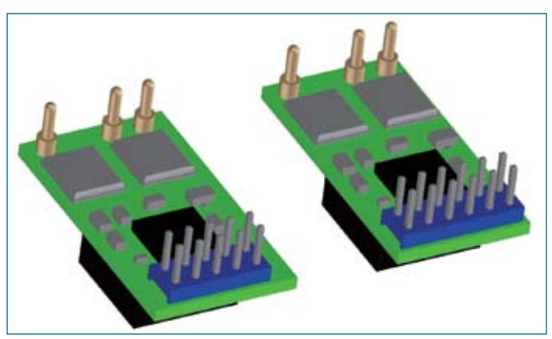

Figure 3: Point-of-load Interconnect (POLIC).

Special Report – Digital Power

The three steps in practice

Analog and digital should cohabit without disturbing each other

To make it possible for digital and analog to cohabit on the same tiny board, it is very important to optimize the power train layout to minimize parasitic components, and to room all related power component on one end of the board, reserving the opposite end for control and I/O (Figure 2a).

I/O connector shall have room for additional functionalities

Datacom servers and ATCA boards are often populated with 40 to 50 power rails delivering tightly regulated voltages to processors and other components requiring communication with their power sources. Paralleling and interleaving are a few of the extra features that the next generation of digital POLs will include, but many more not already disclosed will come.

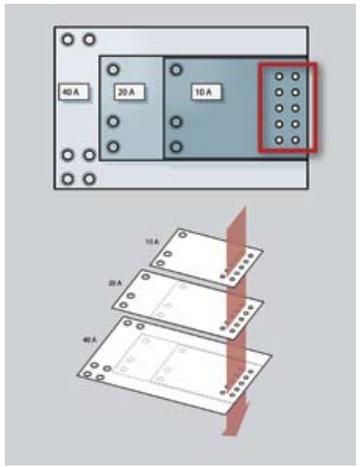

Figure 4: Digital POL scalable footprint.

To accommodate additional features without compromising a good balance between the power train and I/O, it is important not to interfere with it, and to expand I/O connectors while keeping native connections in their original position. This concept named POLIC (Point-of-load Interconnection) makes the product easier to update when new functionalities are required without affecting overall performance (Figure 3).

Footprint must be simple and easy to use

Statistically, most of the POLs sold are in the range of <10A to 40A, and when higher currents are required a multiphase based on core digital POL can be achieved. Figure 4 illustrates how easy it is to layout a multi-current solution when designing boards with digital POLs such as Ericsson's BMR451 or BMR450 (Figures 2a / 2b).

Conclusion

Adding an engine to a horse and cart may work, but may not fully meet drivers' expectations. It goes the same for digital POL, and the three steps above helped Ericsson power designers to navigate the tremendous challenges inherent to new technologies.

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Intelligent Load Switching

Helps implement reliable hot swap systems

Almost invariably, servers, disk arrays and other high-availability systems are subject to the requirement that functional modules be replaceable on-the-fly without the need for powering the system down. Replacing modules while the system is in operation is commonly known as hot swapping. A key factor in being able to provide hot swap capability is the appropriate management of the local power systems on each of the interchangeable modules.

By Srirama Chandra, Product Marketing Manager, Mixed Signal Products, Lattice Semiconductor Corporation

To support hot swapping, a sub assembly such as a printed circuit board must reliably perform several operations, and power management is among the most critical. When inserted into the larger system, a board's hot swap controller must ensure that power at the connector is stable before being distributed to other onboard systems and commanding the board to initialize. For boards drawing little current, power can be switched onboard with digitally switched MOSFETs. Higher levels of current (e.g. 10's of amperes) require more sophisticated switching strategies to avoid inducing transients in the bus-level power supplies and damaging the current-switching MOSFETs. Maximizing system-level performance requires close coordination of the low-level functions of switch control with those of the top-level hot swap management functions, such as sequencing and fault detection. While it is possible to implement such systems with hardwired circuitry, it is often more simple and cost-effective to do so using programmable system components.

Hot Swap Power Switching

The power pins on a hot swappable module's connector typically are not connected directly to the module's internal power buses. The more usual arrangement is for the local board power to be isolated from the bus power with MOSFETs or other types of power switching devices, as shown in the schematic of Figure 1. This circuit controls the connection of a single +12V bus power supply to board-side power through MOSFET M1, and is based on Lattice Semiconductor's ispPAC-POWR-1014 power management device. Some of the individual functions performed by the other parts of this circuit include:

1. Voltage monitoring – through resistive dividers R_1/R_2 and R_7/R_8

2. Current Sensing – through RSENSE and a ZXCT1009 differential amplifier

3. High-side MOSFET drive – the CHARGE_PUMP signal from the ispPAC device is a square-wave used to develop a high voltage (> +12V) across C_2 that can be used to fully switch N-channel MOSFET M1 on. M1's gate voltage is controlled by the SHUT_DOWN signal buffered by Q_2

For modules consuming small amounts of power with minimal internal supply capacitance, one could power up the module simply by switching M_1 into its low-resistance on-state (hard-switching) quickly. In the case of modules with greater power requirements, however, this will result in a large turn-on current transient through M_1, because when C_L is in the process of charging it will appear as a momentary short circuit between the supply rail and ground. The resulting current transient creates two problems. The first is that it can cause voltage drops in the bus power supply, potentially affecting the operation of other modules sharing bus power. A second problem with this scheme is less subtle: the current transient may damage the MOSFET, resulting either in reduced long-term reliability or outright failure.

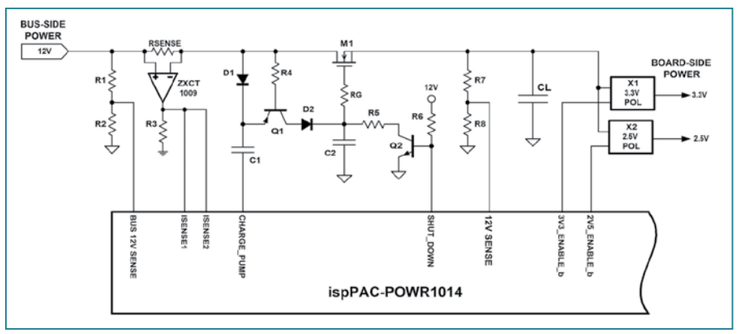

Figure 1: A hot swap controller typically employs a power MOSFET (M1) to connect the bus power to the internal board power systems after the board has been positively seated in its socket. Lattice's ispPAC-POWR1014 provides intelligent control that can be tailored to the application's requirements through its programmable logic and analog functions.

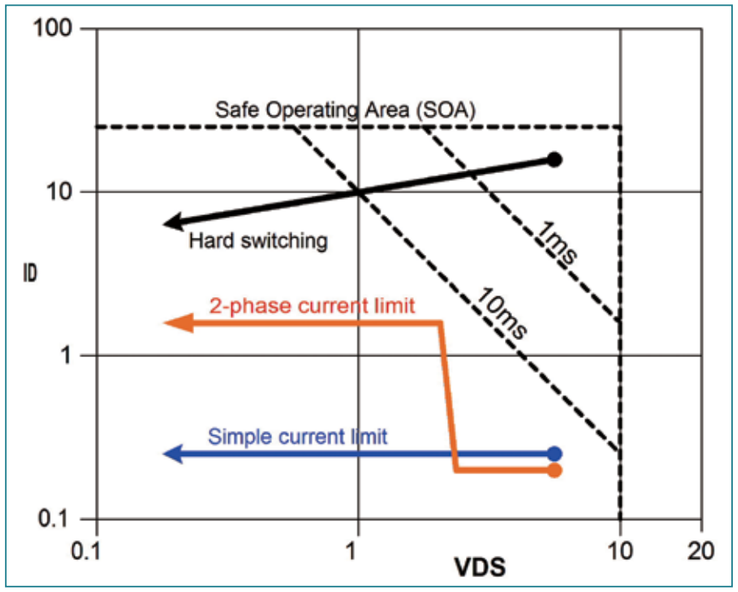

Figure 2: The Safe Operating Area (SOA) chart for a MOSFET shows the device's safe endurance limits for combinations of drain-to-source voltage and drain current. Different control strategies can be used to avoid excessively stressing the MOSFET when used as a hot swap load switch.

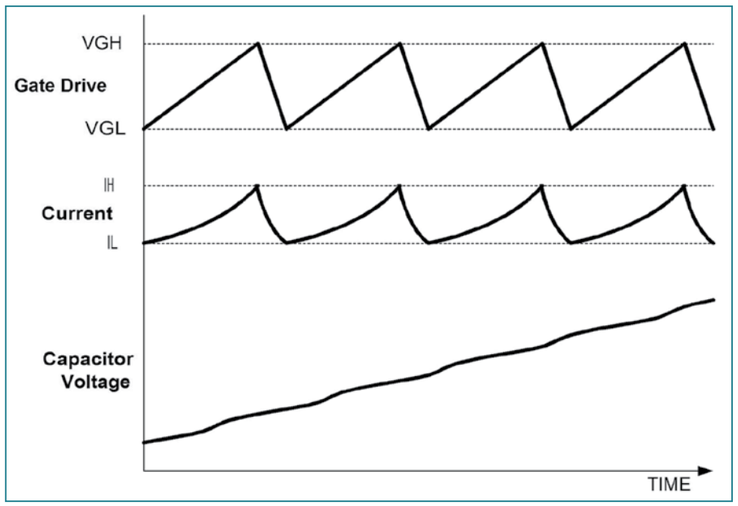

Figure 3: Hysteretic current limiting cyclically allows MOSFET current to increase to a maximum allowable level, and then throttles it back to a slightly lower level. This technique provides many of the advantages of linear current control while sidestepping many of the potential stability issues.

When charging a capacitor (C) up to a voltage source (V) through a MOSFET or other purely resistive device, the total amount of energy dissipated in the MOSFET is $CV^2/2$, the same as that which ends up being stored in the capacitor. This is independent of the value of the MOSFET's on resistance or the time needed to charge. While the total amount of dissipated energy is not negotiable, the rate at which it's dissipated – the instantaneous power - can be controlled. For example, using a MOSFET with a small on resistance results in high power dissipation for a short duration, a device with a larger on resistance will experience lower power dissipation over a longer duration. Making the appropriate tradeoff between maximum power dissipation and the time needed to charge a module's local capacitance is a key part of implementing an effective hot swap design.

The amount of time a MOSFET can safely dissipate a given amount of power usually is specified in the device's data sheet by its safe operating area (SOA) chart (Figure 2). The SOA chart specifies the maximum amount of time the MOSFET can safely remain biased under various combinations of drain-to-source voltage (V_{DS}) and drain current (I_D). Superimposed on this SOA chart are "trajectories" of V_{DS} and I_D corresponding to the control schemes to be discussed.

If one switches the MOSFET on quickly (shown by the black "Hard switching" curve of Figure 2), it is subjected initially to a maximum value of V_{DS}, with I_D limited only by the channel resistance and parasitic impedances such as PCB trace resistance and inductance. As the load capacitor charges, the MOSFET's operating point moves left and down to more benign conditions. If the operating point does not shift quickly enough, the MOSFET may be damaged or destroyed. And even if one selects a MOSFET with sufficiently high power dissipation capabilities, the problem that the initial current surge could disrupt bus-side power supplies still remains.

Controlling Current Surge

One common technique used to avoid the problems resulting from abruptly turning on the MOSFET is to ramp up the MOSFET's gate voltage gradually, at a rate that is slow enough so that the load capacitor's voltage will track with a minimal VGS. This ensures that the operating

point will remain in a low-current region near the bottom of the SOA chart. This strategy can be readily implemented with the circuit of Figure 1 by appropriately selecting the value of C_2.

While simple to implement, ramp-up up rates in the above scheme must be heavily margined to accommodate component variation in both the MOSFET and power-bus load capacitance. For low to moderate current applications, specifying a slightly larger MOSFET may not be much of an additional expense, and may well be justified by cost-savings from simplified control. In other cases, where large on-board capacitances must be charged, this approach can result in significant delays between the time when a module is plugged into the larger system and when it is ready to begin operation.

With current-sensing hardware, it becomes possible to maintain a constant current trajectory through the SOA by using negative feedback control. By providing precise regulation of drain current, the MOSFET switching trajectory (Figure 2, simple current limit) can be set to a higher current level than would be prudent in the previous case of simply ramping up gate voltage in open-loop fashion. Because it is often necessary to monitor current for diagnostic purposes, current-sensing hardware may already be available in a design, in which case only the control logic need be added.

Linear current-mode control, however, can be tricky to implement reliably, with the potential for instability and uncontrolled oscillation. An alternative is to use a hysteretic control scheme (Figure 3), in which the MOSFET current is maintained between a lower and an upper threshold. In a hysteretic control scheme, MOSFET gate voltage is ramped up until the drain current reaches a predetermined upper threshold. At this point, the gate voltage is ramped down until drain current falls below a predetermined lower threshold. The process then repeats, with drain current varying between the two threshold levels.

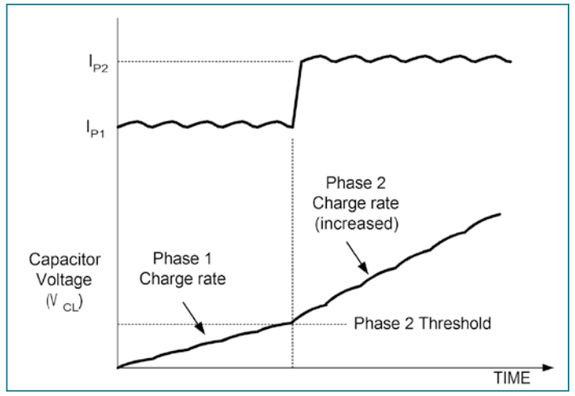

Figure 4: A two-phase switching strategy first charges the on-board capacitors at a low current when the switch MOSFET is subject to a high V_{DS}, and then increases the current when the capacitors are partially charged and the MOSFET experiences lower V_{DS}.

While hysteretic control could be implemented with a small number of discrete components, it can also be realized by merely reprogramming the ispPAC Power Manager in the original circuit of Figure 1. Each of the Power Manager device's voltage monitor pins supports dual comparator functions with independently programmable high and low voltage thresholds. Programming the device's FET driver outputs to a higher current provides a faster but still controlled rise time for MOSFET gate voltage and corresponding drain current. An additional advantage of using a programmable device to manage the current control process is that it is straightforward to fully integrate the hot swap control logic with that needed for normal board operation. For example, the Power Manager device can be programmed to permit higher currents during the short time the board is initializing, and then to seamlessly shift into normal operating mode, where the MOSFET is completely turned on and current is monitored at a lower threshold to detect board fault conditions.

Optimizing Switching Performance

The programmable nature of the Power Manager device supports the designer in realizing more highly optimized control techniques at little or no additional cost. One example of such a technique is charging up board capacitance in two separate phases – a low current initial phase and a high current final phase, as shown in Figure 4. The value of adding this complexity is that it optimizes charge rate so that the MOSFET's operating point more closely follows the constraints of the device's SOA curve (2-phase current limit plot in Figure 2). This provides two benefits over the constant current charging scheme described previously. First, by switching to a higher current midway through the charging cycle, less time is needed to bring the load capacitor up to operating voltage. Second, this scheme only operates the MOSFET at higher current levels when the V_{DS} across the device is relatively low, minimizing power dissipation. This in turn allows the designer to specify a smaller, less expensive MOSFET for a desired level of performance. While this technique is straightforward to implement with a programmable hot swap controller such as an ispPAC Power Manager device, it would require significant additional hardware and design effort if realized using a fixed-function hot swap controller. Programmability also makes it straightforward for the designer to vary control parameters, making it easier to adapt the same basic circuit for use in multiple applications with few or no hardware changes.

Summary

Supporting hot swapping features requires sophisticated power management techniques. While fixed-function controllers may be useful in the most simple designs, programmable solutions provide the designer with the flexibility needed to meet increasingly demanding applications. This article has described one example of how the performance of a load switch can be enhanced through the use of programmable control.

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Managing Multirail Systems

Digital power management made simple

Sophisticated systems with high data processing requirements like video, medical imaging, optical communications or networking utilize complex FPGAs, ASICs, and processors that are powered from multiple voltage rails. These rails have strict requirements for sequencing, voltage accuracy, margining and supervision. Digital power managers add a critical layer of protection to ensure the system powers up correctly and are invaluable in protecting the processor from damage during operation. Tight control of the supply rails helps to improve overall system performance and saves the embarrassment of telling the boss you just blew up the $10K processor. A properly designed digital power management system can also provide useful power consumption data, thereby enabling smart energy management decisions.

By Dave Clemans, Senior Applications Engineer and Alison Steer, Product Marketing Manager, Linear Technology Corporation

Digital power management

A well-designed power management circuit must be robust, easy to use and not consume too much board area. Power management functions have been realized in the past using a plethora of ICs such as FPGAs, sequencers, supervisors, DACs and margin controllers. Linear Technology's LTC2978 digital power management IC combines all of these functions to control up to 8 rails. Figure 1 shows an example of one channel of the LTC2978 controlling a DC/DC converter. A slow and highly accurate analog/digital control loop is wrapped around the DC/DC under control to provide accurate monitoring, sequencing, trimming and margining.

This provides a number of benefits on a system level, since supplies can be easily configured via a PC for faster product development, CPU performance can be optimized with real-time feedback, while digital communication provides easy interfacing to other system ICs to enable complete digital management from a desktop. Differential voltage sense inputs and DAC output pins naturally cancel any ground shifts and noise that may be present, thereby allowing the LTC2978 to truly achieve ±0.25% accuracy in a system. A soft connect feature on the DAC outputs ensures that the DACs do not induce transient voltages when connected. One additional high voltage monitoring input allows users to monitor an input supply rail of up to 15V, however the LTC2978 can operate from a supply voltage as low as 3.3V. The LTC2978 can operate autonomously, or responds to control commands from the system host processor, and to report telemetry. LTC2978 combines all the necessary power management and monitoring features into a single device that can be daisy-chained together with other LTC2978s via a single clock line and optional fault sharing lines to control up to 72 voltages on a single segment of an I^2C bus, as shown in Figure 2.

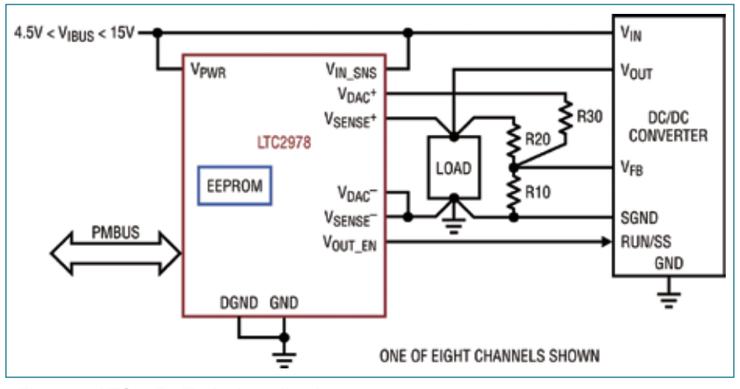

Figure 1: LTC2978 Typical application.

Requirements of a board level digital power management system

The following highlights the major requirements for developing board-level digital power management systems:

- **Sequencing.** Certain processors demand that their I/O voltage rise before their core voltage but certain DSPs require just the opposite. Power down sequencing is also a common requirement. An ideal sequencer, like the

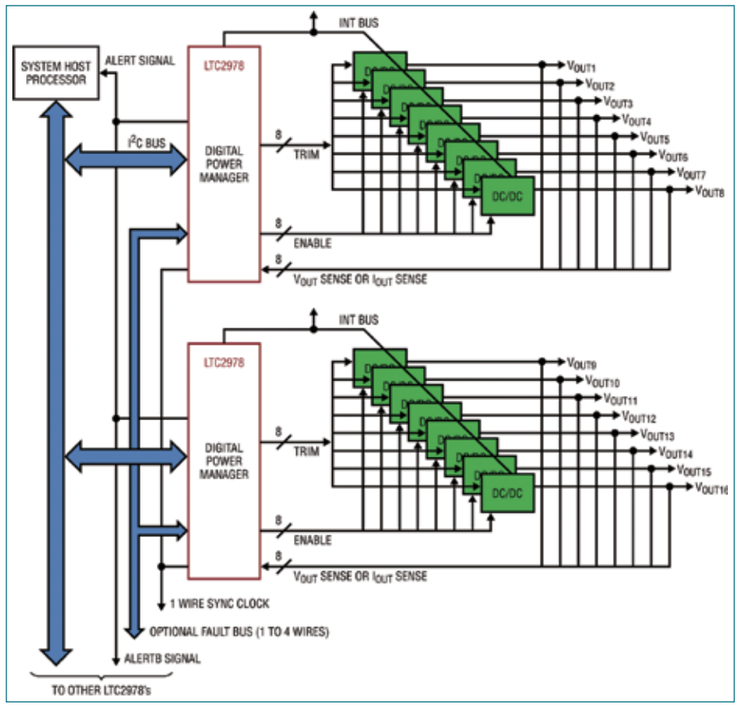

Figure 2: Cascading LTC2978s for a multirail application.

LTC2978, allows arbitrary sequencing of any rail in the system and allows any rail to depend on any other rail. This is accomplished by using one universal clock to synchronize all sequencer ICs to the same time base. Dependencies within the sequencer are established with configurable settings. To establish fault dependencies across sequencers, the LTC2978 uses a fault-sharing bus. As an example, a fault group may be the core and I/O rail of one processor or all 7 rails on an ASIC. A dependency is established between these rails, such that if one of them does not come up to its full voltage during the power-up sequence, the sequence is aborted.

• **Supervision**. High-speed comparators are needed to monitor the voltage levels of each rail and must take immediate protective action if a rail goes out of its specified safe limits. With the LTC2978, the host is notified that a fault has occurred via the SMBus ALERTB line and dependent rails are shut down to protect the processor. The response time is on the order of 10s of microseconds. Variable deglitching of the OV/UV function aids in preventing false trips on noisy rails.

• **Accuracy**. As voltages drop below 1.8V, many off-the-shelf modules have trouble maintaining V_{out} accuracy over temperature. Absolute accuracy requirements of ±10mV on the supply rails are not uncommon and trimming the output voltage now becomes necessary. Margin testing should be performed to assure the system functions properly even if rail voltages drift. This rail voltage drift can be completely eliminated by externally trimming the module. The LTC2978 contains a 15-bit digital servo loop that measures the rail voltage and continuously trims the output voltage to within ±0.25%.

• **Margining**. The LTC2978's digital servo loop described above is used to margin the rail voltages up and down during manufacturing test with one I^2C command. There is one servo per channel.

• **Voltage and current monitoring**. To achieve the desired reductions in power consumption, it is necessary to characterize the loads during all modes of operation. FPGA users have the ability to optimize their code to minimize power. The real-time telemetry of the LTC2978 makes this easy. To accurately measure currents without introducing unwanted loss, the power management IC must have extreme accuracy and resolution. The LTC2978 has a voltage resolution of 122µV and an accuracy of ±0.25%.

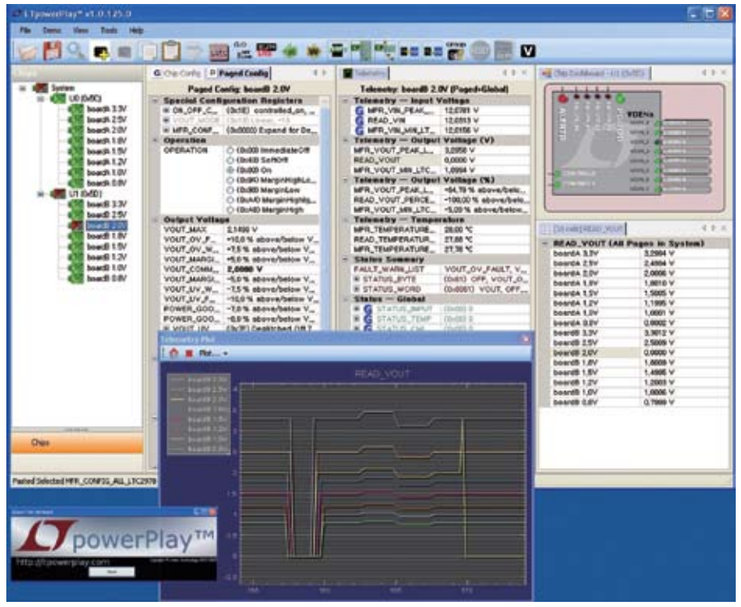

Figure 3: LTpowerPlay interactive GUI.

• **Fault diagnosis**. Inside the LTC2978 is a log of all the faults that have occurred within the last 500ms. It is a simple task for the LTC2978 to indicate which rail has faulted or which part has exceeded its temperature limit and shutoff, making system debug a short task.

• **Fault logging**. Wouldn't it be great to be able to hook up your PC to a field return, click a button in a GUI and read a log of what happened in the last 500ms prior to the failure? The LTC2978 has a rolling average recorder that records peak, min and instantaneous values of voltages, currents and temperature allowing the system to be polled and diagnosed for failures. Designers will find this feature useful during the prototype phase.

• **Autonomous operation**. A really good power management IC must perform all of the functions without any intervention from a host processor. The LTC2978 can be ordered preprogrammed for "set and forget" operation, while the simple digital interface enables field updates of new configuration files for adjusting system performance.

Using these features while keeping it simple

LTpowerPlay™ (see Figure 3) is a user-friendly, interactive, graphical user interface (GUI) that allows the designer to connect a PC to the LTC2978 digital management platform via a tiny connector to access all of its features. The power management system can be completely programmed and controlled without writing a single line of code. The GUI translates the commands into a configuration file that is stored in the EEPROM of the LTC2978. An offline mode allows the user to develop a configuration file for loading before building hardware. During board development, users interactively optimize their configuration. The custom configuration file can be preprogrammed into the device. First pass success is assured.

Conclusion

Digital Power Management adds value during four key phases of the system life cycle. During the design and development phase, the designer can configure the digital power management system to optimize sequencing, minimize power consumption and characterize system performance. Production margin testing is easier to perform than traditional methods because the entire test can be controlled by a couple of standard commands over an I^2C bus. A simple but powerful GUI obviates complicated FPGAs with lots of custom code. In the field, the power management IC operates autonomously to provide continuous supervision and takes preprogrammed action in response to faults. The digital power management system can also be used to report system health status to determine if repairs are needed. If a board is returned, the fault log can be read back to determine which fault occurred, the board temperature and the time of the fault. The LTC2978 is a digital power management IC that provides this functionality and much more to simplify the task of designing multirail power management systems.

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Modeling of SMPS Output Impedance

Fast estimation of time domain output voltage step-load variations

Stability of closed-loop systems as Switch-Mode Power Supplies is typically tested by measurement techniques of signal injection inside the loop, with the help of software tools, spectrum analyzers and isolation transformers available in the market often at a considerable price. Measuring the loop in the frequency domain allows prediction of system response in the time domain, for example against a step load variation.

By Pietro Scalia, EMEA Design Services Group, Power Management Products, Texas Instruments, Germany

This article introduces a quick technique to estimate the ouput voltage variations generated by a step load change, providing a simple equivalent modeling of the ouput impedance of the converter. As an example of the described methodology, its application to an automotive multiphase boost converter for audio amplifiers is presented, where the introduced modeling technique is used to estimate the step load output variation in correspondence of the variation of the ESR of the output capacitors of the converter at negative ambient temperature. According to the drastic ESR value excursion, two equivalent networks modeling the output impedance need to be created, to represent the different behaviors of the closed loop system in the frequency domain. These models allow to determine in a closed simple form the output course in the time domain of the output voltage under the effect of a step-load transient, or they also easily allow the simulation in a proper software environment of the transient event for a more detailed analysis.

Converter in analysis

The designed converter is meant to supply a Class-D Audio Amplifier for Automotive application. It is a 4-Phases Boost controlled by the multiphase current-mode controller TPS40090 from Texas Instruments. The converter is running at about 250kHz. Input voltage range is from 8.5V to 18V, output voltage is 24V and maximum load is 17A. The converter has an output total

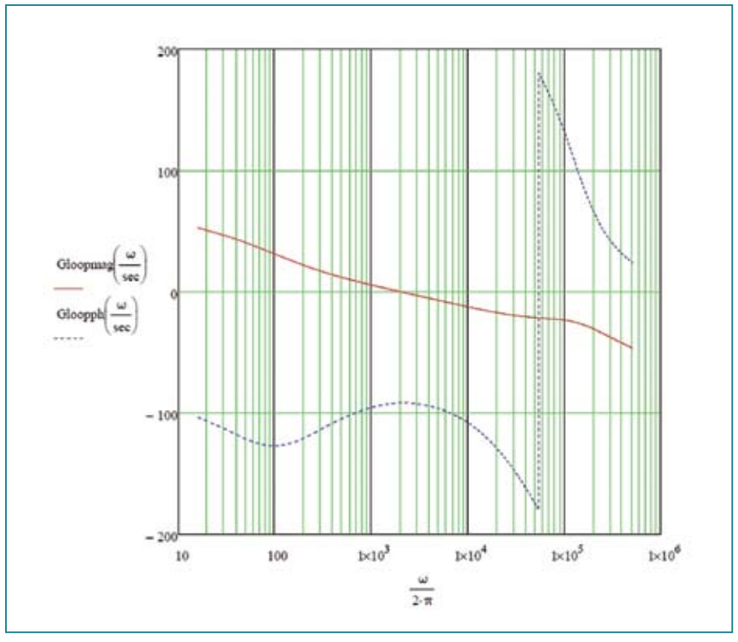

Figure 1: Open Loop Response at Tamb=25°C, full load, Vin_min=8.5V

capacitance as low as 2200µF, electrolytic type, and an output ripple of less than 100mV, made possible by the interleaved phases.

The specific system has been completely modeled and represented in a mathematical environment like MathCad to design its single elements, from the power components to the control parts, estimating the overall converter performances. In particular, the open loop response has been evaluated creating a model of the power stage plus current mode modulator (including slope compensation), together with the modeling of a general type III compensation block. In Fig.1 the open loop response is displayed. Sub-harmonic resonance effect is noticed at fs/2, which Q factor can be lowered by the proper amount of slope compensation, added in the schematic with a circuit external at the PWM (the IC has a fixed internal amount of slope compensation useful up to moderate duty-cycles). The cross-over frequency is set at fco=2kHz, after compensating the ESR Output Capacitance zero at about fz_esr_Cout=8kHz and closing before the effect of the right half plane zero located in the worst case at fz_RHP=36kHz.

Variation of the ESR of the Output Capacitance with negative Temperature

With ambient temperature decreasing down to -55°C or at least -40°C by specification, a drastic degrade of the characteristic of the output capacitors happens. In particular, the ESR of the electrolytic capacitors increases exponentially with temperature. Sometimes is also difficult to find in the datasheets the value at these low temperature, so direct measurements are mandatory. As examples, in the following table, some benchmark of different series of commercial products is provided.

The choice of the capacitor series is based mostly on dimensions and cost. The availability of the ESR data at temperature lower than -10°C is not always guaranteed, so direct measurements are sometimes mandatory. Some better characterized at negative temperature capacitors, are often too big or too costly to be used in some

Model (Rated 35V)	C [µF]	Op. T_{amb} [°C/°C]	Case Size ØDXL[mm]	ESR(20°C) [mΩ]	ESR(-10°C) [mΩ]	ESR(-40°C) [mΩ]	Z-Ratio(120Hz) Z(-40°C)/Z(20°C)
NCC LXY	330	-55/+105	10X20	65	130	NA, 300(measured)	3
NCC LXZ	470	-55/+105	10X20	52	104	NA	NA
NCC GPA	680	-40/+125	12.5X20	A	NA	220	4
NCC LBG	1000	-40/+125	12/5X20	57	NA	290	3

Table 1: Variation of ESR for different series of NCC Electrolytic capacitors.

specific applications. The extreme variation of ESR value, up to 30 times the value at +20°C, can cause the compensation loop at negative temperature to become inadequate, causing oscillations. Note also, that in multiphase system oscillations can happen at the cross over frequency, and at sub-multiple of the switching frequency (not just at the sub-harmonic), due to the out of phase interleaved switching mechanism. In any case, even when the system remains stable, the output step load variation is significantly degraded.

Introduced Methodology

Having a complete system simulation of the closed loop system, stability analysis can be performed with the new value of ESR to evaluate the new phase and gain margins. Indeed, also tests on the bench on a refrigerated unit can be performed with closed loop measurement tools based on signal injection.

More simply, however, the effect of ESR variation can be estimated through the modeling of the output impedance of the converter. The basic hypothesis is that Rout (load) is still larger enough than the ESR of the output capacitance (true with electrolytics).

In Fig.2 the sketched bode plot of the closed loop impedance of the converter is obtained. The open loop impedance given by the DC load resistance (1.41Ω), shows a pole given by:

fp=1/(2*π*Rout*Cout)=50Hz
and a zero given by **fz_ESR=1/(2*π*ESR_Cout*Cout)=7.8kHz**

at ambient temperature of 20°C.

The open loop gain of the converter is taken from Fig.1, with a cross-over frequency of fco=2kHz and a flat -20dB/dec slope. As a result, the closed loop output impedance [(Zout/(1+G_loop)]dB

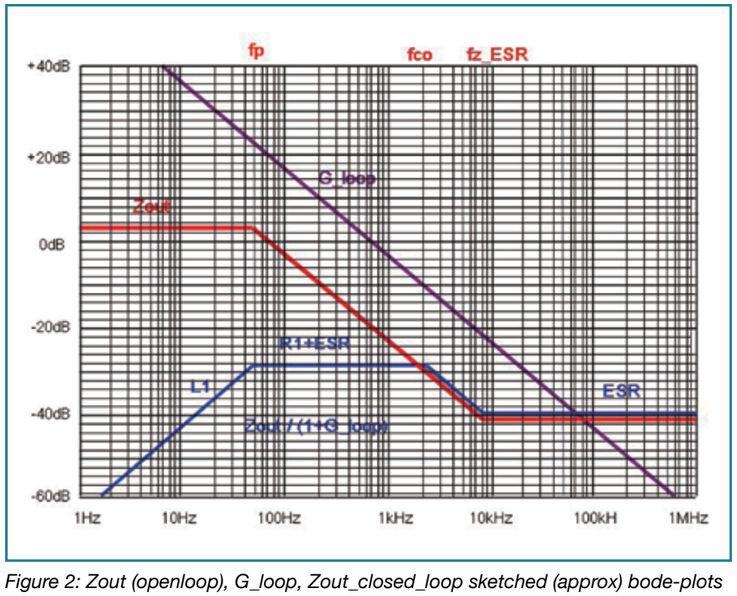

Figure 2: Zout (openloop), G_loop, Zout_closed_loop sketched (approx) bode-plots when fco<fz_ESR.

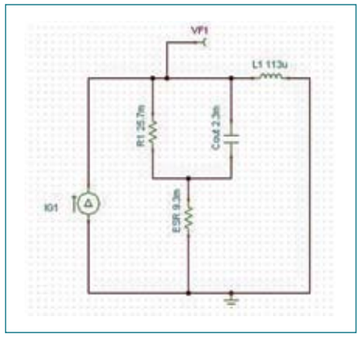

Figure 3: Equivalent Circuit for Zout_closedloop when fz_ESR>fco.

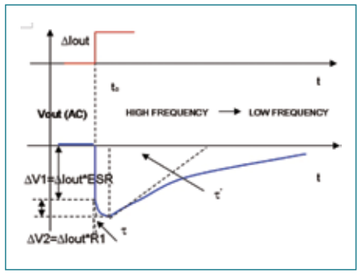

Figure 4: Output Voltage step load variation for fz_ESR>fco.

is drawn by difference of Zout and G_loop in Fig.2, because G_loop>>1 for f<fco. This closed loop impedance is therefore equivalent to the general network of Fig.3 (values are particular to the specific example), where the values of L1, R1 can be calculated from Fig.2, while Cout and ESR are given.

By example, in fact, using nr.7 capacitors NCC LXY 330uF (Cout=2.31mF, ESR=65mΩ/7=9.3mΩ), by the following calculation applied to the bode plot, it is possible to calculate:

$$R1 + ESR = 10^{\frac{-29}{20}} = 35m\Omega \ ;$$

$$L1 = \frac{10^{\frac{29}{20}}}{2 * \pi * fp} = 113\mu H$$ R1=25.7mΩ .

In the time domain the schematic of Fig.3 can be used to determine the response of the converter to a step variation of load. Fig.4 shows the curse of Vout with the different contribution according to each element of the circuit of Fig.3, for the next simple equations for the two tangents:

$\tau = Cout * \frac{R1 * ESR}{R1 + ESR}$ =16µsec; $\tau' = \frac{L1}{R1 + ESR}$ =3.2msec.

Results give ΔV1=0.45V and Δ V2=1.28V, ΔVtot=1.73V.

If the circuit of Fig 3 is simulated, using TINA TI, the transient waveforms of Fig.5 are generated (green waveform), which give the same values as the one easily calculated by the previous equations.

If this method is now applied to the operating case of Tamb=-40°C (ESR=300mΩ/7=42.9mΩ, fz_ESR =1.6kHz), the new plots obtained in Fig.6, due to the very high value of ESR, show a physics inconsistency: R1 comes out negative. It's easy to verify graphically that this new situation, in the frequency domain, translates in practice in the relations fz_ESR<fco (new fco=8kHz).

In this different case, the new model that comes useful for the methodology, is the one represented in Fig.7, with the new unknown L2, L3, R2. By plot measurement it is possible to calculate ESR//R2=32mΩ, and from this

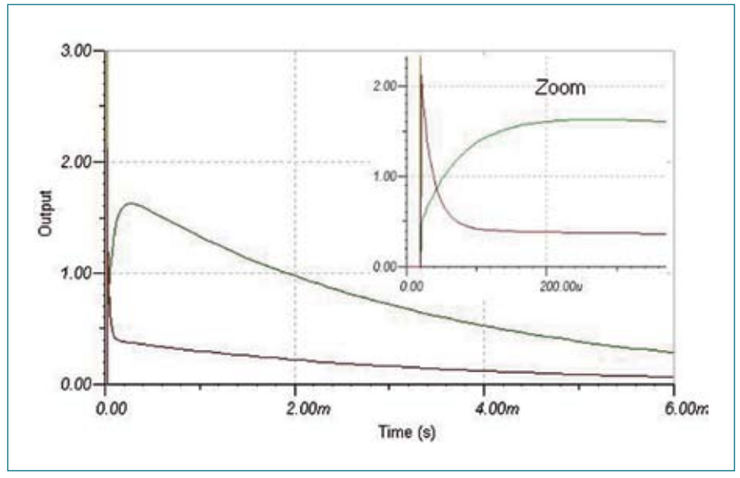

Figure 5: Output Step Load Simulation results (both models).

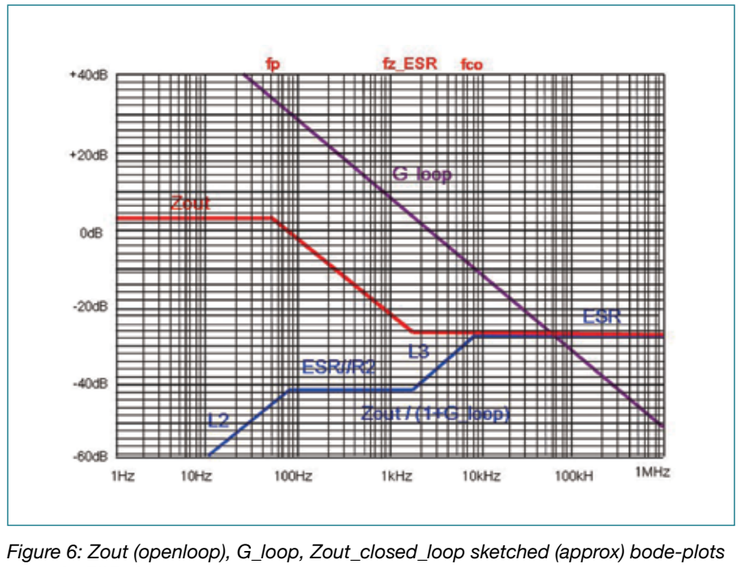

Figure 6: Zout (openloop), G_loop, Zout_closed_loop sketched (approx) bode-plots when fz_ESR<fco.

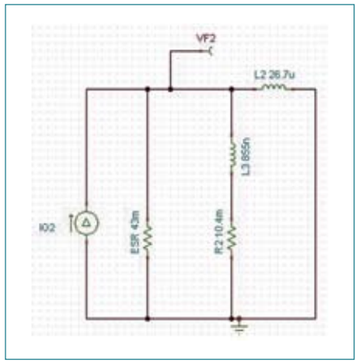

Figure 7: Equivalent Circuit for Zout_closedloop when fz_ESR<fco.

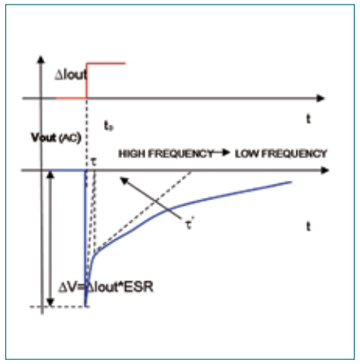

Figure 8: Output Voltage step load variation for fz_ESR<fco.

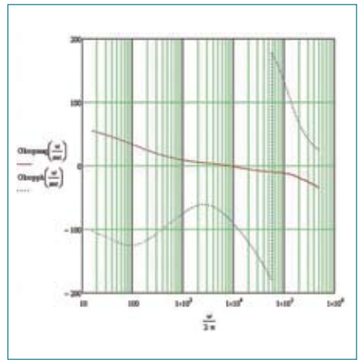

Figure 9: Open Loop Response at Tamb=-40oC, full load, Vin_min=8.5V.

obtain the other parameters with the equations:

$$R2 = \frac{ESR * (ESR \,//\, R2)}{ESR - (ESR \,//\, R2)}$$

$$L2 = \frac{ESR \,//\, R2}{2 * \pi * fp}; \quad L3 = \frac{ESR}{2 * \pi * fco}$$

In the example case, R2=10.4mΩ, L2=26.7μH, L3=855nH.

In the time domain the schematic of Fig.7 gives the response to a step load as in Fig.8, with the different contributions for every element of the circuit. The two tangents are given by equations:

$$\tau \cong \frac{L3}{R2 + ESR} = 16.6\mu sec;$$

$$\tau' \cong \frac{L2}{R2 \,//\, ESR} = 3.2msec.\ \Delta V = 300m\Omega *$$

50A/7=2.16V. The simulation of circuit in Fig.7 with TINA TI is again in Fig.5 (red waveform), confirming the previous results.

Stability Check in the time domain.

The explained methodology of analysis of the step load variation, has been conducted starting from the frequency domain (more confort zone for most) to the time domain. The derived equations, however, just used in the opposite sense, allow therefore to check for stability of the system, to derive the effective fco of the system. And nothing else than a scope and a calculator is needed to perform the very simple measurements (times for tangents of curves, amplitudes for escursions), and the relative calculations to derive fco.

Furthermore, this analysis allow to precisely predict the impact of the real ESR at various temperature on the loop, and therefore on the step load variations, to achieve the optimization of the system through the proper choise of the output capacitance. It is in fact important to stress here once more that the major cause for the increase of step load ΔV at negative ambient temperature is the degraded ESR, and not the bandwidth, that in second case is even larger (fco=8kHz) as we can see from the body plot (MathCad simulation) of Fig.9. From that point of view, there is a benefit on the dynamic performance, and even if the initial peak ΔV will be higher, the duration of the peak is shorter, and most of the output voltage excursion stays below the one at low ambient temperature.

The herein described methodology is therefore the correct approach to use, being usually the step load Δ V estimated just by the well know formula ΔV=ΔI/(2*π*fco*Cout), that is however quite approximate and cannot be used with consistent values of ESR in the output capacitor. This formula just addresses fco as the way to reduce ΔV output. The real way to reduce the Step Load Δ V, is to operate the proper choice of Capacitors, to obtain a value of ESR at minimum operating temperature, able to handle the maximum Δ V acceptable for the specifications of the application. The settling times are determined also by the fco, so a proper choise of that value also has also to be done according to the desired time response.

About the complete loop response at negative ambient temperature, some attention has to be dedicated to verify the gain margin at subharmonic frequency, due to the higher fco, with an increased gain at fs/2. To avoid eventual inconditional instability rise, a proper increase of the amount of slope compensation can be therefore needed.

Conclusion

The introduced method allows to perform analysis of closed loop power systems, without the need of sophisticated measurements tools. With the only aid of an oscilloscope and the defined set of equation, it is possible to quickly shift from the time domain, back into the frequency domain, verifying the bandwidth of the system. A delicate application, of a multiphase boost supplier of an audio amplifier for automotive has been fully analyzed in the critic situation of deep negative ambient temperature, to estimate the effect of the drastically increased ESR of the output electrolytic capacitors selected according to cost and dimension for the application. General criteria and procedure to approach the selection of output capacitors for optimization of the ouput voltage step load variations have been reviewed and validated by the introduced modeling and methodology.

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Power Systems Design Europe **Green Page**

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Solar Gets Competitive

Reported by Cliff Keys, Editor-in-Chief, PSDE

Installations of Photovoltaic (PV) solar systems will soar in 2010, but a dive in the prices of solar components means industry competition will intensify. The global installed watts for PV systems are predicted to grow by 64% in 2010, reaching 8.3GW which will bring a return to the growth levels seen before the fall of 2008 as the worldwide recession recedes and as new geographies and segments of demand emerge. But despite the projected return in demand for this year, the tremendous price erosion that occurred in 2009 continues to squeeze profits. On average, crystalline module prices last year fell by 37.8%, solar wafer prices plunged by 50% and polysilicon prices crashed by 80%, according to iSuppli Corp.

This erosion in pricing is bound to change the face of the solar industry. The freefall of PV prices represents a permanent ratcheting down of price structures that will transform the industry into a more competitive marketplace.

Suppliers will need to continue accelerating cost reductions in order to keep up with the price declines and to repair compressed profit margins. When the cost-down programs eventually catch up with the rate of price declines, an overall improvement in the profit picture

can be expected.

After suffering losses during much of 2009, PV profits will continue to improve in 2010, following a move into the positive during last year's fourth quarter. iSuppli also is projecting that prices on average will pop back by more than 10% in the final quarter of 2010, despite declines for the entire year.

The growth of PV installations in 2010 will be led by a newly energized German market, which recovered from sluggish performance in the first half of 2009 to achieve gradual growth in the second half—a trend expected to continue for the first six months of this year.

The German market could stall again by summertime, if the feed-in-tariff (FIT) designed to encourage the adoption of PV systems is trimmed by the government. The position in the overall PV market held by Germany which accounted for 50% of total worldwide PV installations in 2009 is of such importance that the collective PV demand accruing from other countries will not be sufficient to compensate for a German FIT reduction of 15% if that were imposed in mid-2010.

Several new growth markets will come into play in 2010, the most significant of which are the United States, Italy and latecomer China. Together, these three markets will account for 50% of the growth projected to occur in 2010.

More players will enter this year, led by South Korea's Samsung and LG Electronics, already the world's largest LCD panel makers possessing vast experience at moving into new areas of operation, as well as Taiwan's TSMC foundry and U.S. engineering giant Bechtel.

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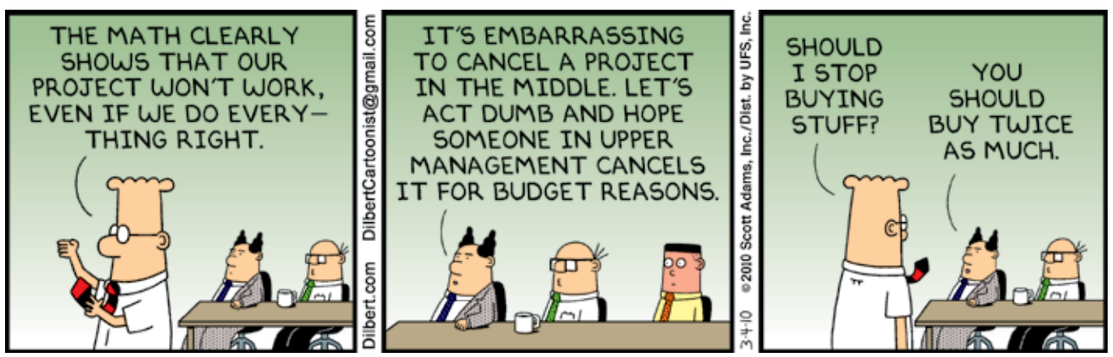
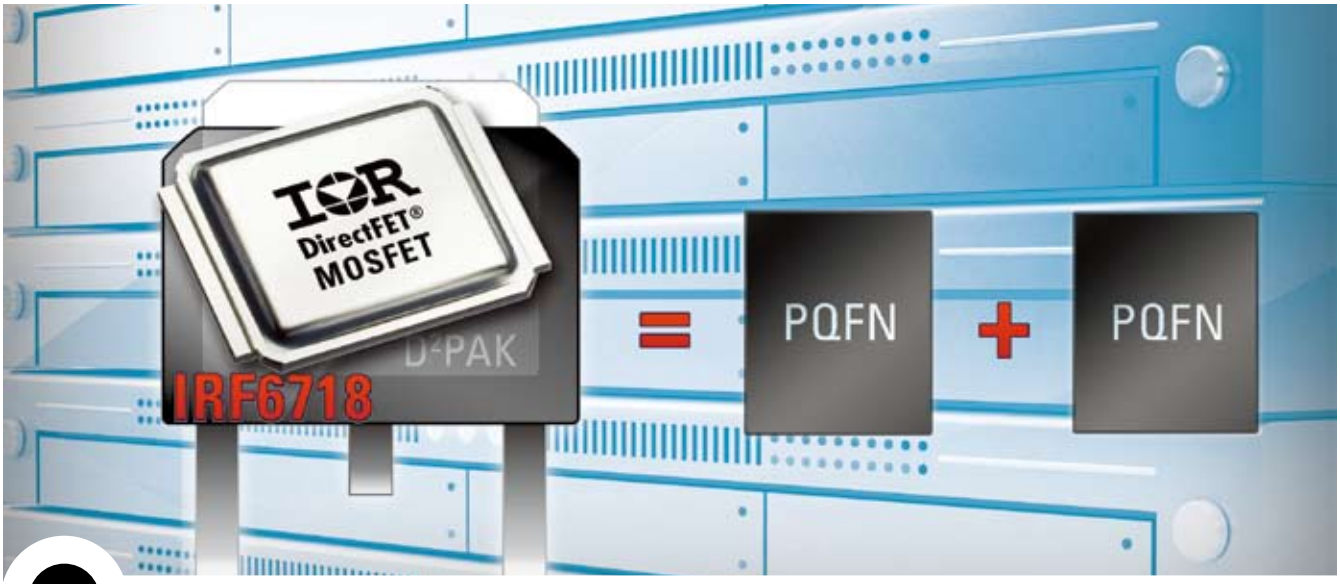
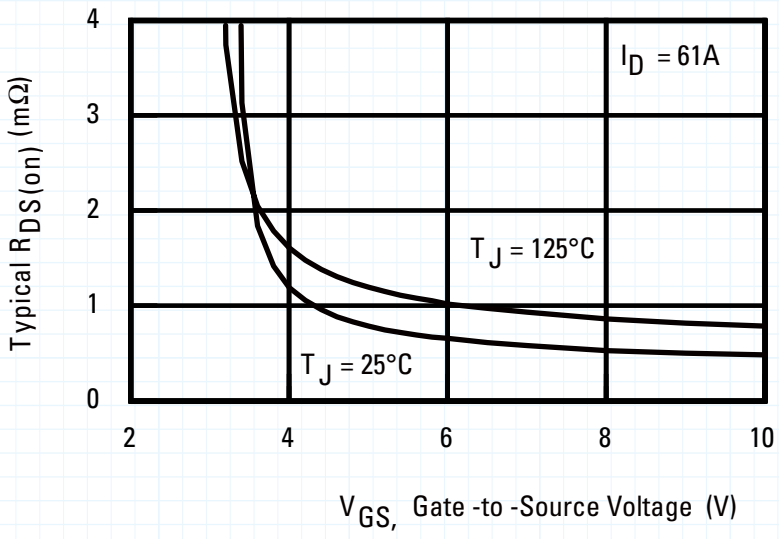




IR's IRF6718 Large Can DirectFET® MOSFET Delivers Industry's Lowest $R_{DS(ON)}$*

Optimized for Active ORing and Hot Swap Applications



The IRF6718L2 features IR's latest generation silicon technology in a new large can DirectFET® package delivering extremely low $R_{DS(on)}$ of only 0.5mOhm (typical) at 10V VGS in a 60% smaller footprint and 85% lower profile than a D²PAK. The IRF6718L2 significantly reduces conduction losses associated with the pass element in ORing or hot swap applications to dramatically improve the efficiency of the entire system.

FEATURES

- Industry Lowest $R_{DS(on)}$ for Reduced Conduction Losses
- Superior electrical and thermal performance in smaller footprint than D²Pak
- Dual-sided Cooling Compatible
- Reduces component count and board space compared to competing solutions
- Compatible with existing Surface Mount Techniques
- RoHS Compliant Containing no Lead or Bromide

Part Number	Package Size (mm x mm)	$R_{DS(on)}$ @10V typ. (mΩ)	I_D @ TA = 25°C (A)
IRF6718	7.1 x 9.1	0.5	270
Competitor 1	10.7 x 15.9	0.7	180
Competitor 2	5.1 x 6.1	0.95	60
Competitor 3	5.1 x 6.1	1.5	65

* Based on data compiled September 2009

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