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March 2011

SPECIAL REPORT: DIGITAL POWER (PG 31)

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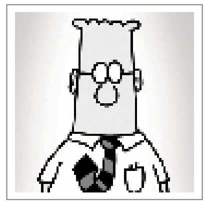

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Volume 8, Issue 2

DIGITAL POWER PARADIGM

Welcome to this issue of PSD where we carry a feature on digital power.First off though, I must let you know about a great new service we have, based on your feedback, to help keep you informed in real-time and to give you the chance to participate. It's our newly-launched community section on our website. Check it out, there's a lot more coming too. Just go to our homepage and click on the community tab on the right.

Going back over the years I remember the focus groups and heated engineering discussions I witnessed, between the analog engineering gurus and the 'new' digital power proponents who were then anxious to utilize their digital skills to do what analog had always done. Visionaries were looking forward to the time when the full advantages of digital power could be harnessed in a way that would not only speed up design cycles such as the control loop compensation, but also be applied more widely at a system level.

Meeting power design specs these days can necessitate the use of complex, high density ICs to provide the differentiated features in products now demanded by the end market. Increasingly, these products can require multiple rails with a corresponding increase in the complexity of system power management. The use of digital power to manage these supplies is becoming increasingly important.

Companies like Zilker Labs, now part of the dynamic Intersil Corporation and expertly steered by its CEO, Dave Bell, have made great strides forward in digital power to show that it is indeed a very useful technology that has successfully been made 'designer friendly' by the development of user friendly GUIs and design tools that take away the fear-factor of entering into a digital power design.

The explosive growth projected for power supplies with digital control and management will increase demand for SiC diodes, DSPs and MPUs according to a report from IMS Research. However, in the long term, this will be at the expense of PFC controller ICs, and analog controllers and regulators. Although supplies with digital control and management are predicted to account for less than 10% of the total merchant market for power supplies in 2015, their components will be worth almost $1 billion. There will be a strong growth in demand for all component types. However, digital controllers/converters are predicted to replace their analog counterparts; and with the use of a DSP or MPU, some functions such as PFC will be performed without a dedicated IC. This will thus impair the demand for some component types.

I hope you enjoy this issue as well as the ongoing improvements to the magazine, website, and community, all based on your valuable feedback. Please keep it coming in. It really helps. And please check out Dilbert at the back of the magazine.

All the best,

Cliff
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Power System Design
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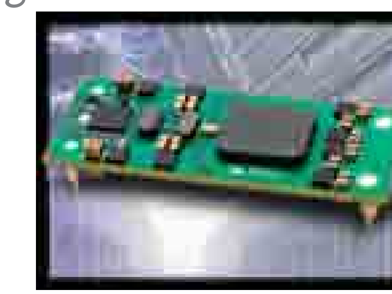
BUS CONVERTERS IN STANDARD PACKAGES

Vicor Corporation has long been the pioneer in the design, development, manufacture, and marketing of modular power components and complete power systems used by OEMs in communications, computing, defense electronics, industrial control, medical, networking, and test equipment markets.



The company's Intermediate Bus Converter (IBC) Module is a very efficient, low profile, isolated, fixed ratio converter for power system applications in enterprise and optical access networks. The IBC conforms to an industry standard eighth brick footprint while supplying the power of a quarter brick. Its leading efficiency enables full load operation at 55°C with only 200LFM airflow, a great advantage in tightly-packed telecom applications where density, efficiency and cooling are premium. Its small cross section facilitates unimpeded airflow - above and below its thin body - to minimize the temperature rise of downstream components.

Vicor has now announced the introduction of the IBC048 series of VI BRICK™ Intermediate Bus Converters, which offer double the power density and half the conversion loss of competitive devices. Available as drop-in replacements for industry standard eighth-brick and quarter-brick 5:1 and 4:1 intermediate bus converters, initial product offerings include 300W and 500W models, providing 9.6V or 12V outputs from a nominal 48V input with a voltage range extending from 38V to 55V.

IBC048-series modules provide pin-compatible upgrades for eighth-brick and quarter-brick bus converters and utilize Vicor's proprietary Sine Amplitude Converter™ engine which is fundamentally different from, and technologically superior to other competing technologies.

The new VI BRICK Bus Converters utilize the same ZCS/ZVS engine that has powered V.I Chips™ into high performance applications with tier-one customers. Switching at approximately 10 times the frequency of competing bus converters, IBC048 modules cut transient response time from 200 to 20 microseconds, eliminating the need for bulk capacitors. Superior density and conversion efficiency enable competitive advantages for OEMs seeking to maximize performance across a range of applications, including computing, data storage, networking and Power-over-Ethernet.

"From pioneering the 'brick' paradigm in the 1980s, Vicor has invested a substantial portion of its revenues in the R&D necessary to architect game-changing innovation in power electronics," said Robert Marchetti, Senior Manager of Product Marketing for Vicor's Brick Business Unit. "With this new product line, we are re-packaging remarkable advances achieved with V.I Chips and applying this superior technology to an established market.

www.vicorpower.com

MAXIM'S DIGITAL POWER PERFECTION

Reported By Cliff Keys

Maxim has dramatically entered the digital power market with its patented InTune technology, and certainly has the capability to become the top supplier of digital power solutions. I had the opportunity to talk with Jim Templeton, Maxim's Director of Business Management on his way back from Europe.

The new technology uses a 'predictive rather than reactive' control, which guarantees stability while achieving the highest possible dynamic performance which can outperform the transient response of analog.

InTune™ technology is based on 'state-space' or 'model-predictive' control rather than proportional-integral-derivative (PID) control used by traditional vendors. InTune performs an automatic compensation routine that is based on measured parameters, which enables the construction of an internal mathematical model of the power supply including the external components. The result is a switching power supply that achieves the highest possible dynamic performance while guaranteeing stability. Furthermore, this information enables several proprietary algorithms that optimize efficiency across a wide range of operating conditions. InTune technology requires up to 5x lower bias current than competing devices, further improving overall efficiency for applications such as networking, telecom, and servers.

Jim explained, "Unlike competing technology, InTune is not an iterative tuning technique. It is deterministic and resolves several limitations present in today's digital power solutions, and unlike PID-based solutions, the InTune loop provides seamless small- and large-signal response without the need to cross back and forth between linear and nonlinear modes. This enables loop response up to 10 times faster than competitors and does not require any user-set thresholds. In fact, InTune PWM controllers are even faster than their analog equivalents."

In addition to internal R&D efforts, the Company has made a key acquisition of a digital power R&D firm and notable university intellectual property. The Company also recently licensed digital power technology 'DPT' patents from Power-One, Inc. Using its new technology and acquisitions, Maxim plans to leverage its position as a top supplier of power-management and control ICs to become the number one supplier of digital power solutions.

"The digital power market has entered the mainstream adoption stage of customer acceptance," said Ryan Sanderson, Senior Market Research Analyst at IMS Research. "Some OEMs report that they now have more than 40 different power supplies on a single PCB. It is no longer practical to rely solely on analog power techniques for these designs. Digital power simplifies design, reduces components, and provides flexibility. IMS estimates that while the digital power IC market accounts for less than 10% of the total market today, it is growing by an average of 30% per year and will amount to over $900 million by 2016."
"Maxim's InTune technology represents the next-generation of digital power," said Wei Tang, Director of R&D at Delta Electronics, Inc. "By providing the best transient response over all operating conditions and enhanced efficiency modes, InTune technology allows us to enable new features, flexibility, and enhanced performance for our power supply customers."

Maxim is building a complete family of digital power products to complement its full offering of analog power ICs. The first InTune chips are currently sampling with partner customers; individual product announcements will follow in the coming months.

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WILL DIGITAL POWER IMPACT ANALOG IC MARKETS?

By Ryan Sanderson

Following an extremely tough time during the global recession, 2010 was an outstanding year for semiconductor manufacturers, with many reporting the highest growth they have seen for a decade. The global semiconductor industry grew by over 30% and recovery occurred in all major market sectors. Now into the first quarter of 2011, most of the capacity shortages seen in 2010 seem to have been resolved and inventories are being replenished.

The key question now is whether market growth can be sustained and how it will differ by semiconductor product type. One area which seems destined for high growth for the foreseeable future is digital power. What is unclear, however, is how much of an impact this will have on existing analog markets.

Recent analysis from IMS Research showed that the global power management and driver IC market grew by more than 35% in 2010, leaving manufacturers of analog and digital power ICs in high spirits. The digital control and conversion IC market however, grew faster in 2010 (around a 50% increase). This followed low single-digit growth in 2009, when the total power IC market declined by over 14%. Our longer-term growth projections for the digital control and conversion IC market are on average 20% higher than those for the analog power IC market.

With a total market in 2010 of over $4.5 billion for switching regulators and controllers, digital controllers and converters still only accounted for less than 5% of this, despite their recent growth. Existing opportunities are still largely limited to infrastructure and datacom equipment such as high-end servers, routers and base stations, all at the OEM or board level, though the penetration of digital controllers into merchant power supplies is growing. Whilst strong growth is projected over the next 5 years as penetration into more applications occurs, driving a digital power IC market of close to $600 million, the digital control and conversion market is still forecast to account for less than 10% of the total switching regulation and control market in 2015.

Having said this, the full impact on other markets is not always clearly visible. For example, we also recently performed a detailed analysis of the components market within merchant power supplies. Strong growth is projected for power supplies with digital control and/or management, driving an associated total component market of close to $1 billion in 2015. One of the benefits of digital solutions in power supply design is the ability to reduce the component count, often by replacing existing functions by using a DSP or microprocessor. In most cases this simply reduces the number of passive components required. However, increasingly, designs are using the processor for functions such as power factor correction (PFC), replacing a dedicated PFC controller IC, or for driving other components which would typically use a dedicated driver IC. Of all the power supplies shipped with PFC in 2010, solutions using a processor in place of a dedicated PFC controller IC accounted for just 1% but this is projected to grow strongly over the next five years.

The picture therefore seems clear. There is a substantial future threat to analog power IC technology. There is already strong competition from non-mainstream analog competitors such as Volterra, Microchip and Chil Semiconductor. As the transition to digital solutions gains momentum, IMS Research believes that more of the analog industry powerhouses will need to develop products in the digital market space, or accept that they will start to lose overall power IC market share.

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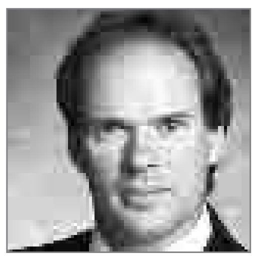
POWER SUPPLY DEVELOPMENT DIARY

Part XI



By Dr. Ray Ridley

This article continues the series in which Dr. Ridley documents the processes involved in taking a power supply from the initial design to the full-power prototype. Part X of this series of articles presented the first five rules for good PC board layout. Part XI concentrates on the sixth and seventh rules, which are concerned with the routing of high-frequency currents.

PCB Layout Rule 6: Keep High-Frequency Current Loops Small

Switching power supplies generate high-frequency waveforms with both high-current and high-voltage pulses. These waveforms generate a broad spectrum of frequency components for square-wave converters. If the PC board is not laid out properly, the high-frequency currents can create numerous problems, including large stray inductances with associated energy storage, increased component stresses, and EMI issues that are very difficult to suppress.

These problems can be controlled by following the sixth rule of good PCB layout: Keep high-frequency current loops as small as possible. This requires careful thought regarding circuit functioning and board layout.

Figure 1 shows the basic schematic of the forward converter with a single output.

When the power switches are turned on, a high-frequency pulse of current flows through components C1, T2, Q1, T1, and Q2. A corresponding pulse of current flows through the secondary of the transformer, and the forward diode.

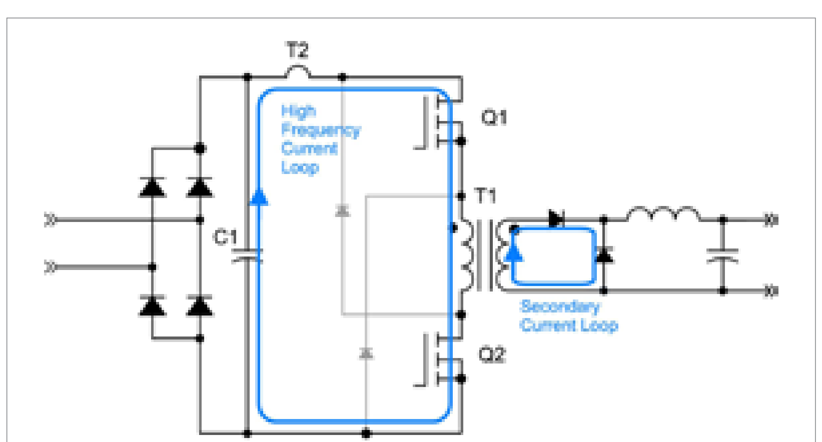


Figure 1: Forward Converter Schematic with High-Frequency Primary Current Path

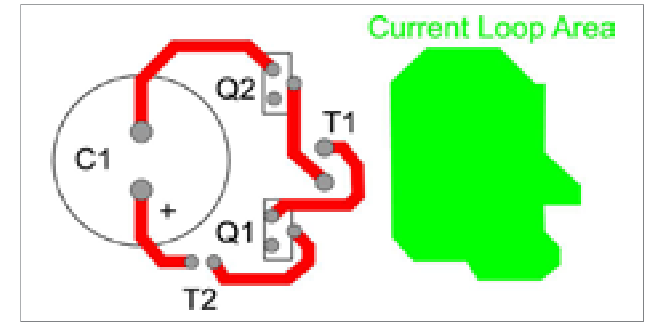


Figure 2: Forward Converter Primary Component Layout on a Single Layer.

It is important that the loop containing these components presents a low inductance. Figure 2 shows the placement of the primary components, and a preliminary layout of the board. In this example, all of the traces are placed on the upper layer and shown in red. This facilitates the testing of the power supply, and is useful for a single-sided board. Attention has been paid to ensure that the traces are well separated for voltage breakdown considerations.

However, the layout of the primary in this example creates a large current loop area, shown in green. This large area results in increased inductance, and a single turn antenna that will radiate EMI that is difficult to suppress. The severity of the problem will depend upon the current levels. Even at low power and current levels, however, these large-area current loops should be avoided.

A similar problem exists on the secondary side of the transformer. For step-down converters, secondary currents are higher and the layout of the secondary is even more crucial. The issues are the same. The illustration of secondary layout is not shown in this article.

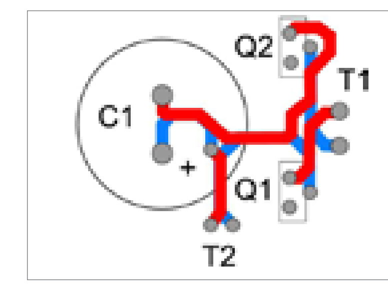


Figure 3: Forward Converter Primary Layout on Two Layers.

Figure 3 shows how the primary layout can be improved by using both layers of the PC board. In this case, the top (red) and bottom (blue) layers are used to carry opposing currents, thus providing cancellation of magnetic fields. This is the optimal situation from the standpoint of minimizing inductance, energy storage, and EMI. To achieve this, some of the board spacings are not as large as we would like to see.

Also, the presence of multiple traces on both layers restricts the flexibility of component placement on the underside of the board. This will impact the performance of other parts of the primary circuit, specifically the effectiveness of the clamp diodes.

Figure 4 shows an alternate arrangement where there is a compromise between minimum loop area, keeping the bottom layer of the board mostly free of traces. In this case, there is at least a 4:1 reduction in current loop area compared to the first layout, while maintaining acceptable voltage spacing.

The layout of Figure 4 now lets us design a good layout for the next phase of the primary operation, shown in Figure 5. When the power switches turn off, the primary current flows through the two diodes. One purpose of these diodes is to reset the magnetizing current in the primary of the transformer. This is a

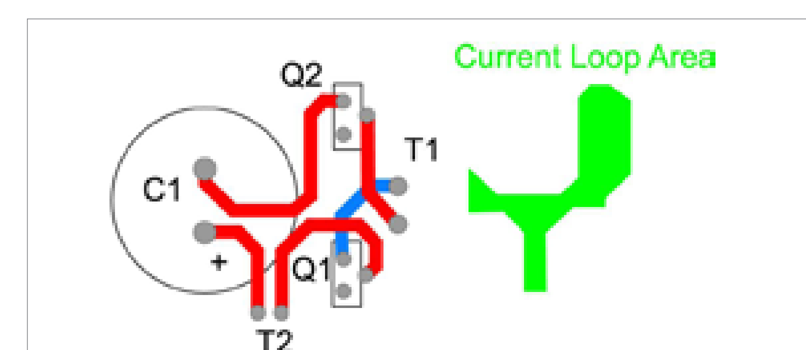


Figure 4: Primary Layout with Small Loop Mostly on Top Layer.

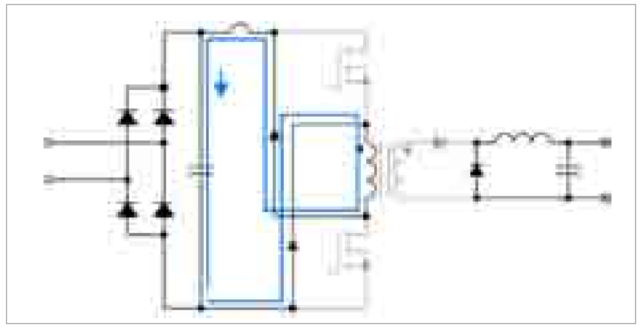


Figure 5: Forward Converter Schematic with High-Frequency Primary Diode Current Path

relatively low current. However, the diodes also provide a clamp for the power devices, and the path through these diodes must be kept as short as possible to avoid excessive voltage spikes caused by the transformer leakage inductance. Proper layout of these parts saves us having to use additional bypass components on the primary of the converter.

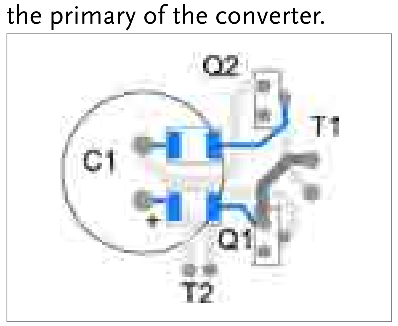


Figure 6: Primary Clamp Diode Layout.

Figure 6 shows the placement and traces for the clamp diodes. The previous top and bottom traces are now shown in grey for clarity, and the diode traces and pads are on the bottom of the board in blue.

Layout Rule 7: Show the Currents Where to Flow

In closing the current loops as shown so far, we are also following Rule Number 7 of good layout: Show the currents where to flow.

The high-frequency currents of a converter must be given only one path to follow to ensure predictable performance. In some cases, there may be multiple connections to a circuit node, but the high current paths must be explicitly laid out.

An example of this is shown in Figure 7 for the gate drive connections to the primary power switches. Gate drive layout is important for several reasons. Firstly, high currents are sometimes needed to switch FETs rapidly, and these can create EMI if the current loops of the gate drive are not closed. Secondly, it is important that the main power currents do not affect the gate drive waveforms due to poor layout.

In Figure 7, it is shown that the returns of the gate drive traces go directly to the source of the power FETs, and not to some other part of the same circuit node. This prevents the power currents from flowing through the gate drive circuit.

Ideally, the gate drive signals flow on opposite sides of the PC board. However, with a two-layer board, this is not always possible. In Figure 7, the left hand gate traces are both on the bottom of the

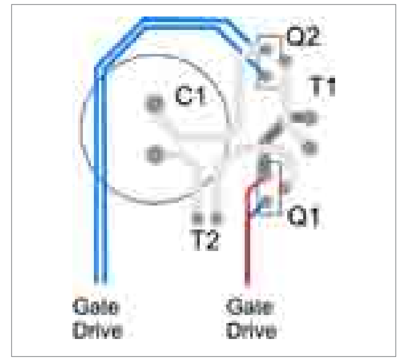


Figure 7: Primary Gate Drive Layout.

board, but with small separation since there is not a large voltage differential between the traces.

Summary

The last few articles have shown seven of the nine critical rules for good PC board layout. Considerable time must be spent on the board layout as this can eliminate later problems with component stresses, proper circuit operation and EMI. The engineer who is intimately familiar with every detail of the circuit operation must be closely involved with the actual board layout, down to the very detailed placement of parts, and proper routing of traces to satisfy multiple simultaneous requirements. This is not a process that can be left to a PCB designer without power experience.

In the final part of this series regarding PCB layout, the proper use of ground and EMI shielding planes will be discussed.

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SYSTEM MANAGEMENT DESIGN

Digital power reduces data center power consumption

By Bruce Haug

Digital power has been hyped by many companies for several years and some consider digital power to be comprised of digital functions and a communications link with a power supply.

Several other companies in the industry say that digital power is a state machine with a built-in chip featuring digital pulse width modulation (PWM). Still others state that it includes a general-purpose digital signal processor (DSP) running an algorithm that closes a control loop and the mere existence of a serial bus does not provide a digital power solution. Even others state that digital power has a digital PWM loop with either a state machine or a DSP.

All of these descriptions can be very confusing and some of these methods do not produce good performance. But, when digital power is done correctly, it can reduce data center power consumption, shorten time to market, have excellent stability and transient response, and increase overall system reliability such as in networking equipment.

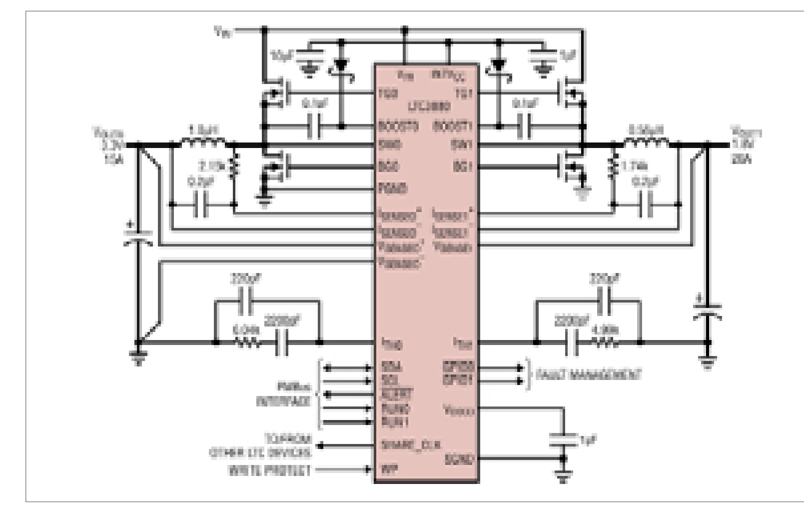

Figure 1: Application Schematic with 2 High Current Outputs Using the LTC3880

System architects of networking equipment are being pushed to increase the data throughput and performance of their systems as well as add functionality and features. At the same time, pressure is being applied to decrease the systems overall power consumption. In data centers, the challenge is to reduce overall power consumption by rescheduling the work flow and moving jobs to underutilized servers, thereby enabling shutdown of other servers. To meet these demands, it is essential to know the power consumption of the end-user equipment. A properly designed digital power management system can provide the user with power consumption data, allowing for smart energy management decisions to be made.

The status of a voltage regulator is perhaps the last remaining "blind spot" in today's modern electronic systems, since they are normally without the means for directly configuring or remotely monitoring key operating parameters. It can be critical for reliable operation that a regulators output voltage drift over time or an over temperature condition be detected and acted on. A well designed Digital Power System Management (DPSM) can monitor the performance of a voltage regulator and report back on its health in order to take corrective action prior to it going out of specification or even failure.

The use of DPSM for voltage regulators and power supply design require that engineers go through a learning curve of how to program and interface these types of devices through a graphical user interface (GUI) on a computer. This includes learning new programming software and each company providing digital power devices has their own software package. As a result, it is important to select a company which has a well thought out and user friendly software package and GUI. In addition, the company should have a well established technical support staff that has the bandwidth to assist in the design of these types of power supplies.

Multirail Board Level Power System

Most embedded systems are powered via a 48V backplane. This voltage is normally stepped down to a lower intermediate bus voltage of typically 12V to 3.3V to power the racks of boards within the system. However, most of the sub-circuits or ICs on these boards are required to operate at voltages ranging from sub-1V to 3.3V at currents ranging from tens of milliamps to hundreds of amps. As a result, point-of-load (POL) DC/DC converters are necessary to step down from the intermediate bus voltage to the desired voltage required by the sub-circuits or ICs. These rails have strict requirements for sequencing, voltage accuracy, margining and supervision.

There can be as any many as 20 POL voltage rails in a datacom, telecom or storage systems and system architects need a simple way to manage these rails with regards to their output voltage, sequencing and maximum allowable current. Certain processors demand that the I/O voltage rises before the core voltage, alternatively certain DSPs require the core voltage to rise before the I/O voltage. Power down sequencing is also necessary. Designers need an easy way to make changes to optimize system performance and to store a specific configuration for each DC/DC converter in order to simplify the design effort.

In order to protect expensive ASICs from the possibility of an over voltage condition, high-speed comparators must monitor the voltage levels of each rail and take immediate protective action if a rail goes out of its specified safe operating limits. In a digital power system, the host can be notified when a fault occurs via the PMBus alert line and dependant rails can be shut down to protect the powered devices such as an ASIC. Achieving this level of protection requires reasonable accuracy and response times on the order of tens of microseconds.
The recently announced LTC®3880/-1 from Linear Technology provides highly accurate digital power system management with its high resolution programmability and fast telemetry read-back for real-time control and monitoring of critical point-of-load converter functions. It is a dual output high efficiency synchronous step-down DC/DC controller with I2C-based PMBus interface with over 100 commands and onboard EEPROM. The device combines a best in class analog switching regulator controller with precision mixed signal data conversion for unsurpassed ease of power system design and management, supported by the LtpowerPlay™ software development system with easy-to-use GUI. Figure 1 shows a typical LTC3880 application schematic.

The LTC3880/-1 can regulate two independent outputs or be configured for a two phase single output. Up to 6 phases can be interleaved and paralleled for accurate sharing among multiple ICs, minimizing input and output filtering requirements for high current or multiple output applications. An onboard differential amplifier provides true remote output voltage sensing. Integrated gate drivers power all N-channel power MOSFETs from input voltages ranging from 4.5V to 24V and it can produce ± 0.50% accurate output voltages up to 5.5V with output currents up to 30A per phase over the full operating temperature range. The LTC3880/-1 can also be used with power blocks and DRMOS devices. Accurate timing across multiple chips and event-based sequencing allow the optimization of power-up and power-down of complex, multiple rail systems. The LTC3880 features an onboard LDO for controller and gate drive power and the LTC3880-1 allows for an external bias voltage for highest efficiency. Both parts are available in a thermally enhanced 6mm x 6mm QFN-40 package.

Control Interface for Digital Power System Management

The PMBus command language was developed to address the needs of large multirail systems and is an open standard power-management protocol with fully defined command language that facilitates communication with power converters, power management devices and system host processors. In addition to a well defined set of standard commands, PMBus compliant devices can also implement their own specialized commands to provide an innovative approach to programming and monitoring POL DC/DC converters. The protocol is implemented over the industry standard SMBus serial interface and enables programming, control, and real-time monitoring of power conversion products. Command language and data format standardization allows for easy firmware development, resulting in reduced time-to-market. For more information, see http://pmbus.org

The LTC3880/-1 programmable control parameters include output voltage, margining, current limits, input and output supervisory limits, power-up sequencing and tracking, switching frequency, identification and traceability data. On-chip precision data converters and EEPROM allows for the capture and nonvolatile storage of regulator configuration settings and telemetry variables, including input and output voltages and currents, duty cycle, temperature and fault logging.

Table 1 shows some parameters that can be programmed with the LTC3880/-1, its high resolution, the telemetry read-back capability and alternative solutions. Configurations for the LTC3880/-

Programmable Control Resolution/Accuracy		
Parameter	LTC3880/-1	Competitive Alternative
V_{OUT} Command	13-bit, ±0.5%	6-bit, ±3%
V_{IN} Supervisor	8-bit, ±2%	6-bit, ±3%
OV & UV Supervisor	8-bit, ±2%	6-bit, ±3%
Current Limit	3-bit, ±5mV	2-bit
Telemetry Read-Back Resolution/Accuracy		
Parameter	LTC3880/-1	Competitive Alternative
V_{OUT} Reading	15-bit, ±0.5%	12-bit
Output Current	15-bit, ±1%	12-bit

Table 1: Some of the LTC3880/-1 Programmable Parameters& Telemetry Read-Back Capability & Accuracy Using the LTC3880

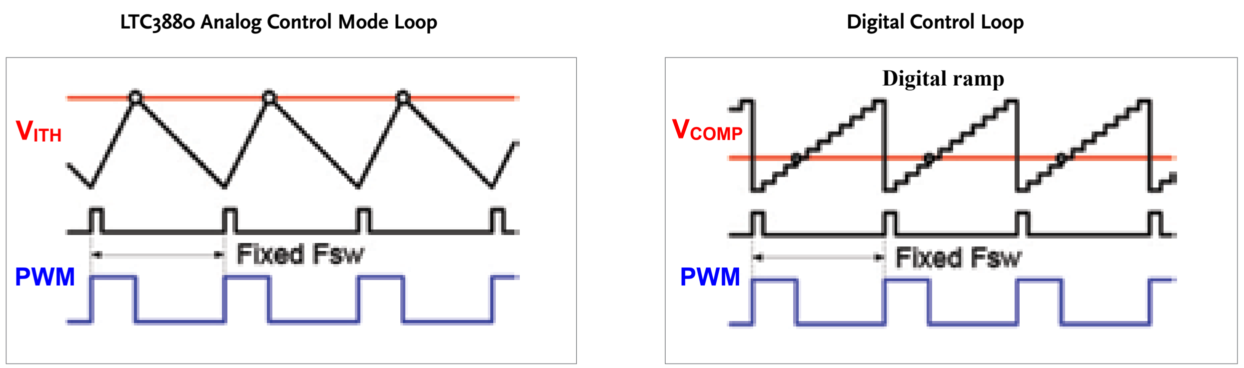

Figure 2: LTC3880's Analog Control Loop vs. a Digital Control Loop

1 are easily saved to internal EEPROM over the device's I2C serial interface. With configurations stored on-chip, the controller can power up autonomously without burdening the host processor. Default settings can be optionally configured by external resistor dividers for output voltage, switching frequency, phase and device address. Multiple designs can be easily calibrated and configured in firmware to optimize a single hardware design for a range of applications.

Analog Control Loop

The LTC3880/-1 is a digitally programmable DC/DC controller for numerous functions like the output voltage, current limit set point, and sequencing to name a few, but it has an analog feedback control loop for best loop stability and transient response without the quantization effect of a digital control loop.

Figure 2 shows the different ramp curves within a controller IC with an analog feedback control loop and with a digital feedback control loop. The analog loop has a smooth ramp, whereas the digital loop is like a step function that can result in stability problems, slower transient response, the need for more output capacitance in some applications and a quantization effect of the digital loop resulting in a higher output ripple. One of the benefits of the LTC3880's analog control loop is that it can use 50% less output capacitance as compared to digital control loop alternative and have better stability with a shorter settling time. In addition, the digital control transient response has an oscillation prior to settling, due to the quantization effects and limitation of its ADC resolution. Figure 3 shows a transient response comparison of an analog control loop to a digital control loop.Furthermore, a digital control loops quantization effect, due to the ADC, digital compensator and digital PWM adds additional voltage to the output ripple, depending on the ADC's resolution and loop design. By contrast, an analog control loop does not have this additional output ripple voltage.

Figure 3: Transient Response Comparison of Analog Loop vs. Digital Control Loop with 25A Load Step, for a 12VIN to 1.2VOUT DC/DC Converter Operating at 400kHz.

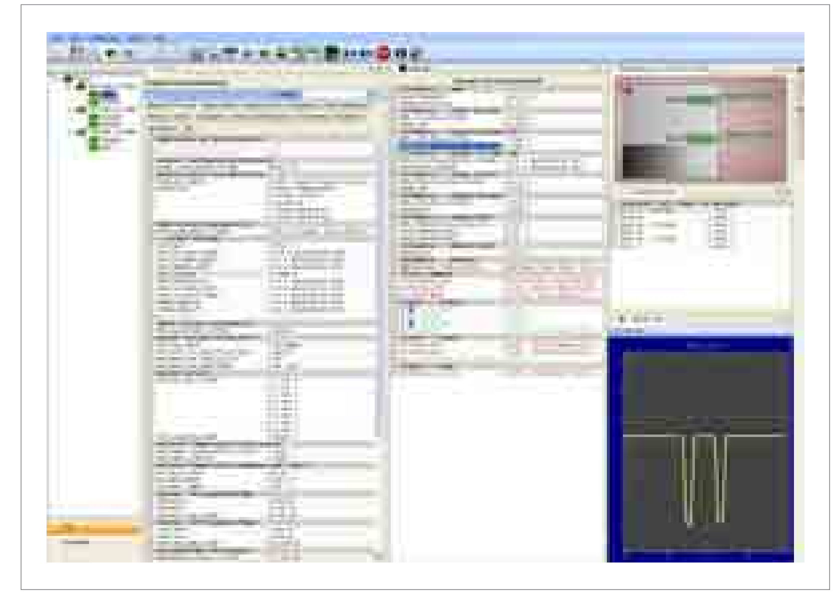

Figure 4 – LTpowerPlay's GUI Screen Shot

Programming LTpowerPlay Software and GUI

The LTC3880 is supported by the LtpowerPlay software development system with easy-to-use GUI. The GUI screen shot shown in Figure 4 illustrates how several functions are controlled, such as the output voltage, protection limits, on/off ramps and a few waveforms including the sequencing of multiple rails and telemetry plots.

This powerful GUI software is available from Linear Technology's web site for free and works in conjunction with other Linear Technology converters and supervisory parts in order to quickly and easily develops high count voltage rail systems.

Conclusion

One of the principal benefits of digital power is the potential to predict power system failures and enable preventive measures, thanks to the availability of real-time telemetry data. Perhaps most significantly, DC/DC converters with digital management functionality allow designers to develop 'green' power systems that meet target performance with the ability to determine when to reduce overall power consumption by rescheduling the work flow and moving jobs to underutilized servers, thereby enabling shutdown of other servers. With minimum energy usage at the point of load, board, rack and even installation levels, helps reduce infrastructure costs and the total cost of ownership over the life of the product.

Another benefit of digital power system management is reduced design cost and faster time to market. Complex multi-rail systems can be efficiently developed using a comprehensive development environment with intuitive GUI. Such systems also simplify in-circuit testing (ICT) and board debug by enabling changes via the GUI instead of soldering fixes.

Digital power has become very confusing as to what it is and what are its benefits. As a result, potential users of digital power need to do their due diligence with regards to what they want to achieve and if the benefits of DPSM are right for their products and customers. They need to make sure that the company they select has high performance analog devices, a well established and easy to use software package and a well educated technical support staff that is willing to assist. Fortunately, such companies exist.

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PV OFF-THE-ROLL

Barrier film for thin-film solar cells

By Dr. Florian Schwager

Thin-film solar cells are developing into a rapidly growing market segment. If their commercial potential is to be fully exploited, the solar modules must be produced in a roll-to-roll manufacturing process. Evonik has now developed the "missing link" necessary for continuous production: a highly transparent and also weathering-resistant barrier film based on PLEXIGLAS® that can replace glass plates as a front cover.

Photo by Solarion AG

Flexible copper indium gallium diselenide (CIGS) thin-film solar cells from Solarion AG, headquartered in Leipzig. Established in the year 2000, the company started up in 2002 the first industrial pilot line in Europe for production of high-flexibility ultralight CIGS thin-film solar cells on a polymer substrate. An industrial scale manufacturing plant is currently constructed. CIGS technology achieves higher efficiencies compared with amorphous silicon technology, but requires superior barrier properties in the encapsulating material. Most of the solar modules to be found on roofs in Germany today contain crystalline solar cells, for which the light sensitive semiconductor layers are produced from silicon wafers. The technology is now well understood: Modules of crystalline solar cells have lifetimes of 25 to 30 years and attain efficiencies averaging 16%.

In these modules the solar cells, which are soldered to one another, are embedded in a thermally curing polymer that protects them from excessive mechanical stress. This is backed by an electrically insulating and weathering-resistant film, and at the front a glass plate shields the cells in the modules from environmental effects.

A module of this type, typically measuring 1.5m x 1m, weighs about 20kg. Mono- or polycrystalline solar cells have thicknesses between 150 and 300 micrometers but the upper 10 micrometers absorb the incident light; a better solution is offered by thin-film solar cells, which are about 100 times thinner than the wafer-based cells. These are made from a variety of materials such as amorphous silicon (a-Si), cadmium telluride (CdTe), and copper indium (gallium) selenide/sulfide (CIGS/CIS). At present they attain module efficiencies of only about 11% at most, but they have the advantage that they can be manufactured in a continuous roll-to-roll process that is highly cost efficient compared to crystalline solar cell production, which, in the tradition of the semiconductor industry, is a batch process.

If the barrier film protecting the solar cells from environmental effects is of plastic rather than glass, flexible and therefore cost efficient thin-film solar cells can be realized with a number of semiconductor materials. (CSG = cristalline silicon on glass, a-Si = amorphous silicon, μc-Si = microcristalline silicon, DSSC = dye sensitized solar cell; OPV = organic photovoltaics)

But there's one obstacle in thin-film solar cell production: Until now, the producer has had at some stage to convert the continuous process to a batch process because no suitable barrier films are available that protect the solar cells from harmful environmental effects over the long term. This means that, with only a few exceptions, even modules with flexible thin-film solar cells have glass plates on the front, and with glass no continuous production process is possible. While thin-film solar modules in the form of roll material do exist, the ethylene tetrafluoroethylene (ETFE) film used does not provide adequate barrier properties; it allows water vapor and oxygen to pass through largely unhindered, so that corrosion effects reduce the service life of the cell.

Given this situation, the industry is interested in a suitable covering film that has the same properties as glass as far as possible and can be integrated into a continuous, and therefore more cost effective, production process. Organic solar cells, which consist of conjugated semiconducting polymers and are currently being intensively investigated, would also benefit from film technology of this kind because they have the additional advantage of being easily printed and can therefore be produced in a roll-to-roll process.

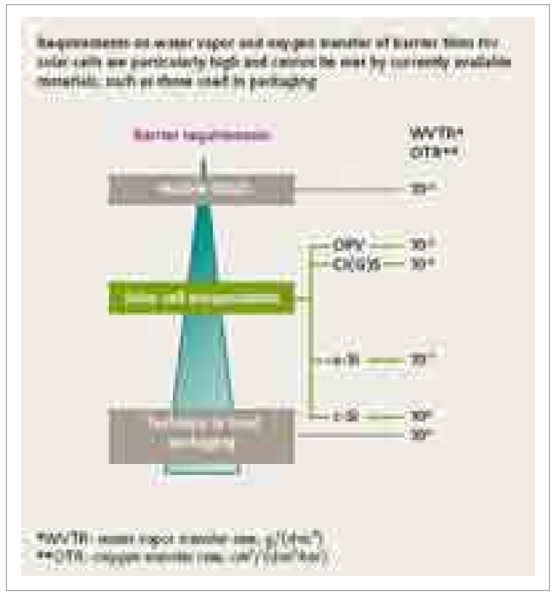
At this point, researchers of Evonik's Functional Films & Surfaces Project House took up the challenge: Why not, they asked, use the Group's polymer expertise to develop a suitable polymer film? This would have to act as a barrier to water vapor and oxygen, allow high light transmission, adhere well to solar cells, and be electrically insulating, flexible, and cost efficient. It should also have high weathering and UV resistance. In short, this would mean developing an entirely new system solution for the photovoltaics industry.

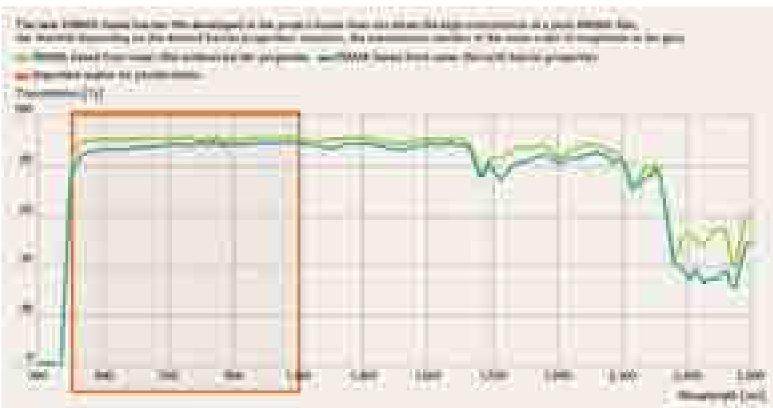
Poly (methyl methacrylate) (PMMA) has many of the required properties such as high transparency, weathering resistance, and UV stability. Initial trials in the project house, which is managed by Evonik's strategic research unit Creavis Technologies & Innovation, were therefore carried out with a film based on PLEXIGLAS® molding compound, which the researchers coated with an inorganic oxide film as a barrier, using a sputter process. The results were disappointing, however: The film could not withstand the sputter process and the barrier requirements could not be met.

Requirements on water vapor and oxygen transfer of barrier films for solar cells are particularly high

and cannot be met by currently available materials, such as those used in packaging.

The new PMMA-based barrier film developed in the project house does not attain the high





Material properties of the barrier film developed in the project house

Material properties	Specification value
WVTR [g/(m²d) at 23 °C, 85 % relative humidity]	[illegible]
OTR [cm³/(m²d·bar) at 23 °C, 50 % relative humidity]	[illegible]
Partial discharge voltage [V]	> 1,000
Transmission [% at 400-1,200 nm]	88 – 90*
Damp heat test [h at 85 % relative humidity, 85 °C]	> 1,000
UV-A/UV-B test [h at 15 kwh/m²]	> 1,000
Adhesion to EVA-fc [N/cm]	> 20

* Depending on product design

transmission of a pure PMMA film, the shortfall depending on the desired barrier properties; however, the transmission remains of the same order of magnitude as for glass.

Composite film provides required properties

Further investigation and tests, for which the project participants also drew inspiration from packaging industry technologies, resulted finally in a multilayer film with the required barrier properties. Water vapor and oxygen permeability– the yardstick for barrier properties–in the thinfilm solar cells need to be one to three orders of magnitude lower than in conventional packaging films. The multilayer film consists of several functional and bonding layers and an outer PMMA layer. The PLEXIGLAS® protects the underlying layers of the film very efficiently against the effects of weathering, thus ensuring the necessary longevity.

In the spectral range relevant to

photovoltaics, Evonik's new film achieves transmission rates of 88 and 90% in the short-wave and long-wave regions; these figures are comparable to those for glass plates. The film is currently being put through weathering tests at the Fraunhofer Institute for Solar Energy Systems in Freiburg (Germany), which exceed the requirements of the IEC 61646 standard for thin-film solar cells. The tests expose the laminated film to strong temperature fluctuations, UV radiation, high humidity, and mechanical loads such as arise from hail, snow, and wind. It is already clear that the multilayer film will more than satisfy the standard in regard to the damp heat test and UV resistance.

The new specialty film is now available off the roll in widths of up to 1.2 meters. The first customers are already testing the film for use in their flexible thin-film solar modules. The project having been successfully wound up in Creavis's Functional Films & Surfaces Project House, its activities are now continued in the Performance Polymers Business Unit.

Photo Centrosolar AG

The TF plate flexible module from Centrosolar AG, Paderborn, is a solar roofing system for large and industrial roofs with a nominal output of 288Wp. The solar power plates are based on thin-film laminates bonded to polymer-coated steel sheeting, and can for example be mounted on trapezoidal sheet metal. The solar roofing system contains thin-film cells with triple-junction technology from United Solar Ovonic, so that excellent yields are obtained even for unfavorable roof alignments or angles. Triple-junction technology is based on amorphous and microcrystalline silicon that is relatively resistant to environmental effects and can therefore be encapsulated with the polymer films currently available on the market.

Attractive growth market

Thin-film solar cells and modules will soon develop into the fastest growing segment in photovoltaics because of their low weight; they weigh less than a third than crystalline silicon solar modules.

- Flat roofs, which for structural reasons cannot currently be used as supports for the heavy, rigid, solar modules.
- The automotive sector - integrated into roofs and tarpaulins of passenger cars, trucks, and buses.
- The consumer electronics industry is also becoming increasingly interested in flexible solar cells to make the increasing number of mobile devices–cell phones, smartphones, notebooks, etc.–less dependent on mains power

Even hand-held bags or backpacks with integrated flexible thinfilm solar cells on the outside are no longer the stuff of science fiction, and are indeed already available on the market.

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GROUNDING TRANSFORMERS

Why a wind farm's success depends on them

By Curt Collins

The grounding transformer is an often neglected component of the wind farm – shunted off to a sidebar issue. However, those who neglect to adequately plan for grounding transformers do so at their peril.

In reality, millions of dollars in liability and loss can be attributed to ground-fault arcing, so grounding-related issues should top the checklists of any electrical contractor developing a wind farm.

Proper construction to meet the specific needs of wind farms is absolutely essential. In addition, be sure your grounding transformer considers such essential parameters as primary voltage, size needed to carry the rated continuous primary phase current without exceeding temperature limits, and fault current and duration. Finally, select from among the variety of options available based on the application's site-specific needs.

What is a grounding transformer and why is it needed on wind farms?

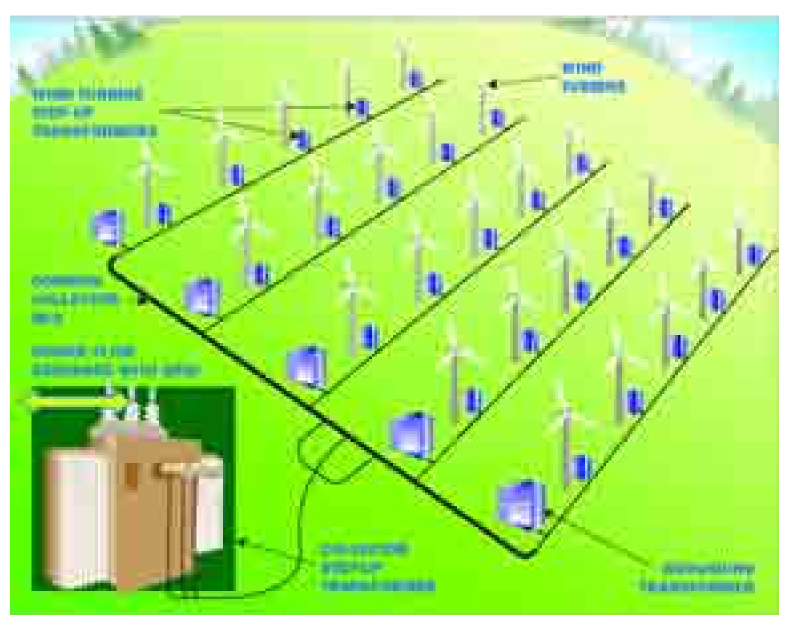

Figure 1 – Typical wind farm configuration

Simply put, a grounding transformer is used to provide a ground path to either an ungrounded Wye or a delta-connected system. Grounding transformers are typically used to:

- Provide a relatively low impedance path to ground, thereby maintaining the system neutral at or near ground potential.
- Limit the magnitude of transient over voltages when re-striking ground faults occur.
- Provide a source of ground fault current during line-to-ground faults.
- Permit the connection of phase to neutral loads when desired.

If a single line-to-ground fault occurs on an ungrounded or isolated system, no return path exists for the fault current, so no current flows. The system will continue to operate, but the other two un-faulted lines will rise in voltage by the square root of 3, resulting in overstressing of the transformer insulation and other associated components on the system by 173 percent. Metal Oxide Varistors (MOVs), solid state devices used to suppress voltage surges/spikes (lightning arresters), are particularly susceptible to damage from heating by leakage across the blocks even if the voltage increase is not sufficient to flash over. A grounding transformer provides a ground path to prevent this.

Grounding transformers are essential for large multi-turbine wind farms, where the substation transformer frequently provides the sole ground source for the distribution system. A grounding transformer placed on the turbine string provides a ground path in the event the string becomes isolated from the system ground.

When a ground fault on a collector cable causes the substation circuit breaker for that cable to open, the wind turbine string becomes isolated from the ground source. The turbines do not always detect this fault or the fact that the string is isolated and ungrounded, the generators continue to energize the collector cable, and the voltages between the un-faulted cables and the ground rise far above the normal voltage magnitude. The resulting costs can be staggering. The loss of revenue alone for a string of 10 turbines can exceed $10,000 per day. Considering removal and replacement, costs of equipment could approach an additional $40,000 per transformer.

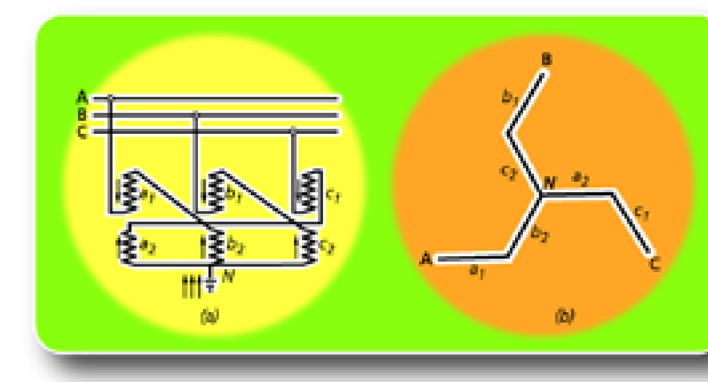

Figure 2 – Grounding transformer configurationsconfiguration

For example, a typical wind farm configuration is somewhat analogous to a carriage wheel with a ring, hub and spokes. The wheel's outer ring is like the fence around the wind farm and the hub in the center is where the collector is located, which connects to the grid. The spokes are radial lines where each wind turbines sit. Typically each radial string of turbines will connect to a grounding transformer. Figure 1 provides a generalized diagram of this layout.

Proper grounding transformer construction

Grounding transformers are normally constructed with one of two configurations: a Zig-Zag (Zn)-connected winding with or without an auxiliary winding, or a Wye (Ynd)-connected winding with a delta-connected secondary that may or may not be used to supply auxiliary power. Figure 2 shows these two possible configurations. The current trend in wind farm designs is toward the Wye-connected primary with a delta secondary (b). There are several reasons why the 2-winding Wye-connected grounding transformers are seemingly more popular than Zig-Zag designs.

- Though not actually the case, 2-winding transformers are perceived to be more readily available for replacement or upgrade.

- Lack of familiarity with the design basics required for the Zig-Zag configuration means designers tend to fall back on the more familiar configuration.
- The Wye-connected 2-winding design allows for secondary loading and metering while Zig-Zag designs do not.
- Not all manufacturers provide Zig-Zag grounding options to potential customers, even those for whom that configuration might be most appropriate.

The Zig-Zag connection's geometry (a) is useful to limit circulation of third harmonics and can be used without a delta-connected winding or the 4- or 5-leg core design normally used for this purpose in distribution and power transformers. Eliminating the need for a secondary winding can make this option both less expensive and smaller than a comparable two-winding grounding transformer. Furthermore, use of a Zig-Zag transformer provides grounding with a smaller unit than a two-winding Wye-Delta transformer providing the same zero sequence impedance.

Wye-connected grounding transformers, on the other hand, require either a delta-connected secondary or the application of 4- or 5-leg core construction to provide a return flux path for unbalanced loading associated with this primary connection. Since it is often desirable to provide auxiliary power from the grounding transformer secondary winding, this benefit may make it preferable to use a two-winding grounding transformer instead of a Zig-Zag connection. Both Zig-Zag and two-winding grounding transformers can be constructed with auxiliary power capabilities, and this can be either a Wye- or delta-connected load.

A solidly grounded system using a grounding transformer offers many safety improvements over an ungrounded system. However, the ground transformer alone lacks the current limiting ability of a resistive grounding system. For this reason, neutral ground resistors are often used in conjunction with the grounding transformer to limit neutral ground fault current magnitude. Their ohm values should be specified to allow high enough ground fault current flow to permit reliable operation of the protective relaying equipment, but low enough to limit thermal damage.

Key parameters

When selecting and specifying a grounding transformer for your wind farm, be sure to consider the following key parameters:

Primary voltage – This is the system voltage to which the grounded winding is to be connected. Don't forget to specify the transformer's basic impulse level (BIL), which measures its ability to withstand lightning surges. In some cases the BIL will be dictated by equipment considerations, such as 150 kilovolt (kV) BIL ratings on 34500 volt wind farms because of the limitation on dead front connectors.

Rated kilo-volt amperes (kVA) – Because the grounding transformer is normally a short time device, its size and cost are less compared to a continuous duty transformer of equal kVA rating. For this reason, grounding transformers are often not sized by kVA, but by their continuous and short time current ratings. Regardless of how you rate it, the grounding transformer must be sized to carry the rated continuous primary phase current without exceeding its temperature limit. This load includes the magnetizing current of the core, the capacitive charging current for the cables, and any auxiliary load if applicable. The higher this value, the larger and more costly the transformer will be. Typical continuous current values can be as low as 5 amps to as high as a few hundred. Be sure to include any auxiliary loading requirements.

Continuous neutral current – The continuous neutral current is defined as three times the phase to current, or in other words, the zero sequence current. This is usually considered to be zero if the system is balanced. However, for the purposes of designing a grounding transformer, it is a value that is expected to flow in the neutral circuit without tripping protective circuits (which would force the current to be zero) or the leakage current to ground that is not a symmetrical function. Again this value is needed to design for thermal capacity of the grounding transformer.

Fault current and duration – This value is needed to calculate the short time heating that results from a fault on the system and should be determined from an engineered system study. Typical values range from a few hundred amps to a few thousand amps, with duration times expressed in seconds and not cycles. For instance, a value of 400 amps for 10 seconds is typical. The fault duration is a critical parameter for the transformer designer. Where protection schemes use the grounding transformer for tripping functions, a relatively short time duration is specified (5 -10 seconds). On the other hand, a continuous or extended neutral fault current duration would be required when the grounding transformer is used in a ground fault alarm scheme.

Impedance – The impedance can be expressed as a percentage or as an ohm value per phase. In either case it should be chosen so that the un-faulted phase voltages during a ground fault are within the temporary over-voltage capability of the transformer and associated equipment, such as arresters and terminal connectors. Values, which can vary from as low as 2.5 percent to almost 10 percent, must be provided by the system designer.

Primary winding connection – Be sure to specify the type of primary connection, either Zig-Zag or grounded Wye. Consider the factors discussed above concerning situations for which a particular configuration might be most appropriate, before making the decision.

Secondary connection – specify the secondary voltage and connection when applicable. Also be sure to consider the size of auxiliary loading to be connected for either Zn- or Wye-connected primary windings.
If the option is to have a two-winding transformer with no secondary load, determine if the delta winding can be "buried" (that is, not brought out) or if only one bushing is to be brought out for grounding to the tank or testing.

Important grounding transformer features and options

In addition to the design characteristics discussed, there are a number of other considerations or desirable features you should consider when building your wind farm grounding transformers:

- Advise the supplier whether you need a compartmental padmount transformer with integral tamper-proof compartment or substation design.
- Consider whether the grounding transformer will be located outdoors or indoors. Even outdoor units need special attention when placed near other structures.
- Select the proper fluid type for the particular application. Options include mineral oil, silicone, and Envirotemp® FR3™ Fluid, a natural ester-based fluid with exceptional fire-resistant properties and favorable environmental attributes.
- Consider connectivity choices and select the best one for the site. Options vary from dead front, live front, and spade terminals. Terminal location can be under a cover or on a sidewall, exposed or enclosed.
- Temperature rise is assumed to be 65°C – adjust design if necessary.
- Consider site elevation or any special environmental concerns.
- Special paint as required.
- Neutral ground resistors – The rated voltage of the NGR should be equal to the grounding transformer's line to ground voltage. The current rating and duration should match the grounding transformer ratings. Remember to set the current rating high enough to be above the cable charging current and grounding transformer magnetizing current.

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SURGE CURRENT LIMITATIONS

Capability of wire-bonded power diodes

By Thomas Hunger, Oliver Schilling, Frank Wolter, Thomas Schütze

The ability of silicon power diodes to withstand a rapid forward current load, described by its i2t-value, is an important criterion that has to be regarded in the selection of the proper devices for power electronic applications.

The dependence of the surge current limit on its pulse width is investigated for different diode types. A simple analytical formula for the maximum achievable surge current is derived.

Historically, diodes have been employed in passive input rectifier circuits prior to their extensive use as free wheeling diodes (FWD) for inverters. In rectifier circuits the time dependence of on-state current is closely linked to the frequency of the supply voltage. Therefore 10ms sinusoidal half wave pulses are typically applied to characterise the surge current capability. But there are working conditions that demand other pulse durations like in the 16⅔Hz power line of railway supplies where tP=30ms occur at the input rectifier.

Furthermore a rectifying action of the FWDs may also happen if energy is regenerated from the motor through the inverter into the DC link capacity at frequencies below 50Hz giving rise to tP~100ms. On the other hand short but high current pulses have to be withstood by the diodes if the energy in the DC link capacitor discharges during a bridge short circuit. The circuit consisting of the stray inductances and the capacitance of the inverter gives rise to damped current oscillations characterised by pulse widths far below 1ms.

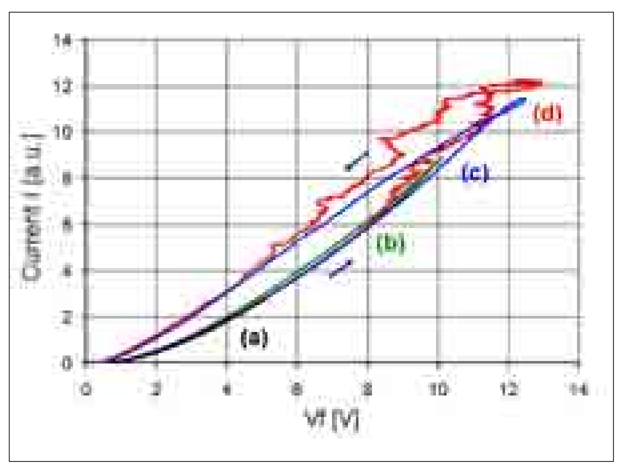

Figure 1: I-V characteristics of 10ms half sine pulses at different peak currents. Curve (c) is slightly above, curve (d) is far above the destruction threshold.

Surge current experiments

The surge current is measured via half-sine-current of a certain pulse length tP. Mostly, tP=10ms from a transferred 50Hz line is used. Fig. 1 and 2 show typical I-V characteristics taken for a succession of pulses.

The failure signature of a FWD destroyed by a surge current overload is designated by molten areas are located around the bond wedges. The failure signature indicates a thermal limitation of the surge current capability by local over-heating and destruction of the aluminium metallization layer. Interdiffusion of silicon and aluminium occurs at the die surface leading to a spiking of aluminium. The destruction of the upper pn junction is a consequence. Therefore, a loss of the blocking capability is the most sensitive indicator to determine the destruction threshold during surge current experiments.

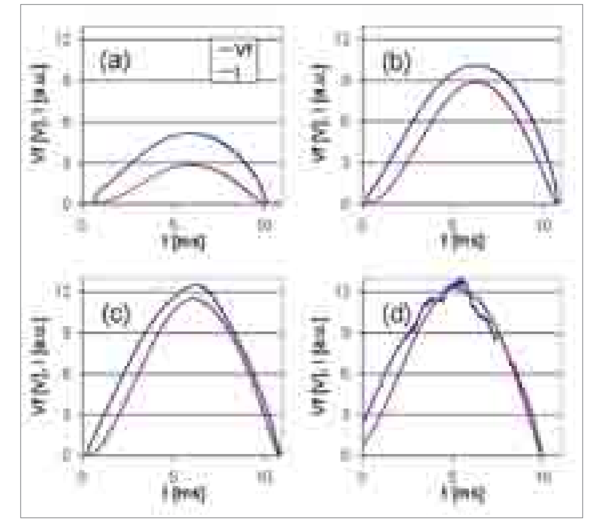

Figure 2: Time dependencies of current and forward voltage for the pulses of fig. 1. The curves depict I-V curves which are typical for diodes both in the up- and downward branch of the sinusoidal current. In fig. 2 the time dependencies of current and forward voltage drop are shown.

Analytical approach to the thermal limitations of surge currents

The temperature swing at the die surface is given by the thermal impedance Zth and the applied power:

(1) $\Delta T(t) = Z_{th}(t) \times P_0$

with a step function

(2) $P = P_0 \times \Theta(t)$

The pulse power of a sinusoidal current is now approximated as an effective square pulse with a temperature independent resistance R:

(3) $P_0 = \frac{\pi}{2} R \times I_{FSM}^2 = R \times I_{eff}^2$

Assuming equal destruction temperatures, eqn. (1) and (3) result in a simple formula for the dependence of the peak current IFSM at an arbitrary pulse duration tp:

(4) $\frac{I_{FSM}(t_p)}{I_{FSM}(10ms)} = \sqrt{\frac{Z_{th}(10ms)}{Z_{th}(t_p)}}$

The peak current of a pulse depends only on the square root of the ratio of its thermal impedance value with respect to a reference pulse. Fig. 3 shows the experimental data normalized to the 10ms values together with a scaling curve according to eqn. (4). The datasets for all diodes scale onto one single curve. Thus, the surge current of all diodes is supposed to be limited by the same physical mechanism. The thermal impedance curve is determined via a finite element approach under the assumption of a homogeneous power loss in the diode volume because of the lack of reliable experimental Zth-data for such short time scales.

There is a deviation between the experimental data and the thermal impedance considerations at short times. This is mainly due to the dynamics of the spike formation itself. Temperature alone is not sufficient since the pulse time and thus the diffusion time is also of importance. Therefore, the thermal impedance scaling, which is based only on the temperature argument, underestimates the actual surge current limit for short pulse durations because there is not enough time for sufficient spiking.

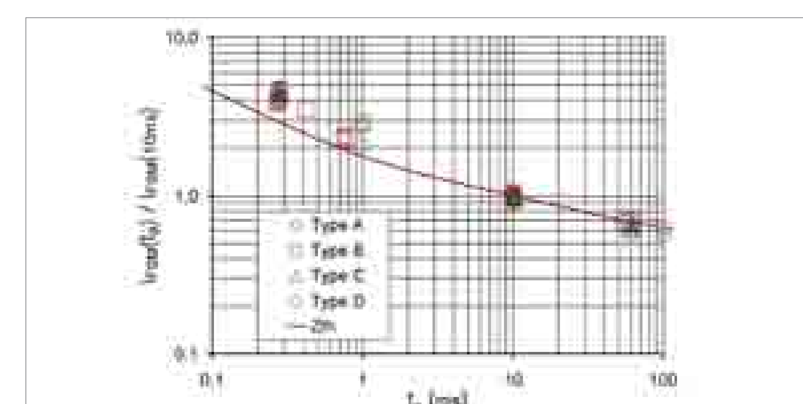

Figure 3: Normalized peak currents for different diode types. All experimental data taken for different diode types fall onto a single curve.

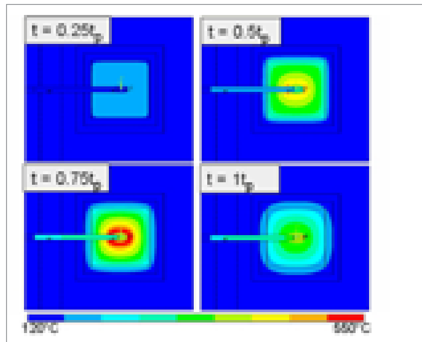

Figure 4: Temperature distribution at t=0.25tp, 0.5tp, 0.75tp and tp. The area around the bond wedge shows the highest temperature during the pulse.

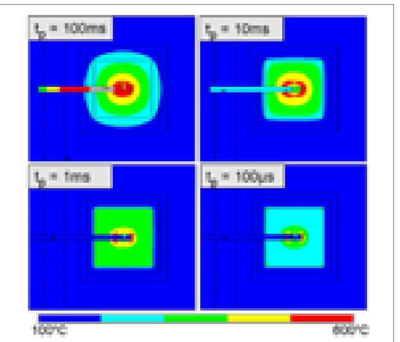

Figure 5: Temperature distribution at t=0.6tp for different pulse durations tp.

Simulation results

Finite element simulations of a test diode with one bond wedge were carried out to clarify the failure mechanism. Fig. 4 shows snapshots taken at different times during a simulation run for IFSM=172A and tp=10ms. The areas in the vicinity of the bond wedge get hottest during the sinusoidal current pulse. This corresponds very well to the failure signature, where molten aluminium is located around the wedge.

A comparison of the diode temperature distribution for different pulse durations is shown in fig. 5. For long pulses (here 100ms) the whole wedge area is heated. The bond wire itself is the hottest part. This is not surprising as one comes closer to the DC limits. Pulses with tp<100ms are limited by the temperature swing of the diode's metallization. For shorter pulse widths a localization of hot spots near the wedge can be observed.

Assuming that the failure events can be described by an equal maximum temperature of the hot spots, the dependence of the maximum surge current on the pulse width can be derived from a finite element calculation. The result is given in fig. 6 together with the prediction expected from the thermal impedance model of eqn. (4).

The simulation result resembles the scaled thermal impedance data for pulse durations of tp>5ms. The thermal impedance used here is computed for a specific test assembly. The deviations for small pulse widths can be explained by the high local temperature gradients which are in the order of the finite element mesh size. Improving the finite element mesh near the wedge would enhance the match of the results.

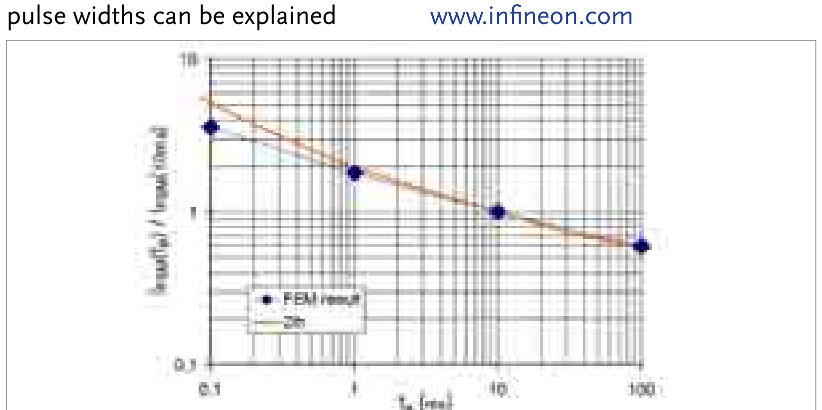

Figure 6: Normalized peak currents from the finite element simulation in comparison to the result based on the thermal impedance according to eqn. (4).

Conclusions

The surge current limitations of wire bonded silicon free-wheeling diodes were studied both experimentally and numerically. An analytical formula describing the peak current IFSM limit for different pulse widths based on the thermal impedance is derived. It is useable for the determination of a lower bound for the actual IFSM. Finite element simulations are used for the study of the destruction mode. The temperature distribution found numerically corresponds to the experimentally gathered failure signatures.

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EFFECTIVE CONTACT

Driving the electric revolution in the automotive industry

By Ted Worroll

This advanced charging in electric vehicles (EV) requires highly efficient power contacts to provide flexible functionality, with minimal modifications, across a power range from a low of 15 amps/120 volts to a high of 75 amps/ 240 volts.

As in most industries, the ultimate driving force in the automotive market is the consumer. In today's marketplace, consumers are demanding economical, fuel-efficient vehicles that still provide the safety standards, sleek engineering and hands-free controls that have become standard features in luxury models. As the pendulum has swung away from gas-guzzling status symbols of 'bigger and better' today's market has ushered in era of alternative energy and electrically powered vehicles. Manufacturers are designing new vehicle models with energy efficiency in mind to meet this growing public demand.

The most popular answer to increasing the efficiency of vehicles has been the implementation of plug in hybrid or full plug in electric vehicle technology. The lithium-ion battery that powers the electric motor requires a relatively long time to recharge and the battery life is shorter than desired by consumers. The inconvenience and inefficiency of the electric vehicle's charging system has certainly delayed the mass acceptance of hybrid vehicles by consumers.

A recent technological

ITT Interconnect Solutions' EVC series connectors advancement has enabled design engineers to address consumers' concerns about the electric vehicle's charging time requirements, thus resolving an uncertainty that has plagued the electric vehicle industry. In order to understand the change, one must look at the standard of which electric vehicles are held to for the proper charge. Previously, the standard charging time of an electric vehicle's lithium-ion battery was eight hours for a full charge.

The Society of Automotive Engineers (SAE) established the SAE J1772 practice covering the electrical, physical, performance requirements and communication procedures for the charge systems of electric vehicle. This charging specification standard has been adopted in both the U.S. and Japan for Level I and Level II electric vehicle charging.

- Level I: AC energy to the vehicle's on-board charger; from the most common U.S. grounded household receptacle, commonly referred to as a 15A/120V or 240V outlet)
- Level II: AC energy to the vehicle's on-board charger; 208-240 volt, single phase. The maximum current specified is 32 amps (continuous) with a branch circuit breaker rated at 40 amps. Maximum continuous input power is specified as 7.68kW (240V x 32A)

To pass the stringent specifications, the automotive market demanded a robust coupler. Additionally, the application requires a high-amperage charging solution that could provide fast, easy and safe charging of any electric vehicle. Manufacturers addressing the need for a high-amperage solution have reduced the Level II charge time by 50%, as illustrated by ITT Interconnect Solutions' EVC Series connectors. This advanced charging solution features highly efficient power contacts to provide flexible functionality, with minimal modifications, across a power curve ranging from a low of 15 amps/ 120 volts to a high of 75 amps/ 240 volts. Five contacts (two power, one ground, and two signal) make up the J1772 inlet, which features a touch-proof seal on the power and ground contacts. This flexible interconnect system is designed to exceed the electrical and mechanical UL specifications, as well as the SAE 1772 specifications across the power curve.

The interconnect solution also provides an enhanced cable management system that incorporates robust and proven technology with ground pin contacts on the inlet side by utilizing standard ITT VEAM CIR Series backshells, flange gaskets and mounting plates. Moisture drain holes are strategically placed to prevent latch freezing, making the interconnect non-functional for outdoor use in extreme environments.

Temperature stresses are common in automotive applications, requiring interconnects to withstand extreme temperatures. Further, the locking feature prevents unauthorized use of the charging system. All plastic-based materials are F1-rated per UL 746 C and are resistant to engine oils and UV rays. The IP44-sealed charging solution is rated for 10,000 plus cycles. In order to ensure the versatility for powering electric vehicles, the inlet has a rear accessory thread to accept a cable management backshell system. The inlet comes completely wired (with or without a backshell) and custom lengths are available. Right angle or straight configurations can be provided as well. If sealing is required, an optional gland or potting is provided.

As the automotive market continues to be driven by the consumer demanding more certainty and reliability, the electric vehicle is proving to be the viable option for the energy-efficient, environmentally sound alternative. The vast improvement and incentives for buying electric and hybrid cars continues to motivate buyers.

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Special Report: Digital Power

PSD EUROPE
Power Systems Design: Empowering Global Innovation

Inside:

DIGITAL POWER POL

What can it do for FPGAs, processors and other loads?

By Dan Tooth PhD

An engineer designing with FPGAs or Processors often has to provide some serious amount of power at high efficiency over load. Not only must the rails be regulated correctly and not overheat, but additional functionality may be required.

Recent evaluation boards from Xilinx (ML605 and SP605) for Virtex-6 and Spartan-6 FPGAs use a Texas Instruments digital controller power scheme. From the myriad ways to provide point-of-load power, why does an engineer need the digital power option? This is the question addressed here.

A Digital POL Power Scheme

Figure 1 shows a multi-rail digital controller IC, UCD9246, connected to a variety of power stages. The controller regulates the output voltages via sampling voltages / currents, implementing digital control loops and outputting high-resolution PWM signals to the power stages. A power stage has the FET drivers, FETs, power inductor and capacitors. It also provides the current / voltage / temperature feedback signals for the controller.

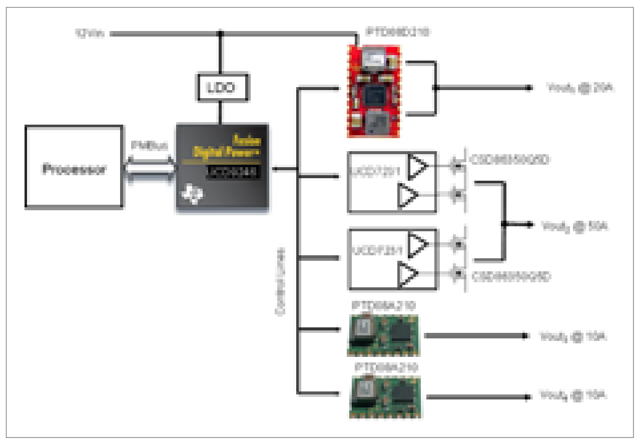

Figure 1: Digital POL Power Scheme

The Power Stage

The simplest way to implement the power stage is with a compact (15 x 28mm) digital power module like PTD08D210. It has two outputs that can be configured as 2 x 10A rails, or paralleled for a 1 x 20A rail. Another way to design a power stage is to use the digital FET driver UCD7232 (to release soon, similar to UCD7231) plus Texas Instruments very high efficiency "NexFET" MOSFETs, like the dual CSD86350Q5D or CSD86330Q3D.

Reasons to implement a voltage rail using the discrete ICs include (1) It is possible to convert from a lower input voltage – down to 2.2Vin (2) You can choose your own inductor and e.g. minimize its height. (3) You can design a rail with a particular output current to suit.

The Fusion GUI

The Fusion Digital Power Designer™ GUI is the powerful, free-download, Texas Instruments software used to configure all aspects of the controller. The Vout Configuration window is shown in Figure 2, as an example. The graphical representation of the sequencing makes it easy to visualize what effect the numbers being entered for the parameters will have.

9 Features of a Digital POL Solution

Ultimately, designers choose a particular solution over another one because of the cost-benefits, not because a solution is new or because it is "digital." In this section the benefits of the UCD92xx digital power solution are examined and their relationship to the Fusion GUI explained.

(1) Sequencing of rails up / down. Frequently, there is a requirement for certain voltage rails to be present before others, particularly when powering an FPGA or processor. Even if there is not a requirement, there still may be a case for sequencing them to guarantee repeatability when the design goes to manufacture. Another good reason for using sequencing is to reduce inrush current. The Fusion GUI easily allows setting the dependencies of each voltage rail upon other rails – you can set a voltage rail to start (or stop) after another has reached regulation or gone out of regulation.

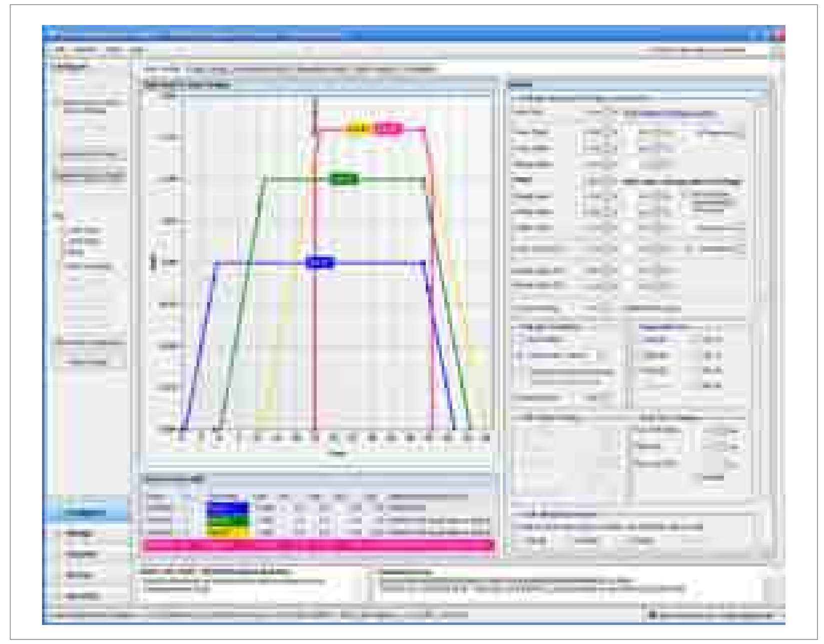
Figure 2: Vout Configuration Window in the Fusion GUI

Using the programmable delay and rise time capability of the UCD92xx controllers enables timed starting of multiple voltage rails. The UCD92xx devices can also be configured to enable sequential starting (or stopping) of voltage rails and/or ratiometric start-up, where two rails enter regulation at the same time. Tracking start-up of rails is also supported, as is pre-bias start-up, see item (8) below.

(2) Monitoring and event-logging to non-volatile memory. The UCD92xx controller allows four levels to be set per rail – under/over voltage warning and under/over voltage fault. The controller can be set to take actions, such as turning off other rail(s), or automatically restarting, if a rail goes out of its User-defined regulation.
The current per phase is also monitored by the power stage and reported back, as is the input voltage and power-stage temperature – if a digital power stage module is used. Over/under current, over/under voltage, over temperature warnings and fault thresholds can all be set by the user.

(3) Parts count reduction. Using the digital power solution enables multi-rail, multi-phase power supplies controlled by one IC. Since timing is configured digitally, there are no timing caps or resistors. The compensation loops are in the digital domain, so there are no external passive components to set poles and zeros. The same IC also provides other features, such as the monitoring and sequencing functions.

(4) Digitally changing Vout &

Vout Margining. A digital power solution has Vout for each rail under digital control, meaning the host processor can write a new value of Vout for a particular voltage rail over the PMBus interface to the digital controller. Some controllers in the UCD92xx family, such as the UCD9222 and UCD9224, also have a multi-bit VID (voltage identification) interface which allows the powered device to dynamically adjust the voltage being supplied to it.
Margining is the ability to change Vout up or down by a prescribed amount to test the robustness of the overall system design to the set-point tolerance of each rail and is fully supported by the controller.

(5) Paralleling of outputs for higher current and phase-shedding at light load.
It is often desirable to parallel multiple sets of MOSFET half-bridge and inductor circuits. At full load, where conduction losses dominate, the efficiency of the multi-phase converter is higher than a single phase solution. Another advantage of using multiple phases is to increase the surface area of the power conversion, which enables improved thermals and a lower profile solution. If the switching action of the phases is interleaved, then the effective switching frequency is increased and a reduction in output and input ripple voltage can be obtained, reducing capacitor count. At light load, when switching losses become a bigger factor, the UCD92xx controller can be configured to automatically turn off unneeded power stages. This is called phase-shedding and increases light-load efficiency.

(6) Configure your own control loop compensation or use Autotune. Autotune is a powerful part of the Fusion GUI that designs the poles/zeros compensation for a modular or user-defined power stage. Non-linear control can be used. An example would be to reduce the gain during steady state conditions to minimize jitter noise on the output, but if the error increases past a certain level, then switch to a higher gain, to bring the converter's output back to the set-point more quickly. This means Vout disturbances in response to load transients is minimized.

Auto-ID is another remarkable feature of the UCD9246, which injects a sine wave into the control loop and measures the system response at another point in the loop. This allows the UCD9246 to measures its own closed-loop transfer functions.

(7) Switching frequency synchronization. In some applications it is desirable to synchronize the switching frequencies across one or more controllers to a common clock input and this is supported by these controllers.

(8) Pre-bias start-up. "Pre-bias" refers to a pre-existing voltage on a non-enabled rail (e.g. the core voltage) that has been parasitically charged-up to some voltage via another voltage source. If not carefully managed, when the core voltage rail is enabled, a large current can flow through the synchronous MOSFET, destroying it. To prevent this, the controller implements a closed-loop start-up function, using the pre-bias on Vout as an input to that function. As a result, when the voltage rail is enabled it ramps up seamlessly and monotonically.

(9) Supports last minute changes and new customer requirement spins with no hardware changes. Sometimes, last minute requirements or changes creep into the specification. Because more of the power scheme is under firmware control, the chances are greater that the amendments can be made without needing a board spin.

Conclusion
Digital POL power finds its niche in applications where their strong features are valued and helps engineers designing with FPGAs or Processors to provide the required amount of power at high efficiency over the full range of loads with the differentiating benefit of additional functionality.

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DELIVERING PRECISION PERFORMANCE

Automated control of circuit board DC-DC power supplies

By Randy Skinner

Modern microprocessors, FPGAs and other complex ICs require accurate power supply voltages, often more accurate, in fact, than the tolerances provided by commodity low-dropout regulators (LDOs) and DC-to-DC power supplies. More precise power supplies are available, but at a premium price. The cost effective alternative is to use a separate power supply management IC to adjust the precision of one or more supplies at the same time.

Providing a control signal to dynamically and continuously adjust a power supply's output voltage is referred to as closed-loop trimming.

Once the power supply is adjustable, other benefits can be realized. For example, a circuit board can also be tested for reliable operation over a range of voltage supply values. This is referred to as supply voltage margining. The adjustable voltage supply values can be used to simulate the expected precision of the power supply voltage, drift that can occur due to component

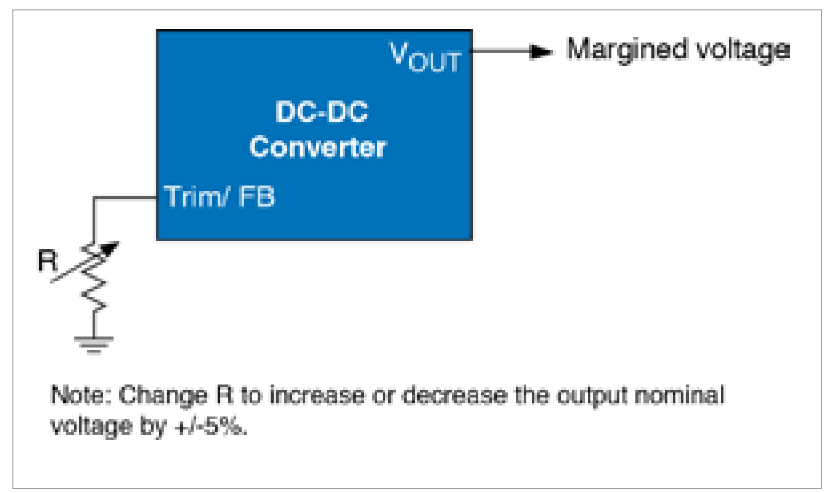

Figure 1: Supplies are margined by changing the resistor connected to the Trim/FB node

aging, ambient temperature changes or fluctuations in supply load current.

Voltage margining
A voltage margining test ensures that the board is functional

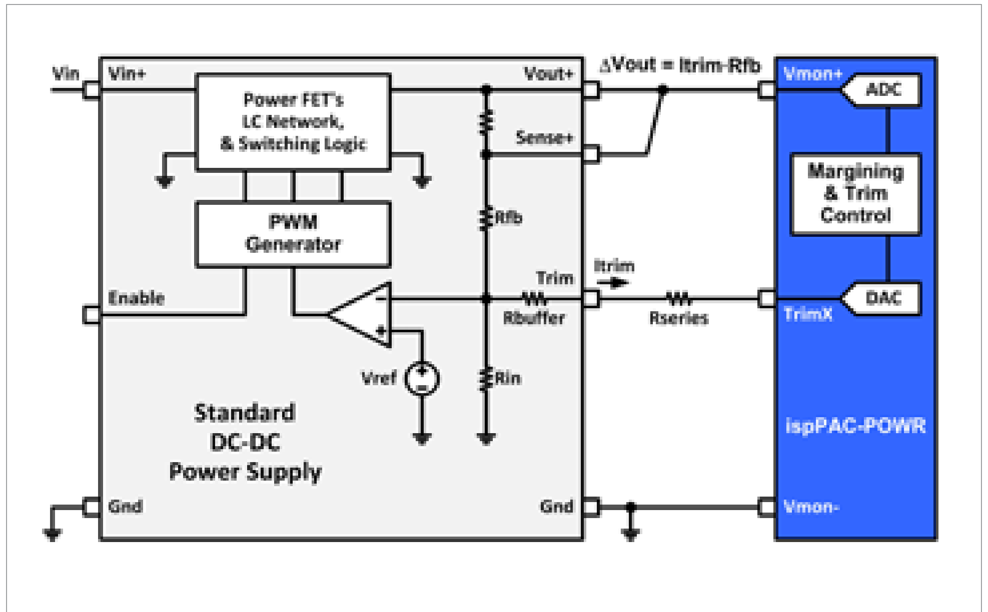

Figure 2: Supplies are margined by changing the resistor connected to the Trim/FB node

across the operating range of its onboard and input supplies. Circuit boards are also subject to other margining tests, such as temperature, timing and noise. For example, if the allowed tolerance of a supply input is ±10%, the voltage margining test ensures that the board is functional when the input supply is at its margin-high (nominal voltage +10%) value and when its supply is at margin-low (nominal voltage -10%) value. If the board has a number of board-mounted supplies, then the margining test should also include the variation of individual board-mounted supplies. Margining tests typically are conducted during board debug. In some cases, Quality and Reliability departments will require margining before they will approve manufactured boards.

Voltage margining implementation

Figure 1 shows a DC-DC converter with a resistor connected to its internal Trim/Feedback Node. The value of this resistor typically determines the nominal output voltage value of the DC-DC converter and is specified in the power supply's datasheet.

DC-DC converters usually require standard resistor values to set their output voltage to a standard value – e.g. 3.3V, 2.5V, 1.5V. To change the output voltage by +/-5% of their nominal operating voltage, designers use either a potentiometer for each of the DC-DC converters or a series parallel combination of standard resistor values. One has to manually implement the resistor change to all the boards that will be subject to testing in an environmental chamber. Due to delays and added cost, margin testing usually is not performed in a production environment. If it could be automated, however, it would become a powerful tool in verifying the reliable operation of a circuit board.

Applications that require power supply trimming

Trimming is required for circuit boards using ICs that require low supply voltages (1.2V or lower) with high current ratings (5A or more).

For example, a 1.2V DC-DC converter should guarantee a maximum of +/-5% (+/-60mV) variation under all of the following conditions:

- No-load to full-load average current variation
- Output voltage ripple
- Dynamic power demands by the IC during different average current levels
- Component tolerances during manufacturing

In general, to meet the voltage device spec under all of the above conditions safely, the DC-DC converter requires an initial operating voltage accuracy of 2% or better. These high-accuracy, low-voltage supplies are usually more expensive and require high precision resistors to set the voltage.

Alternatively, the accuracy of a conventional lower cost DC-DC converter can be improved by using an external trimming mechanism. The next section describes trimming using a Lattice Semiconductor power management IC. Similar products are also available from Maxim, TI and Analog Devices. The Lattice Semiconductor products will be used here to explain the basic principles of trimming and margining.

Trimming and margining: Principle of operation

Figure 2 shows a Lattice Power Manager II device implementing trimming and margining functions for an analog DC-DC converter.

On the top portion of Figure 2 is a DC-DC converter supplying power to its load. The output voltage is determined by the components used in its feedback circuitry. The Power Manager II device on the right measures the DC-DC output voltage using the on-chip ADC though differential sense inputs (Vmon+ and Vmon-). The Power Manager II can increase or decrease the output voltage of the DC-DC converter by increasing or decreasing its trim voltage with its on-chip DAC, thus changing the current applied to the DC-DC converter's feedback node.

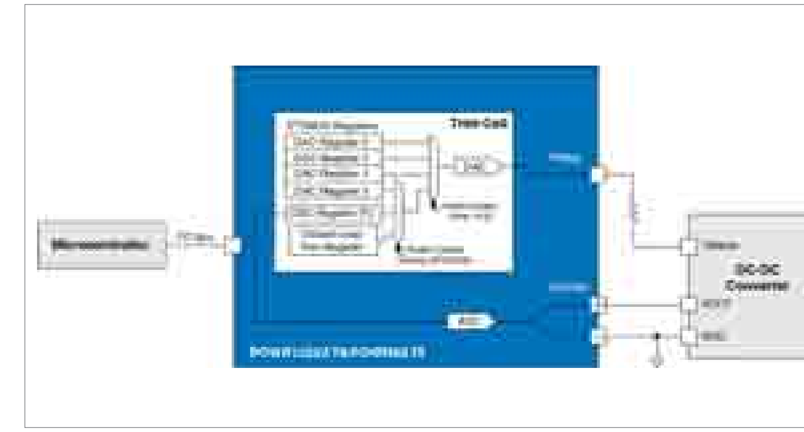

Figure 3: Closed Loop Trimming and Margining Using a Microcontroller

A set-point register in the Power Manager II control circuitry holds the required voltage value at the load. Once every 580us the Power Manager II device measures the voltage at the load using its on-chip ADC. The digital output of the ADC is compared against the set-point register contents. If the load voltage is higher, the DAC contents are decremented, which in turn reduces the voltage applied to the feedback node of the DC-DC converter. If the load voltage is lower, the DAC contents are incremented, applying higher voltage to the node. This is called the closed loop trim mechanism.

It is possible to break the closed loop trim and load the DAC register directly through the I2C bus to the Power Manager II device. This method is used to implement margining. An external microprocessor directly loads a pre-selected DAC value into the Power Manager II, which will result in changing the output voltage by, for example, +/-5%. The microprocessor can also measure the output voltage of the DC-DC converter using the Power Manager II's ADC, and tweak the output voltage up and down as needed to implement closed loop margining. In a circuit board, there typically are multiple types of supplies providing different supply voltages. These individual supplies require different current levels to be injected into their feedback nodes. This in turn requires a unique resistor network for each type of DC-DC converter to be connected between the Power Manager II and the DC-DC converter feedback node.

Closed loop trim and closed loop margining using a microcontroller

Figure 3 shows the configuration used for closed loop trimming with a microcontroller. Here the microcontroller measures the DC-DC converter output voltage periodically, using the on-chip ADC through the I2C bus. The microcontroller then algorithmically calculates the new DAC value depending on the DCDC converter voltage and loads the new DAC code through the I2C interface.

The microcontroller-based margining is implemented entirely through the I2C bus and uses profile 0 in the Power Manager II. To implement closed loop margining, the microcontroller loads the starting DAC code into the DAC register via I2C and waits for the ADC voltage to stabilize. Depending on the stabilized voltage value, the microcontroller increments or decrements the DAC code. This method enables setting and controlling the margined voltage accurately.

Designing trimming and margining networks using PAC-Designer software

Determining the required resistor topology involves finding a solution for a number of nodal equations and an understanding of the error amplifier architecture of the DC-DC converter. In addition, the design can be iterated until the solution yields standard resistor values.

The Lattice PAC-Designer software automates the process of determining the resistor topology while using standard resistors in the resistor network. More details on interfacing Power Manager devices to various types of power supplies and how PAC-Designer design software simplifies that task are available online at www.latticesemi.com. An excellent reference showing more detail can be found in Lattice application note AN6074, Interfacing the Trim Output of Power Manager II Devices to DC-DC Converters.

Summary

The use of widely available power management control ICs, such as those available from Lattice Semiconductor (Power Manager II and Platform Manager product families) enable the use of commodity priced DC-DC and LDO power supplies to deliver precision voltage performance. In addition, testing techniques such as power supply margining are made available via I2C control once the supplies are in a control environment.

Devices from multiple vendors are available ranging from simple 1 to six supplies. Lattice provides two families of power and board management devices with up to eight trim power supply trim outputs. Also integrated in the same Lattice devices are other power and board management functions, such as supply sequencing and monitoring, supervisory functions, reset generation, hot swap and more.

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DIGITAL POWER DELIVERS AUTO-COMPENSATION

Saves designers' time for a more stable power supply

By Chris M. Young

Stability is a critical operational requirement for power supplies. In regulated power supplies, the stability is controlled, by a large part, by the characteristics of the feedback path.

Power supply engineers need to be conscientious of these characteristics during design to ensure stable operation over all load conditions, environmental conditions, and component characteristic variations. Often, the design of the feedback loop to be stable under all of these conditions is a time consuming task.

Depending on the analog filter network used, a number of components may be needed to compensate a conventional power supply. During development, these components need to be selected, procured, and soldered to the board. Many times the component values need to be adjusted to tune the compensator to attain the desired compensation over the full operational space. To further complicate the problem, parasitics play a strong role in the feedback loop. These parasitic elements are challenging to model and are not well controlled for many power components. The load itself is a key element in the feedback loop and many times its characteristics are not well understood. Add the fact that the parasitic elements and the load itself may not be constant valued so the compensation needs to be robust to parametric variations.

To further illustrate the difficulty in compensation, consider two situations. In the first situation a high Q (low loss) design can be readily compensated in lab but once the design gets into production, the power inductor can vary in value by +/-10% and the output capacitors can vary by +/- 10%. This can significantly change the control loop even to the extent that the power supply has substantially degraded stability. In the second situation, consider equipment designed for outdoor applications and used electrolytic capacitors in the output filter stage. During the winter, cold electrolytic will have high ESR and low capacitance until they warm up and then the ESR will fall and the capacitance will rise. This, again, significantly changes the feedback loop and can lead to degraded stability.

For over a decade now, digital power solutions have provided an alternative to analog compensation. Since an analog compensation network is simply a filter network, the digital filters in a digital power controller can be used for the filter/compensation element. This means that the compensation has no external components and can be tuned by changing the gain values stored in digital registers. Clearly this offers an advantage over analog compensation in terms of dealing with the external compensation elements. So, digital compensation allows easy tuning of the compensator and is done, in most modern designs, using a graphical user interface (GUI) where gain values are entered using a point-and-click, easy to use tool.

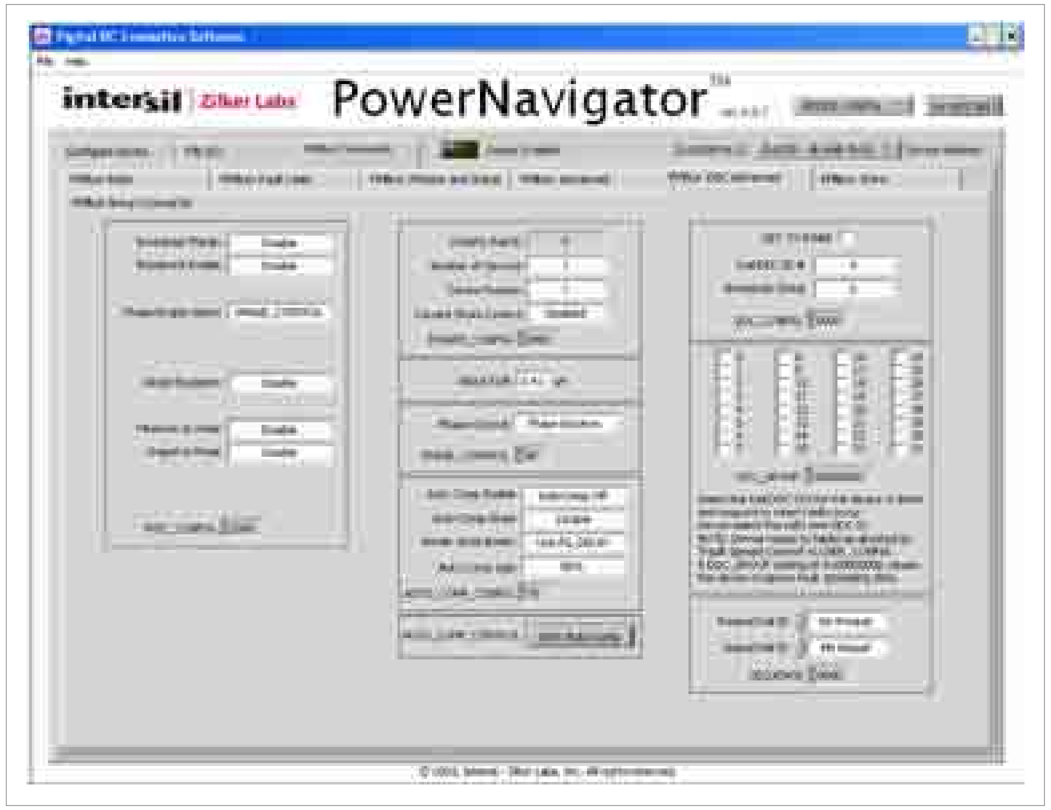

Figure 1: GUI view of Auto Compensation page

Digital filters are not simply replacements of analog filters. Digital filters can perform functions that go far beyond the capabilities of analog filters. For example, in high Q (>0.5) second order circuits, the poles in the plant are complex conjugate poles which may require complex conjugate zeros in the compensation network to effectively compensate. Conventional analog compensators only provide real zeros for compensation. This limits their ability to effectively compensate high Q power supplies. On the other hand, digital filters can easily provide the complex conjugate zeros to compensate high Q power supplies. This means that their compensation starts out more stable than their analog counterparts so they are less affected by component parameter variations. Nonetheless, even this advantage, in many cases is not enough to stabilize and optimize a power supply over all conditions. What is really needed is a method for compensating power supplies that is automatic. In recent years, the digital power industry has focused on this issue of automatic compensation. While a number of papers have been published discussing ideas for automatic compensation, until recently, no parts have been made available. Intersil's Zilker Labs has recently released its ZL6105 which is a full featured, intelligent, digital power supply that does have the capability of automatic compensation.

The ZL6105 is based on the popular digital controller line from Zilker Labs and uses an advanced digital algorithm to characterize the plant and to determine appropriate compensation settings for stable operation. These digital

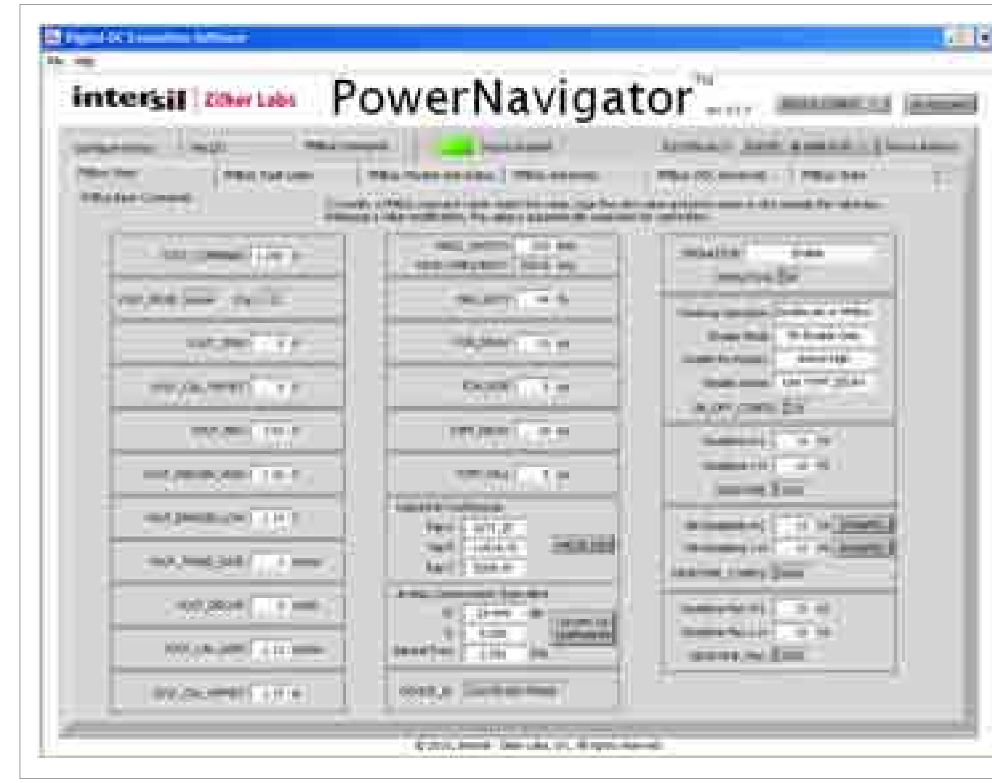

Figure 2: Power Navigator(TM) showing compensation values

controllers use a dedicated state machine for the digital PWM controller and an embedded microcontroller to monitor the circuit, environmental conditions, and configuration profile to setup and modify the state machine operation in real time. During auto-compensation, the microcontroller adjusts the state machine to stabilize the power conversion process. Power train component values are set at the manufacturing stage or change slowly so that the microcontroller can easily accomplish its tasks with little power.

Like the other Intersil digital controllers, the ZL6105 can be configured using the GUI interface, Power Navigator™. Power Navigator™ connects to the power supply through a USB to SMBus dongle.

Once connected, Power Navigator™ is used to fully configure the controller and provides telemetry information such as input and output voltage, output current and temperature as provided by the controller. The automatic compensation can also be configured using the GUI interface.

Auto-compensation can be configured as desired. Figure 1 shows the view of the GUI, tabbed to the page that allows configuration of the auto-compensation. There are four basic modes that can be selected: off, once, once per second, and once per minute. The "off" configuration disables the auto-compensation. The compensation can be set manually using the options found on a different page within the GUI.

The "once" option configures auto-compensation to occur only when (and every time) the power supply is enabled. This is a good option if the primary concern is compensation at time of manufacturing. The "once per second" and "once per minute" options can be used to periodically re-compensate the power supply and is useful when the circuit parameters change over time.

While the controller can be configured to automatically auto-compensate, it can also be commanded via PMBus command to compensate itself on demand. Using the GUI, this is done with the push of a button.

The auto-compensation configuration has an option to save the compensation values in non-volatile memory. Otherwise the compensation values are stored in RAM. Non-volatile memory has a finite number of write operations so care needs to be used when allowing the controller to save the values to non-volatile memory especially if "once per second" compensation is selected.

With auto-compensation configured as "once", the auto-compensation algorithm performs its operation right after the ramp of the voltage, once the power supply is in regulation. The "power good" indicator is usually set to indicate that the power supply is in regulation but it can be configured to wait until the auto-compensation algorithm is complete.

A final configuration option for auto-compensation is a gain value associated with the final compensation. Users may want to reduce the control loop bandwidth to balance tradeoffs between transient performance, noise, and stability. The final loop gain can be adjusted in 10% steps from 10% to 100% of full value.

Of course, out of the box, the controller is set with default values so that the power of auto-compensation can be used without user interaction. Figure 2 shows the compensator settings, both in terms of the raw compensation gain values and more user friendly values of Gain, Q, and Natural Frequency which more intuitively characterize second order systems.

Automatic compensation takes what has been a difficult, time consuming task and reduces it to the simple click of a button or even more simple, a default setting. The patent pending auto-compensation algorithm is designed to be robust even in an environment of changing circuit parameters.

An additional benefit of automatic compensation is that the plant is characterized by the compensation algorithm. The values of Gain, Q, and Natural Frequency can be monitored over the life of the power supply and significant changes in the plant can be observed, many times, before failure of the system. This allows the user to incorporate predictive diagnostics of the system health for improved reliability.

By saving the design engineer a considerable amount of time, producing a more stable power supply, and potentially improving the reliability with predictive diagnostics digital power with automatic compensation is major technological improvement.

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DIGITAL POWER CONVERSION

Improved current sharing made easy

By Andrew Skinner

Power supplies with digital control are gaining in popularity. However the term 'digital control' is commonly applied to two quite different meanings.

The two main terms are; 'Digital power management' where customers communicate with the power supply to monitor status and adjust certain parameters remotely such as voltage, current limit, etc. and 'Digital power conversion', which is still in its infancy in terms of products available commercially, involving replacement of the common power supply analogue control loop with a digital control loop.

Flexibility is one of the major advantages of power supplies using digital power conversion, where customer specific optimisations can be achieved without the expense of changing the hardware. Andrew Skinner, Chief Technology Officer of TDK-Lambda UK explains how current sharing power supplies operating in parallel can be improved significantly without compromising reliability.

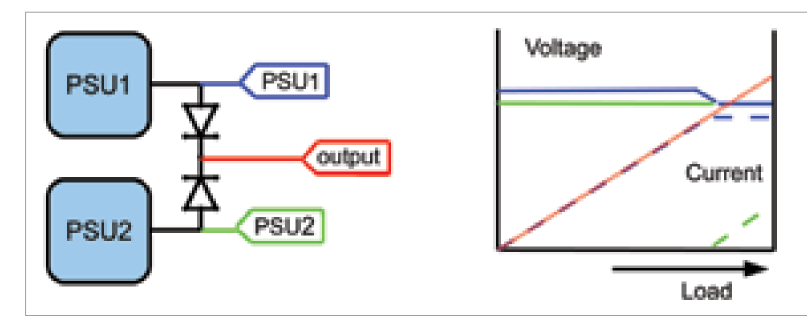

Figure 1: The effects of parallel connecting two power supplies without share control

When two or more power supplies are connected in parallel, the power supply with the highest output voltage will supply the load; the second unit only supplying current when the output voltage of the first falls below the voltage of the second. The amount of load required to achieve some degree of sharing is dependent on the setting accuracy, load regulation and thermal drift of the supplies used. For power supplies with a small variation in output voltage with load, no sharing may occur until the first power supply is overloaded and enters current limit - see Fig. 1.

The normal solution to this problem is to have a separate circuit that forces current sharing. This usually takes the form of a single wire connection between all the power supplies that are paralleled known as a current share bus. The bus effectively acts as a current demand reference and all the power supplies endeavour to follow this. In theory, this is quite a good solution since it maintains good load regulation but in practice at light loads it doesn't tend to work very well; it is not uncommon to require a minimum load for sharing to occur. The current share bus is also a single point of failure for the whole system since loss of the bus could result in zero demand to all the power supplies. Now one of the main reasons for paralleling power supplies is to improve reliability by having an N+1 setup – so to have something where you have a single failure point bringing the system down completely defeats the objective.

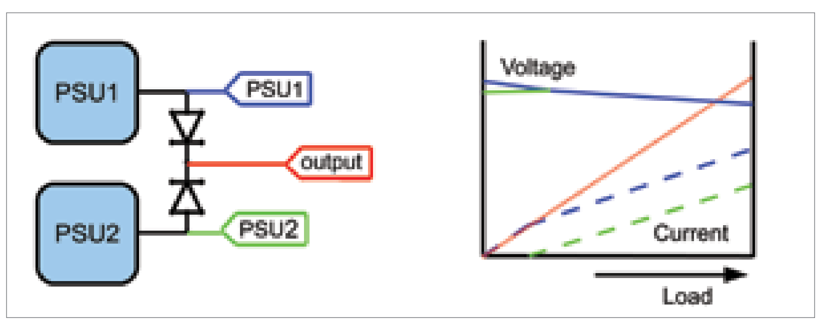

Figure 2: Characteristics of parallel connected power supplies incorporating droop share

Another less common solution to provide sharing between paralleled power supplies is to increase the load regulation (the amount the output voltage changes with load). By doing so, the output voltage changes more quickly with load current and therefore not as much current is needed in the higher voltage power supply before the lower voltage one starts to carry current (see Fig. 2). In this scheme there is no share bus and hence no single point of failure. In a number of high reliability applications, including some telecom systems and a number of medical applications, this is the preferred method of current sharing. This method is often referred to as 'droop sharing'.

Clearly there are some applications that require droop but many applications with only one power supply that don't. On the EFE series, which uses digital power conversion, the normal setting for a single power supply unit is just as you would expect with a nominally zero slope. However, for paralleling, rather than having a fixed output characteristic, which you would find in most power supplies, on the EFE series the load regulation is defined as one of the many programmable features. Effectively this feature allows the 50% load point voltage to be set -5/+10% of nominal and the load regulation can be programmed with either a positive or negative slope. The control algorithm is programmed such that the result of the slope is always within the specified output range.

Skinner notes: "Optimising the power supply performance in this way has become possible due to our strategic decision to develop our own digital power conversion intellectual property from scratch rather than use some of the proprietary devices now available. You need to fully understand the algorithms involved in order to maximise the flexibility that digital power conversion can bring."

Referring back to Fig.1, if the two power supplies are operated in parallel with no droop sharing then for most load conditions, one carries all of the current (and consequently runs hot) and the other one sits there doing nothing (consequently running cooler). In itself, this does not cause a problem other than the fact that reliability and life are temperature-dependent. However, some topologies when lightly loaded will enter a different operating mode (e.g. PWM controlled forward converters will go into discontinuous-mode resulting in a high effective output impedance until the control circuit recovers resulting in a low output voltage if fully loaded). If PSU1 fails then the duty-cycle of PSU2 must ramp up from its very low level in order to supply the load before the output capacitor discharges. This could require significant additional capacitance to be fitted in order for the combined output to stay within acceptable limits.

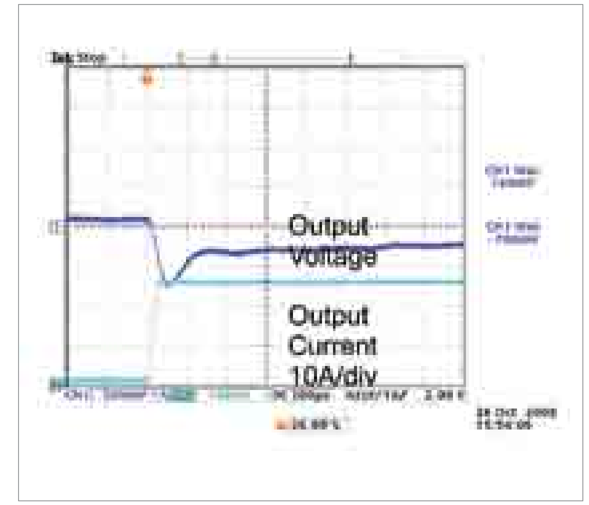

Figure 2: Characteristics of parallel connected power supplies incorporating droop share

Conversely the EFE300M, which includes an ORing MOSFET, operates in a way in that ensures the correct output voltage is maintained even at zero loads and that the output impedance remains at a low level. Droop, when specified, will improve current sharing and product life but, even when droop is not specified redundancy will still be achieved due to the excellent 0-100% load-transient performance of the EFE, see Fig. 3.

Skinner concluded, "The beauty of digital power conversion in supplies such as the EFE range is that customer specific droop characteristics are simple software changes with standard hardware thus reducing cost, speeding up time to market, and improving overall system reliability."

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www.uk.tdk-lambda.com

DIGITAL POWER CONTROL IMPACTS POWER DESIGN ON MANY LEVELS (PART 1)

By David G. Morrison

Use of digital power control is on the rise as it finds its way into more and more applications, a wider range of power levels, and even high-volume applications where cost barriers may have prevented its entry in the past. Although volumes are still low for many digital power designs, the field is growing and as it does, it is changing the way power components, power supplies, and power systems are designed. Consequently, the mix of skills required to design these products is also changing.

With digital power control, power supply and power system designs tend to fall into two main camps. There is the highly programmable approach that builds designs around digital signal processors (DSPs) and digital signal controllers (DSCs). Then there's the approach using dedicated power supply controller ICs built around state machines that run control algorithms designed for a specific power conversion function like a multi-phase buck converter. The DSP/DSC approach tends to be applied at higher power levels and across a wider range of power supply functions. The state-machine approach is currently being applied in high-volume, board-mounted power applications.

In the first part of this article, we'll look at the impact of digital power supply controller ICs on the types of skills and experience required in power design. Next month, in part two of the article, we look at the impact of DSCs and DSPs on engineering requirements.

Wide Ranging Applications

Much has been previously written about the benefits of digital power control–how it enables designers to optimize efficiency, reduce components count and cost, improve transient response, obtain design flexibility, etc. Such benefits have spurred adoption of digital power control across "wide variety of power conversion applications," according to Bill Hutchings, a product marketing manager with the High-Performance Microcontroller Division of Microchip Technology.

"Digital power control is being used in traditional power-supply products, such as ac-dc power supplies, dc-dc converters, and uninterruptable power supplies. It is also extensively used in renewable energy for control in solar and wind inverters," says Hutchings whose company supplies DSCs into digital power applications. "However, the applications extend out well past what we normally think of as power control to a wide variety of lighting products such as HID and LED light ballasts. Additionally, digital power control is used in numerous market segments, including the industrial, medical, consumer, and automotive markets. "

While some applications of digital power are new, others are well established. Patrick Le Fèvre, marketing and communication director of Ericsson Power Modules observes that the UPS industry has been using DSP-based control since about 2003. And since around 2005, says Le Fèvre, original equipment manufacturers in the information and communications technology (ICT) industry–which encompasses everything from radio base stations to data centers–have been using digital power control in various forms in both isolated and nonisolated dc-dc converters. Ericsson Power Modules is one the companies supplying this industry with such digitally controlled dc-dc converter modules.

Chip Design Requires A Team Approach

The spread of digital control into these various applications is changing the way power IC, power supply, and power system designers do their work, but in different ways. First, let's consider an example of chip design.

David Williams is the director of systems engineering at CHiL Semiconductor, which supplies digital power controller ICs used in multiphase buck converters that power CPUs, GPUs, and memory. According to Williams, the migration from analog to digital control has meant that more of a team approach is needed to designing the controller. "You don't have the lone IC designer going off and creating an analog controller like the '3542, you've got a team of designers, one doing the analog section, one doing the digital section, another guy (the system architect) overseeing how the things go together. Then, there's another person overseeing how the controller goes into a system and how it's going to react to the system board," says Williams. "Lastly, we need to create graphical user interfaces (GUIs) so customers (power supply designers) can interface with and program the VR PWM controller."

Although going to a digital controller design enables new performance capabilities and functions, the heart of the job is translating what would be an analog chip into digital. "Instead of PWM ramps, you've got digital comparisons deciding how to create the PWM pulse width. Instead of Rs and Cs doing the feedback loop, you've got PID coefficients that modify the error voltage digital value to help determine the pulse width. But it's essentially the same type of architecture," explains Williams.

While the designers working on the analog section have analog circuit design background, the digital designers, who write the state machine code have different experience. At CHiL, these engineers are former telecom IC designers who have a thorough understanding of filters and registers. "The telecom guys are used to working on A-Ds, processing signals, bringing them in, filtering them, processing them, and sending them back out," says Williams. This type of background enables the digital designers to translate the requirements for inputs and outputs for the control block as specified to them by the system architect.

GUIs Simplify Power Supply Design, But Digital Knowledge Helps

The above example not only illustrates the group effort required to produce a digital power controller IC, but also how the technology requires greater specialization of the engineers working in the power IC world. While the process of designing such digital power ICs is complex, the goal here is to remove much of the complexity of applying digital power control in power supplies and power systems. Bob White, president and chief engineer of Embedded Power Labs, explains how he sees digital control affecting these engineers.

"Most power supply engineers will never be writing code or doing Z transforms to implement a digital control loop. They will be using ICs from companies like TI or Intersil to implement digital control loops," says White. "However, they will interact with these ICs through computer-based interfaces. In the short term, I think those interfaces will present the design in terms familiar to power supply designers: continuous-time Bode plots. Over time, I think the designs will migrate into direct digital design, especially as more and more engineers who are in school now move into the working world." Others in the industry expressed similar sentiments regarding requirements for implementing digital control loops at the power supply or power system level. "You only need to work with the Z-domain to optimize the control loop if you're developing a low-level product [such as the controller IC]," says Patrick Le Fèvre. "Within the power community, perhaps only 10% to 15% need to have this very high knowledge of coding. If you design a power-on-board solution, you don't need to go down to this level, you can simply use the graphical user interface provided by the silicon provider, do the whole simulation on your screen, flash the memory in the power IC, and then run the device."

Nevertheless, Bob White adds a note of caution with respect to GUIs. "While most power supply engineers may not be writing code or programming DSCs and FPGAs, they will want to know 'what's under the hood.' Being given a GUI does not lend a lot of assurance that the chip is going to do what it is supposed to do all the time. So I think that power supply engineers will need to know the basics of discrete time design. They will have to understand the issues with sampling, delay, the effects of finite word length, be familiar with continuous time/discrete time transformations, basics of the algorithms used, and digital PWM techniques. It also means that the IC makers, many of whom will have "secret sauces", are going to have to figure out how to educate their customers on how their parts really work without giving away the secrets."

For examples of actual engineering positions in the power IC industry related to the development of digital power ICs, see the online version of this article.

About the Author

David G. Morrison is the editor of How2Power.com, a site designed to speed your search for power supply design information. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Watch a short video about How2Power Today at www.how2power.com/newsletters.

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DIGITAL SOLAR

By Cliff Keys

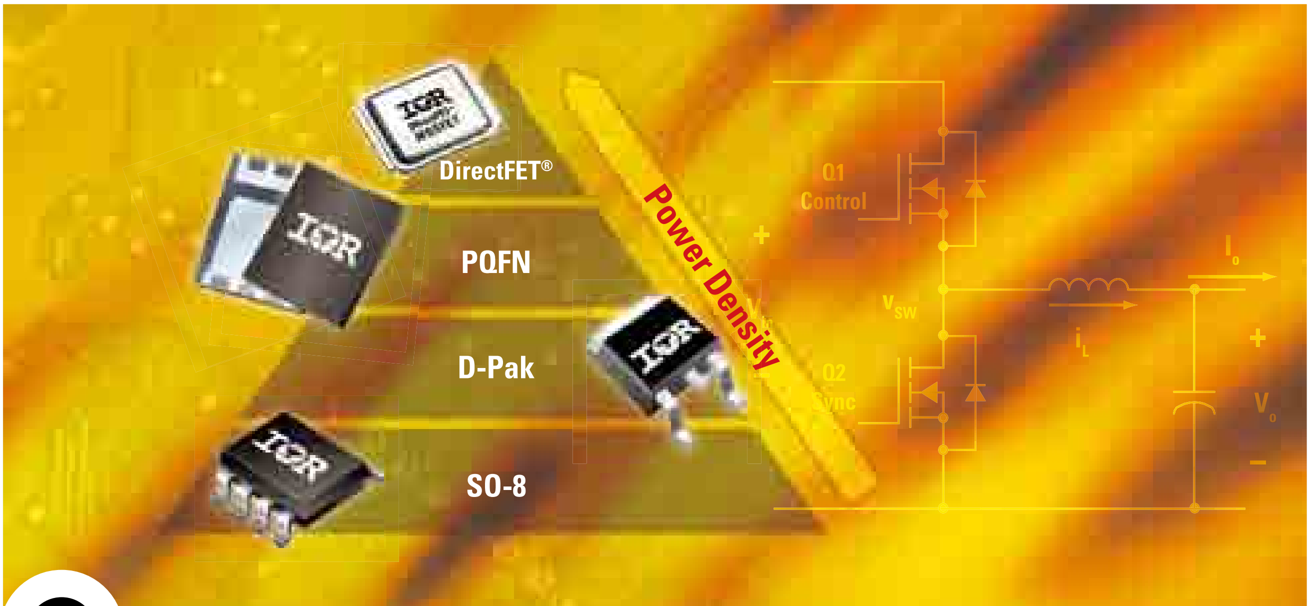
If what we are all reading and hearing from the analysts and research houses is correct, digital power is to continue to grow at a fantastic rate.

This should be a great business opportunity for digital power vendors and gives us all in the power industry a new technology to get to grips with and take advantage of, but there is another side: It should help products get to market faster and run leaner and meaner – and therefore greener. I believe it will help considerably over time. And with digital power technology working to secure the IP and get the very best out of the latest Solar installations, this is further proof of the benefit.

Solar has proven its contribution as a green energy source already. With their capability to increase the efficiency of solar systems, module level power management (MLPM) solutions are set for fast growth, with almost 40% of residential PV installations expected to use the technology in 2014, a new IHS iSuppli research indicates. Global shipments of MLPM systems, a category consisting of microinverters and optimizers, are set to rise to 6.2GW in 2014, up by nearly a factor of 40 from 160MW and by the end of 2014, 38% of residential PV installations worldwide will employ MLPM solutions, up from 2% in 2010. With the MLPM market still in its very early stages, competitors are starting to flood into the business. There are at least 15 companies in the MLPM space, with more coming over the horizon.

But on the business side, while new PV installations are expected to rise robustly in 2011, the road to growth will be bumpy, with inventories throughout the solar industry expected to surge in the first quarter because of a temporary dip in demand, , IHS believes. Stockpiles for materials and products across the PV supply chain are set to spike in the first quarter, as a result of a short-term softening in demand for new solar installations. Days of inventory (DOI) will expand by 22.9% for crystalline silicon (c-Si) modules and by 21.4% for thin-film (TF) modules. The industry average DOI for c-Si modules in the first quarter of 2011 will reach 48, up from 37 in the fourth quarter of 2010. DOI for thin-film modules during the same period will reach 41, up from 32 days.

PV modules are expected to suffer the most pronounced jump in inventories, but solar polysilicon, wafer and cell materials also will see DOI increases. These developments serve as an early indication of a looming overcapacity situation. However, the inventory spike will be confined to just the initial two to three months of the year.



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IRFHM830	30	Sync	PQFN 3x3	3.8	15
IRFHM830D	30	Sync	PQFN 3x3	4.3	13
IRFH7911	30	Control	Half-Bridge Asymmetric PQFN 5x6	8.6	8.3
		Sync		3.0	34
IRLR8729	30	Control	D-Pak	8.9	10
IRLR8726	30	Sync	D-Pak	5.8	15
IRF8714	30	Control	SO-8	8.7	8.1
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