PSD EUROPE

Power Systems Design: Empowering Global Innovation

April 2012

SPECIAL REPORT: MOTOR DRIVE, ROBOTICS & CONTROL (PG37)

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COVER STORY
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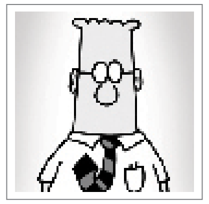

PSD EUROPE

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MOTOR DRIVES, ROBOTICS AND CONTROL

Our current theme and special-report focus is "Motor Drives, Robotics, and Control", which is well matched with the upcoming PCIM Europe Exhibition and Conference being held May 8 – 10 in Nuremberg, Germany. Here, the industry's key international players will meet. Conference attendees will get up-to-the-minute information on the newest trends and developments as well as state-of-the-art solutions for your most challenging problems.

Mesago Messe Frankfurt GmbH, organizers of PCIM Europe and PCIM Asia, are extending their global footprint with the launch of PCIM South America, to be held in Sao Paulo, Brazil this September 11 – 13.

While we are on the subject of PCIM Exhibitions and Conferences, PCIM Asia, which is being held in Shanghai, China this June 21 – 23, will feature a keynote address by Dr. Thomas Stockmeier, General Manager and Chief Technology Officer at Semikron. Power Systems Design (PSD) was granted an exclusive interview with Dr. Stockmeier. The content of this exclusive interview titled "Power modules gain from important new packaging materials and assembly technologies" is carried in full in this issue of PSDE.

Our special report delivers feature articles from the industries leading companies participating in this niche including Analog Devices, Cypress Semiconductor, Renesas, and On Semiconductor.

Lastly, we welcome Joshua Israelsohn to our editorial team. Joshua is our newly appointed Editor-in-Chief, Power Systems Design – North America. This addition to our editorial team strengthens PSD as the only global franchise dedicated exclusively to power electronics, with editors for each of our publishing editions and websites. China, Europe, and North America.

Please enjoy this issue of PSDE as well as our English website, www.powersystemsdesign.com and don't forget to catch Dilbert at the end of this issue. He continues to give us tremendous insight to the oddities of our industry.

Best Regards,

Jim Graham

Publishing Director, Power Systems Design
Jim.Graham@powersystemsdesign.com

ISABELLENHÜTTE PROVIDES FORMULA 1 TEAMS WITH CONTROLLED MEANS OF ACCELERATION

Nine top teams are using the IVT-F current sensor made by Isabellenhütte, during the 2012 Formula 1 season. The module has been integrated in the so-called E-KER systems: E-KERS is an Electric Kinetic Energy Recovery System that was used for the first time in 2009 and which was integrated in Formula 1 cars again for the 2011 season.

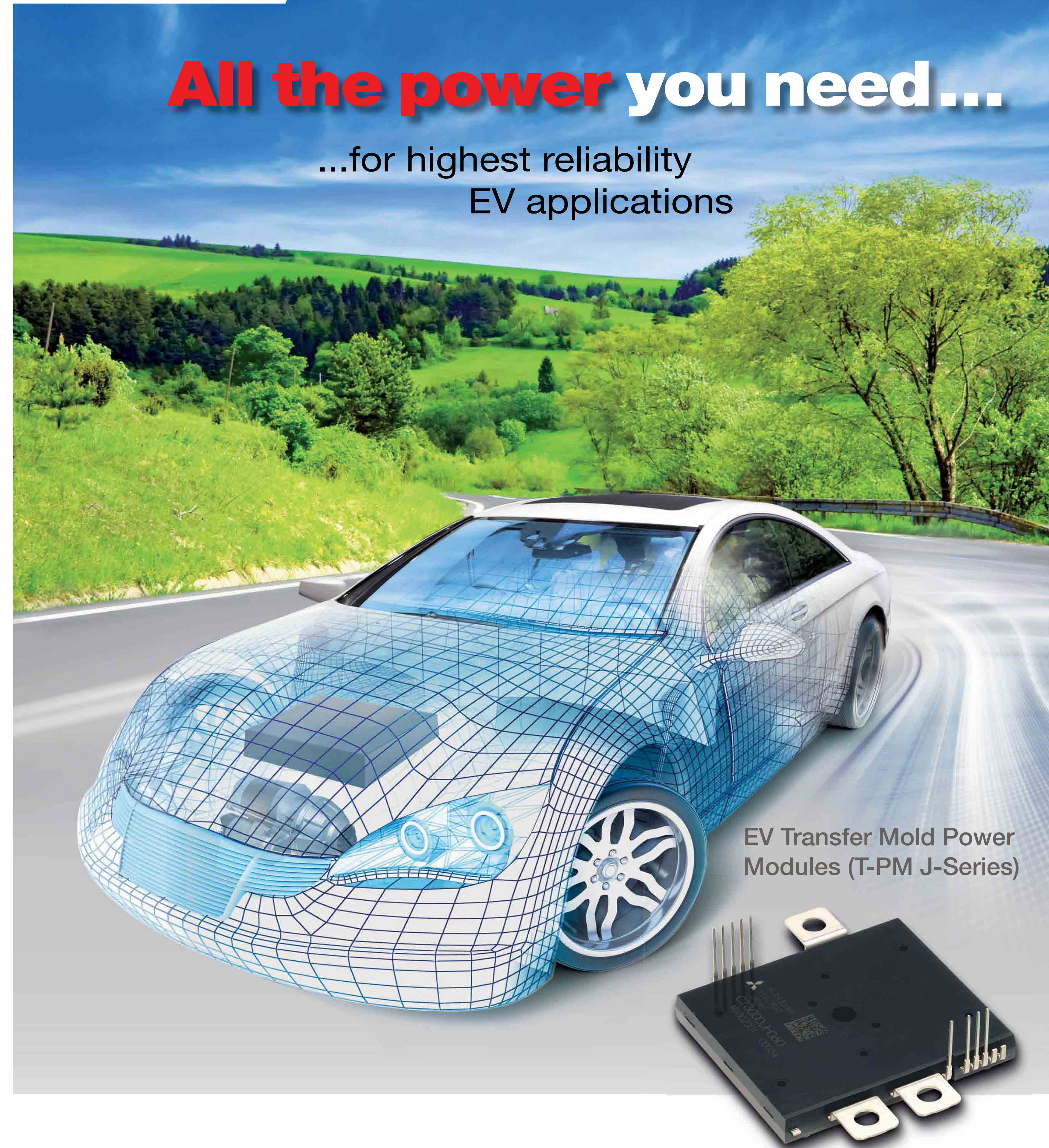
E-KERS forms part of the power transmission of F1 cars. It converts kinetic energy won during the breaking process into electricity with the help of an electric motor that also performs as a generator. This power is stored in lithium-ion batteries and fed back into an electric motor in strictly regulated quantities, which in turn boosts the Formula 1 car's combustion engine during acceleration periods. Isabellenhütte's IVT-F integrated current sensor controls the quantity of power supplied by the E-KERS. The Formula 1 umbrella organisation FIA (Fédération Internationale de l'Automobile) aims to ensure in this way that the racing teams will not use E-KERS to break the rules. It took just two months to develop the modules and they are specifically designed for use in Formula 1. Isabellenhütte's measurement segment aims to cement its position as technological leader in the field of shunt-based current measurement with these products.

Jens Hartmann, Sales Director Measurement at Isabellenhütte Heusler GmbH & Co. KG comments: "We are already working on sensors for the 2013 and 2014 Formula 1 seasons."

IVT-F technical data

- Three-channel measuring system for current, voltage and temperature (I,U,T)
- Internal sample rate: 3.5 KHz
- Fixed calculation of mean value over 16 sampling values
- U/I with input filter cut-off frequency of fg=350Hz
- 500 Hz measured value output
- CAN-Bus with 1 MBit data rate

www.isabellenhuette.de



AUTOMOTIVE LED LIGHTING - A LOOK TO THE FUTURE

By: Tony Armstrong

One of the key application areas driving significant growth in LEDs for illumination purposes is the backlighting of automotive displays. These TFT-LCD applications range from infotainment systems, gauge clusters and a wide array of instrument displays.

Of course, backlighting these displays with LEDs creates some unique LED driver IC design challenges in order to optimize display readability across a myriad of lighting conditions. This requires LED drivers to offer very wide dimming ratios and high efficiency conversion while also withstanding the rigors of the relatively caustic automotive electrical and physical environment.

LEDs are ten times more efficient at producing light than incandescent bulbs and almost twice as efficient as fluorescent lamps, including cold cathode fluorescent lamps (CCFL); thereby reducing the amount of electrical power required to deliver a given amount of light output (measured in lumens per watt). As LEDs are further developed, their efficacy, or ability to produce lumens of light output from an electrical power source, will only continue to rise.

The extended operating lifetime of LEDs allows them to be permanently embedded into the end-application. This is especially important for the backlighting of automotive clusters, instrumentation and infotainment panels - which are often embedded into a vehicle's dashboard, since they will not require replacement during the working life of the car. Furthermore, LEDs also have the ability to dim and turn on/off much faster than the human eye can detect, enabling significant improvements in backlighting of LCD displays while simultaneously allowing dramatic contrast ratios and a higher resolution picture.

Nevertheless, one of the biggest obstacles facing automotive lighting systems designers is how to optimize all of the features and benefits provided by this newest generation of LEDs. Since LEDs generally require an accurate and efficient current source and a means for dimming them, a LED driver IC must be designed to address these requirements under a wide variety of operating conditions. Further, their power supply solutions must be highly efficient, rugged and reliable while also being very compact and cost effective.

Many emerging automotive designs use a single panel to backlight all of the display gauges for driver control. Often, the LED backlighting for the instrument panel is shared with the infotainment system, creating an easy to read all-in-one control panel. Similarly, many vehicles including cars, trains and airplanes also have LCD displays that entertain passengers in the rearward seat(s) with movies, video games and so forth. Historically, these displays have used CCFL backlighting; however, it is becoming more common to replace these relatively large bulb designs with very low-profile arrays of white LEDs to provide more precise and adjustable backlighting as well as an extended service life.

In conclusion, the benefits of using LED lighting in an automotive environment has several positive implications. First, they never need to be replaced, since their solid state longevity is in excess of 100K hours – equivalent to 11.5 service years, thereby surpassing the life of the vehicle. This allows automobile manufactures to permanently embed them into "in cabin" backlighting without requiring accessibility for replacement. Yes, the future is bright indeed for automotive LED lighting.

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2015 LEGISLATION IMPACTS VARIABLE SPEED DRIVES MARKET NOW

By: Jenalea Howell

Nine top teams are using the IVT-F current sensor made by Isabellenhütte, during the 2012 Formula 1 season. The module has been integrated in the so-called E-KER systems: E-KERS is an Electric Kinetic Energy Recovery System that was used for the first time in 2009 and which was integrated in Formula 1 cars again for the 2011 season.

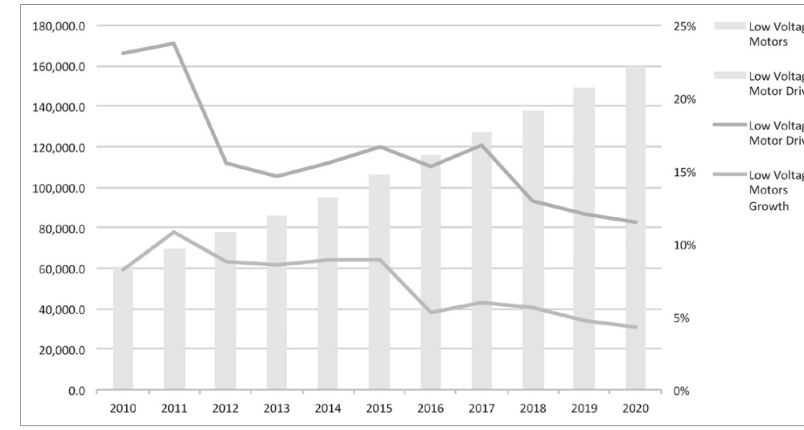
Although the mandate including variable speed drives is a few years off, I believe the impact on the market is beginning now and will gather momentum over the next three years, increasing the ratio of drives to motors shipped each year, due largely to the educational effect this legislation is having on purchasers.

Phase 1 of the ErP directive marked the transition to IE2 motors in 2011; however, slated to begin in January 2015 Phase 2 will require IE3 efficiency levels, either by changing to an IE3 motor or coupling an IE2 motor with a variable speed drive, and in 2017 Phase 3 will expand the motor ranges covered. Impacts on the drives market from this legislation is expected to occur in the following three stages:

Stage 1: Trickle Effect – In the short term, Phase 2 of the ErP directive is predicted to slowly ramp up demand for drives to 2015 as users begin to think increasingly more about motor efficiency in the context of a larger drive system (i.e. both the motor and the drive, the latter including electronic drives and gearing).

Stage 2: 2015 Mandate – Unlike the motors market reaction to Phase 1, the 2015 mandate will not create immediate high demand for drives as the current penetration of motors to drives rated between 7.5kW and 365kW, the range covered by this legislation, is already higher than average. As more drives than motors are shipped in these power ranges with a ratio of 1:1.4, it is clear that energy efficiency has long been a consideration in this segment of the market.

Stage 3: 2017 – Save the Date – Every drives supplier should have 2017 in their calendars, as Phase 3 of the initiative will expand to cover integral motors rated up to 7.5kW, representing 95% of motors shipped in 2010. Over 70% energy gains have been reported from installing a variable speed drive when beneficial to overall system



efficiency, while in stark contrast the efficiency difference between an IE2 and IE3 motor is much less. Ultimately, price will influence purchasing decisions and the drives market can benefit as in some cases an IE2 motor and drive will be cheaper than an IE3 motor.

The overall effect on the market is an increase in the motor to drive shipment ratio, currently estimated at 5:2 for the merchant sales in 2010. Ramping up to 2015 this ratio is projected to reach 2:1 and with a spike two years later, this ratio could easily reach 5:4 by 2020. As retrofit and replacement of drives are included, and also taking into account the shrinking life span of drives as electronics continually improve, it is important to note that the ceiling for penetration can surpass 100%. As the drives market steams on by 2025 it is conceivable more drives than motors will be shipped, with this ratio reaching 1:1.1 or higher.

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POWER MODULES GAIN FROM IMPORTANT NEW PACKAGING MATERIALS AND ASSEMBLY TECHNOLOGIES

By: Joshua Israelsohn, Editor-in-Chief, Power Systems Design

As power densities have increased across virtually all electronic products, some power-module applications have approached the limit of what traditional packaging materials and assembly technologies can support. In response, a large number of new packaging alternatives have emerged.

In advance of his keynote presentation at PCIM Asia 2012 this coming June, Semikron Elektronik GmbH Chief Technology Officer, Dr. Thomas Stockmeier, generously fielded questions on this topic from Power Systems Design:

PSD: Compared to typical periods in our industry's evolution, recently, there seem to be an unusual number of new power-module-assembly technologies coming to market. Do you see these as reflecting demands of disparate applications or are we seeing a fractioning of the market served until now by modules born of more traditional assembly technologies?

Dr. Stockmeier: Traditionally, power modules serve markets like industrial applications, automation, welding, power supplies, and other applications, where already a broad spectrum of power modules is necessary to accommodate the different power levels and circuit topologies. However, new applications, like hybrid and electric vehicles, as well as renewable energy have gained quite some momentum, which now rightfully request power modules tailored to their respective needs. Therefore, the market is not really fractioning more than in the past, but new fields are emerging.

PSD: Are the distinctions between competing assembly technologies sufficiently reflected in power modules' data sheets or do system designers need to be aware of the assembly technologies exploited by the power modules they specify? If the latter, how should such an awareness affect their module-selection process?

Dr. Stockmeier: Data sheets can only serve as a first order selection tool; the specific fit of the selected module has to be intensively tested and qualified. Data sheets will most likely not provide enough information to select the right power module without testing. Whereas the selection with respect to the right power handling capability can be determined with the help of simulation tools provided by module manufacturers, many other parameters, such as EMC, or reliability and durability for a specific environment are not possible to specify fully from the module supplier.

PSD: It appears that module manufacturers are exploiting many of the new assembly technologies to accommodate increasing maximum junction temperatures of the modules' various pass elements. Do wide bandgap semiconductors, such as SiC and GaN that claim better power-handling capability than traditional Si, depend on these new module-assembly technologies?

Dr. Stockmeier: The great advantage of wide bandgap materials, such as SiC and GaN, are their higher junction temperatures and much faster switching speeds. This may ultimately allow much higher power densities for many power electronic systems. However, traditional power-module-assembly technologies and designs cannot accommodate these needs. In particular, module manufacturers must develop new designs to address medium to high power applications.

PSD: If power-module manufacturers are beginning to exploit multiple and diverse packaging materials and assembly techniques, will the market not necessarily see increasing module costs across the board due to falling economies of scale?

Dr. Stockmeier: One has always to consider the system cost, which power modules must help decrease. For example, if the power module allows much higher power density and switching frequency, power-subsystem designers can dramatically reduce the size and cost of filtering. Therefore, some shift in cost from filter to power module may become acceptable. Lower system cost also results from functional integration in power devices, eliminating expensive electrical, thermal, and mechanical interfaces. Again, the power module may have higher cost, but the overall system cost is less. Another benefit: fewer interfaces and less material yields higher reliability.

PSD: Do you see power modules for specific applications—such as automotive, communications base stations, or computational server farms—clustering around specific packaging and assembly technologies or do applications draw from the full width and breadth of available packaging materials and assembly methods?

Dr. Stockmeier: I don´t think that a specific market will exhibit its own specific set of materials and technologies. One example: recently, we completed a study on power modules for the main electric drive in automotive applications. We found all possible ways of applying materials, technologies, and packages. What we have to be careful about is that we don´t re-invent the wheel many times. Precompetitive research and development and co-operation across application fields become a necessity. Initiatives like ECPE (the European Center for Power Electronics) are exemplary.

PSD: Often, when a technology sector sees a sudden increase in the number of technologies competing to solve a given problem, there follows a fierce battle between them followed by significant consolidation. Will the recent bumper crop of innovations in power-module packaging follow this classic trend or is there a sufficient market niche for each?

Dr. Stockmeier: Has the power-module market ever really consolidated technologies or designs? I see new functions, forms, and fits of power modules at every PCIM show. Very rarely do I see the discontinuation of specific power devices. The reason is that the market is still fast growing. While old designs and technologies serve existing production, which may go on for decades, new projects need and incorporate new technologies for lower cost, higher power densities, and higher reliability. Maybe what we see is not a technology bump, as you call it, but the beginning of an even more diverse (and complicated) world.

PSD: Given the growing cost sensitivities in many of the end applications, are specific assembly technologies gaining an edge as the pressures of commercialization come to bear?

Dr. Stockmeier: Power modules are very sensitive to material cost. Module manufacturers achieve cost reduction by using less material (such as a module without a base plate), improved thermal conductivity to enable chip shrink, and functional integration to eliminate interfaces. Secondly, large production volumes are required to justify a high degree of automation, to gain productivity, and leverage supply. Any technology that serves these purposes has an edge.

PSD: Evidently, reliability concerns have been key drivers for many of these innovations. Of course, power modules are not the only components subject to failure due to high-temperature operation and thermal-cycling stress. How can innovations in power-module packaging inform developments in packaging technologies for complex integrated circuits?

Dr. Stockmeier: I don´t think, integrated circuits are our greatest headache in high temperature operation. IC technology provides suitable packages and continues to develop even better ones. Of much greater concern are, for example, capacitors, current sensors, and PCBs.

PSD: Are most power-module manufacturers exploiting new materials and assembly methods or are only a few vendors commercializing these new technologies?

Dr. Stockmeier: All power module manufacturers very actively research and develop new materials and assembly technologies. This makes our technical community so interesting and makes shows and conferences such as PCIM so vivid. Whereas the overall goals are most likely the same for all manufacturers, the ways to solutions are different. All vendors intend to commercialize these technologies – sooner or later.

PSD: If the current power-density trend continues, will it force power-module manufacturers to adopt hermetic packaging methods? How are innovations in non-hermetic packaging staving off that outcome?

Dr. Stockmeier: High power density does not require hermetic packaging. Much higher power density can be achieved by liquid cooling technologies, either integrated or discrete. Hermetic packages, on the other hand, are necessary in harsh environments and, there, all other components of power-electronic circuits require consideration, as well. If the power density of modules increases drastically, and designs can considerably reduce the filter size, the compartment that houses the entire power electronic system may become much smaller. Therefore, it may be more useful to look at a suitable sealing for the entire (small) compartment, rather than just looking for hermetically sealed power modules.

PSD: Thank you, Dr. Stockmeier; we look forward to your keynote address at PCIM Asia 2012.

Joshua Israelsohn, Editor-in-Chief, Power Systems Design

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MANUAL FREQUENCY RESPONSE MEASUREMENTS FOR MAGNETICS

By: Dr. Ray Ridley

In this article, Dr. Ridley describes how you can make frequency response measurements of transformers and inductors using equipment that you probably already have in your laboratory. This is very important for students and very small companies who cannot afford the sophisticated equipment needed for more serious production level work and for high-speed development.

The Importance of Impedance Measurements

While still a student at Boston University, I was fortunate to enroll in a machines class which was taught in the Franklin Institute. The course was very hands-on, involving ac motors, transformers, and generators, in a laboratory that had been in place for decades. To this day, I clearly remember many aspects of the lab due to the immediate and interactive nature of the experiments.

One of the first things that we did in the lab was to plot a transfer function of transformer and motor windings in order to extract important equivalent component values needed for design and analysis. This process was always a fundamental first step in doing any experimental work. The experiments were performed using basic laboratory equipment, using an analog signal generator and analog oscilloscope.

Once I started work in power supply design, I applied the same philosophy when building hardware. All magnetics should be properly characterized over a wide range of frequencies in order to extract important parameters. During the design phase, these parameters are very important. Later on, during the transition from design to manufacturing, the characteristic frequency response curves are a powerful and sensitive tool to determine proper construction of magnetics.

Ideally, the measurements of magnetics impedance should be made with a properly calibrated and automated piece of test equipment [1]. However, many students of power electronics, and engineers just starting their careers or their own companies do not have access to anything but the most basic of laboratory instruments. Even in this situation, it is highly recommended that the impedances of magnetics be properly measured and recorded. It may be a time-consuming process, but it is very important

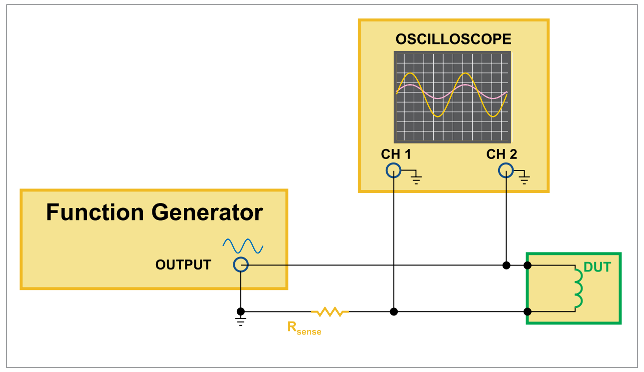

Fig. 1: Schematic of how to measure frequency response of magnetics using a signal generator and oscilloscope.

for understanding of your circuit, and repeatability of design.

Manual Setup of Impedance Measurements

Figure 1 shows the recommended test setup for measuring magnetic components. The device under test is connected in series with a 1-ohm test resistor, and a signal applied across the series combination. The voltage across the 1-ohm resistor, representing the current, is measured with one channel of an oscilloscope, and the voltage across the series combination measured with the second channel. Figure 2 shows a photograph of the actual lab test setup.

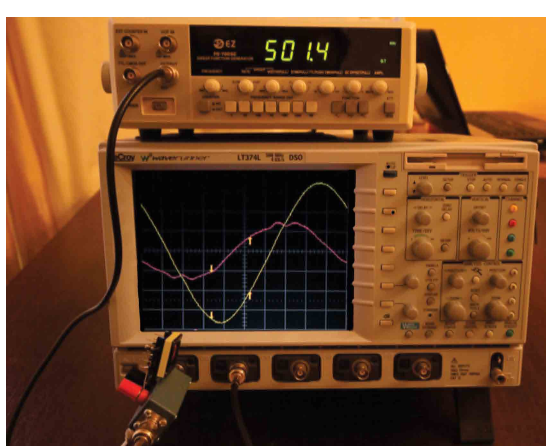

Fig. 2: Photograph of manual magnetics impedance test setup.

A small test fixture containing the sense resistor was used to improve RF layout issues of the test setup.

I always recommend people with limited budgets use this test setup, but it is actually an experiment that I have not done for over 25 years. I have to admit that I encountered some surprises when revisiting this technique in preparation for this article:

1. Modern signal generators are not as clean as the older pure analog signal generators. Switching techniques generate noise and distortion, especially at higher frequencies. The effect of this can be seen in the waveforms of Figure 2 where high-frequency resonant harmonics are excited.
2. Modern low-cost oscilloscopes do not do a good job of rejecting high-frequency noise, and the noise floor is quite high. The 20 MHz bandwidth limiting function does not work as effectively as it should. The oscilloscope used in Figure 2 is a high-quality instrument from LeCroy, necessary for good noise performance.
3. Switching power supply noise is EVERYWHERE in today's world, and it will show up in your measurements. Most bench equipment includes switching power supplies, and these are filtered with varying degrees of success. Computer adaptor and power supplies also contribute to this noise.
4. It takes longer that I ever remembered to make hand measurements. An average of around 4 minutes per data point was needed when phase data was also recorded, and more time was needed with distorted waveforms.

Frequency kHz	Channel 1 (A)	Channel 2 (V)	Impedance (Ohm)	Impedance (dB Ohm)
0.1009	0.400	0.431	1.078	0.648
0.1996	0.403	0.435	1.079	0.664
0.4005	0.406	0.485	1.195	1.544
0.8007	0.406	0.681	1.677	4.492
1.610	0.406	1.162	2.862	9.134
4.061	0.406	2.680	6.601	16.392
8.262	0.387	5.060	13.075	22.329
10.39	0.381	6.180	16.220	24.201
20.16	0.337	10.350	30.712	29.746
40.30	0.253	15.130	59.802	35.534
81.76	0.157	18.300	116.561	41.331
106.0	0.129	19.000	147.860	43.397
201.6	0.073	20.400	279.835	48.938
503.4	0.028	20.900	757.246	57.585
741.0	0.015	20.900	1352.751	62.624
1059	0.008	20.600	2658.065	68.491
1586	0.004	19.900	5076.531	74.111
2124	0.006	19.500	3266.332	70.281
3016	0.010	18.100	1727.099	64.746
5340	0.022	16.300	747.706	57.475

Fig. 3: Table of data collected with manual measurements.

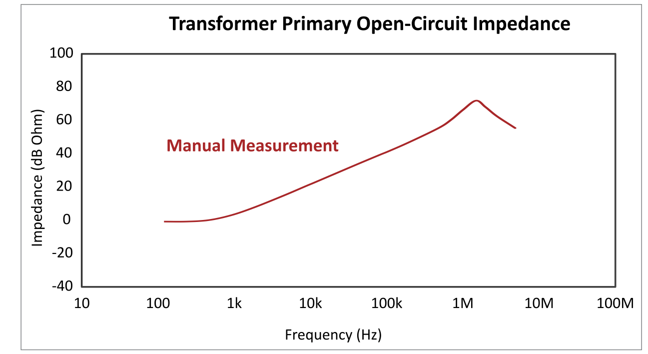

Fig. 4: Open-circuit manual impedance measurements of transformer.

Experimental Results with Manual Impedance Measurements

Data was collected for a sample forward converter transformer, and this data is shown in the Table of Figure 3.

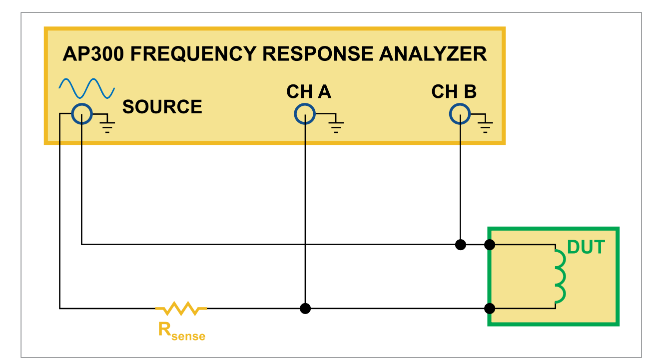

Fig. 5: Schematic of test setup for measuring magnetics impedance with AP300 Analyzer.

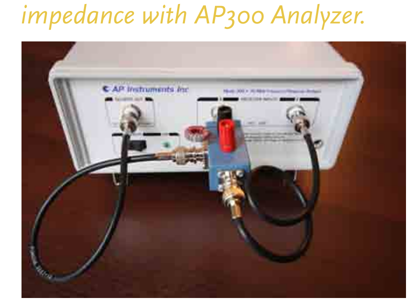

Fig. 6: Photograph of magnetics test setup with AP300 Analyzer.

Figure 4 shows the plot of the impedance versus frequency. A smoothed curve chart was selected within Excel to plot this data. The total time required to collect the data and plot the points was approximately one hour. This did not include recording phase data.

Comparison of Manual and Automated Impedance Measurements

Figure 5 shows the automated test setup schematic using the AP300 Analyzer, and Figure 6 shows a photograph of the actual hardware used. The same impedance test fixture was used as for the manual measurements.

Figure 7 shows the plots of both the manual and automated measurements of the primary transformer impedance. At frequencies from 1 kHz to 5 MHz, the two techniques gave very good agreement, validating the usefulness of the manual approach. Resonant frequencies were very similar, with any difference attributable to calibration errors in the signal generator.

Below 1 kHz, the primary impedance dropped below 1 ohm. The raw data does not show how much of the impedance was due to the sense resistor, and how much due to the winding impedance. In order to extract this data, you can use a lower value sense resistor to extend the measurement range. Alternatively, you can collect phase data at each frequency point, then subtract the value of the sense resistor when post-processing the collected data values. This was not done for the curves of Figure 7.

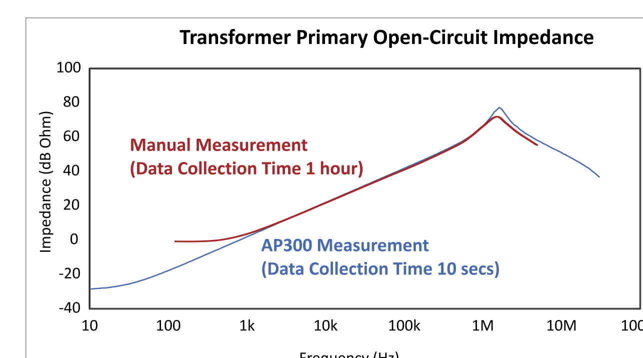

Fig. 7: Comparison of manual transformer Open-Circuit impedance measurements and automated measurements with the AP300.

The signal generator used had a maximum frequency of just 5 MHz, and a better piece of equipment is needed to extend the frequency range to see the full characteristics of the magnetics component.

While the data collected manually was very good, the big drawback

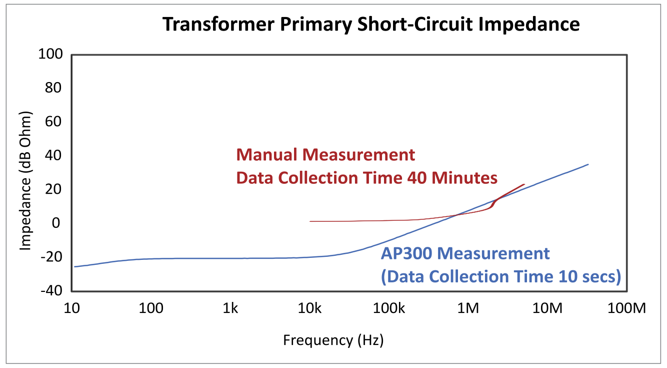

Fig. 8: Comparison of manual transformer Short-Circuit impedance measurements and automated measurements with the AP300.

of this technique was the amount of time needed to collect accurate data. It took over one hour to accurately measure and plot the data. The AP300 analyzer collects the same information, plus phase data, in under ten seconds. This time saving becomes very important when you are doing real production work. However, for university work, and initial experiments, the manual technique is very useful.

Manual and Automated Short-Circuit Impedance Measurements

Manual impedance measurements were also collected with the secondary of the forward transformer shorted. This greatly reduced the impedance level of the measurements, and created problems in getting accurate results. The biggest issue was with the distorted output of the signal generator when driving the low impedance of the shorted transformer.

Figure 8 shows the results of both the manual and automated measurements with the secondary of the transformer shorted. The manual results were not nearly as good due to the difficulty in getting accurate measurements. It was very difficult to get accurate phase measurements with the distorted waveforms.

Improvements can be made with a better signal generator, and with a lower value sense resistor. Often you will find that older laboratory equipment will do a better job than some of the modern designs.

When measuring short-circuit impedances, phase information is much more important to collect since the leakage inductance parameter is a nonlinear element which changes with frequency. You cannot just look at the magnitude of the impedance curve and assume 90 degrees phase shift. Calculation of the leakage inductance at each frequency requires both gain and accurate phase information.
Only ten data points were collected for the manual measurements, and this took about 45 minutes. This is compared to just 10 seconds with the AP300 automated measurements. With more complex impedance curves, such as that shown in Figure 9, many more data points must be collected to completely record the full impedance characteristics of the magnetics.

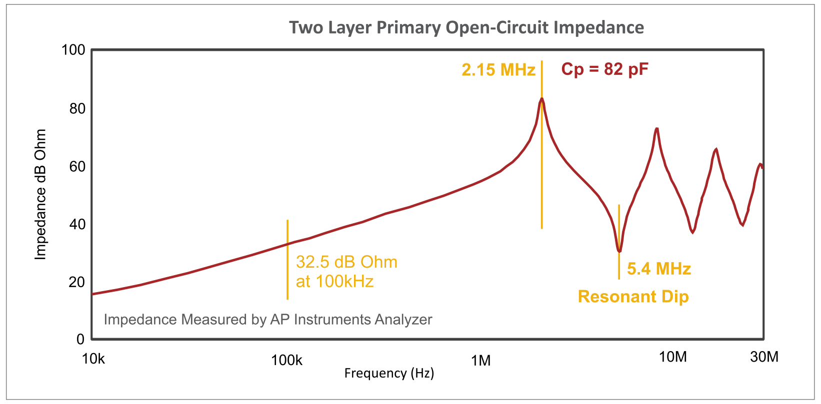

Fig. 9: More complex flyback transformer primary impedance measurements.

Manual measurements of such an impedance characteristic would take a couple of hours if you want to accurately reproduce the true characteristics of the device.

While the impedance measurements require either time or budget for good equipment, they ultimately save you time and money in your project by guaranteeing that you have maintained consistency of manufacturing from one sample to another.

Summary

Magnetics impedance measurements should always be made for switching power supplies, whether you are a student, an engineer at a small company, or working for a large organization. If you cannot afford the proper automated test equipment, you should spend the time necessary to collect data manually with the techniques described in this article. The frequency response curves are an important record of your design process, and a good way to evaluate later design iterations of magnetics.

As you move to towards production and more serious design work, you will find that your time becomes more valuable, and more accurate equipment is needed to speed up your design process. At some point you will find that the manual data collection process takes more time than you can afford.

Ridley Engineering Design Center,

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THE STATUS OF GaN BASED POWER DEVICE DEVELOPMENT AT INTERNATIONAL RECTIFIER

A Truly Revolutionary Technology

By: Michael A. Briere, ACOO Enterprises LLC, under contract with International Rectifier

There are relatively few opportunities in one's career to participate in the development of a truly revolutionary technology in a chosen field. The past 8 years have been such an opportunity for this author through the development of GaN based power devices. Over three and a half years ago, International Rectifier announced that it was working on a program, named GaNpowIR ®, focused on the development of power devices for use in applications between 20 and 1200 V, based on the AlGaN-GaN high electron mobility transistor (HEMT), using cost effective hetero-epitaxy on silicon substrates and silicon CMOS foundry compatible device fabrication.

At the time, a projected time frame for the development of 600 V devices was the end of 2011. It is with a tremendous sense of pride in the accomplishment of the IR GaN team that this milestone was reached. Large area, high current devices were developed, meeting all performance criterion and have been provided to select OEM power supply partners for additional rigorous and independent application evaluation and further product definition refinement.

Amongst the significant technical challenges that were met to achieve this goal of commercially viable 600 V capable GaN based power devices was the development of hetero-epitaxial techniques to provide reproducibly crack free, thick (e.g. > 4.5 um) III-N epi on large diameter (150 mm) silicon wafers of standard thickness with resulting bow of less than 30 um. In addition, reduction of the drain to gate and drain to source leakage currents to below 1 nA/mm of gate periphery at the device rating of 600 V was achieved. The resulting devices exhibit an Ion/Ioff ratio of greater than 10 Million. Further, the essential elimination of transient charge trapping phenomena associated with such effects as drain current collapse and dynamic Rdson has also been accomplished. Finally, sufficient field engineering has been developed to provide long term reliability under applied drain bias stress, necessary to satisfy the rigorous commercial standards developed for silicon based incumbent devices.

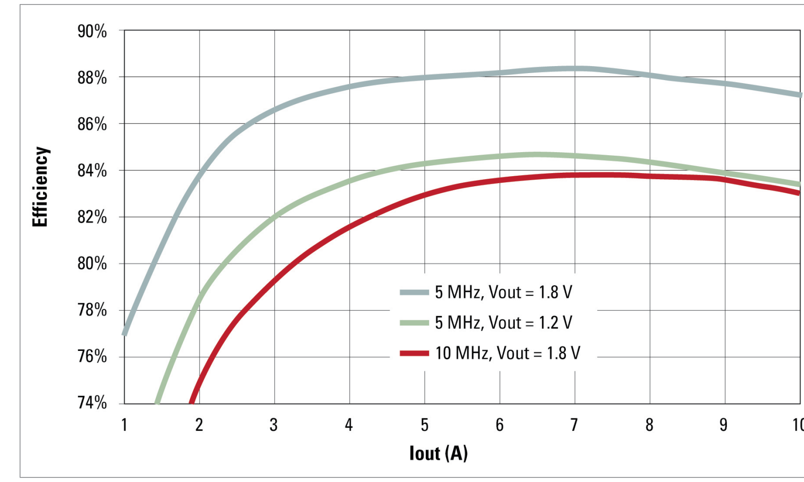

Figure 1 : Measured efficiency of a high frequency 12 Vin to POL buck converter, including output filter losses, using low voltage GaN based power devices.

The 600 V application node is particularly important since it represents some 40 % of the entire market for power semiconductors between 20 and 1200 V [2], as well as an obvious performance to cost advantage of GaN based devices over the silicon incumbents, where the potential performance improvement is 10 to 100 fold [1]. Current social and economic emphasis on energy conservation is easily satisfied by the significantly improved circuit efficiencies as well as higher density and lower system costs achieved using such GaN based power devices in applications ranging from ac-dc power supplies, inverters for photovoltaics and motor drives for appliances as well as in primary and auxiliary power converters in electric vehicles.

It is likely for this reason that the advent of commercially viable 600 V devices has received considerably more attention than that of the low voltage device developments provided in functional block, buck regulator power stage modules, as announced in early 2010. It is, however, the author's present contention that the low voltage GaN based solutions will have a significant impact on both the power semiconductor market place and the associated computing applications within the next 5 years. The significance is due, in part, to the fact that 20-40 V switch applications also represent some 40 % of the previously mentioned targeted total power semiconductor market between 20 and 1200 V [2]. In addition, this author argues that only GaN based devices offer the potential for efficient (> 88 %) single stage compact conversion (12 Vin to 1.2 Vout) which will be required to effectively support future many core (> 32) micro-processor architectures, using conversion switching frequencies of greater than 30-50 MHz [3]. The present results using first generation commercial low voltage devices (RonQg = 30 mohm nC) in a 12 Vin to POL Vout converter are shown in Figure 1. Here it can be seen that excellent efficiency response of 88% is found across a wide load range at 5 MHz for Vout of 1.8 V and a record performance of 84 % efficiency is achieved at 10 MHz. As discussed previously [3] while silicon based devices, with a technological RonQsw limit of more than 20 mohm nC, are physically limited to about 3 MHz for a 12V to 1 V conversion with 88% efficiency, it is possible for GaN based HEMTs to support efficient switching, with these criteria, to > 30 MHz. In fact the current goal is to achieve 2 to 3 mohm nC performance, a factor of about 4 more than the calculated technological limit, within the next 5 years.

The mid-voltage power device

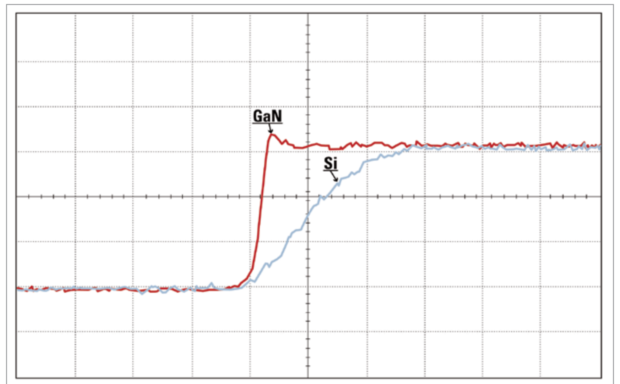

Figure 2 : Measured switch-node waveform comparing GaN based 100 V devices to best in class silicon based alternatives. Y axis is 20 V/div and X axis is 10 ns/div.

market, for commercial application from 60 to 250 V, is highly fragmented and represents only some 10 % of the target market for power semiconductors [2]. For this reason, it has received less attention than either the 20 to 40 V or the 600 V rated device development activities. Even so, there are remarkable advantages for GaN based devices over silicon incumbents in this voltage application regime. One example is the class-D audio amplifier application with bus voltages of 60 to 100 V. In this bus range, 100 to 150 V rated devices are most often used in symmetric half bridge topologies. Exhibiting considerably less (e.g. 40 % less in first generation devices) output charge, GaN based devices switch much faster than comparably rated silicon based devices, as shown in Figure 2 for a +/- 35 V bus and 100 V rated devices. Consequently the fidelity of the amplified PWM signal is far superior. Shown in Figure 3 is a measure of the amplifier fidelity in total harmonic distortion across the applicable spectrum. As can be seen, the GaN based amplifier provides superior audio fidelity compared to the best in class silicon alternative. In addition, the GaN based solution provides improved power

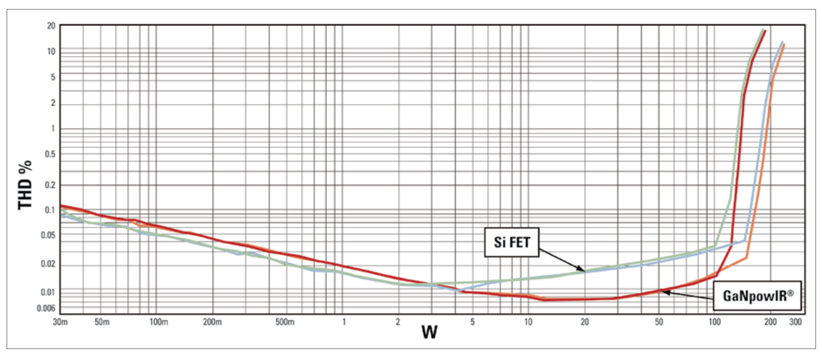

Figure 3: Measured total harmonic distortion spectrum for a nominally 160 W class D audio amplifier, showing improved fidelity using 100 V rated GaN based devices versus best in class silicon alternatives.

conversion efficiency across the entire load range of between 1.6 % at light load and more than 1 % at full load. In this case, despite the fact that these early GaN based devices are housed in a thermally inferior package, compared to the silicon devices which leverage the thermally optimal DirectFET® package, the GaN solution is more than 10 C cooler at the operational load (1/8 clipping).

In its first generation, IR's 600 V rated GaN based switches exhibit a factor of four improvement in conduction loss * switching loss performance, compared to best in class 600 V rated silicon based superjunction FETs as well as state of the art trench Insulated Gate Bipolar Transistors (tIGBTs). As in the case of the mid voltage devices, IR's 600 V rated switches are constructed as a two component cascode composite device. The first component, the native depletion mode GaN HEMT, is arranged in series with a low voltage silicon MOSFET, where the source of the silicon device is connected to the gate of the GaN HEMT and the source of the GaN HEMT is intimately connected to the drain of the silicon MOSFET. In this way, the inverse of the voltage developed across the silicon device is presented across the gate-source terminals of the HEMT. Amongst the many advantages of this compound device configuration is the freedom to drive the resulting switch in the same manner as more than 30 years of experience in driving silicon switches has made the circuit designer accustomed. Therefore, standard drive circuitry can be used and threshold voltages can be selected as required for the circuit environment (e.g. from logic level to +4.5 V, as commonly used in industrial or very noisy circuit environments).

As has been discussed previously [1], a GaN based 600 V rectifier can be similarly constructed by substituting a low voltage silicon diode instead of the FET. Since the wide bandgap III-N material has few minority carriers to effect switching behavior, the resulting rectifier behaves very much like a SiC diode, where the small reverse recovery charge is dominated by essentially temperature independent capacitive contributions. The low voltage silicon diode contributes only a small percentage to the total reverse recovery behavior. In this way, high performance rectifiers are possible at a fraction of the current SiC diode costs.

This composite switch changes state very fast, since the GaN has a high transconductance (e.g. 300 mS/mm gate width) and the effective GaN gate drive on-resistance is that of the silicon companion device (e.g. mohms). It is important to take adequate care of the potential parasitic inductances, present both within the switch packaged assembly and in the surrounding

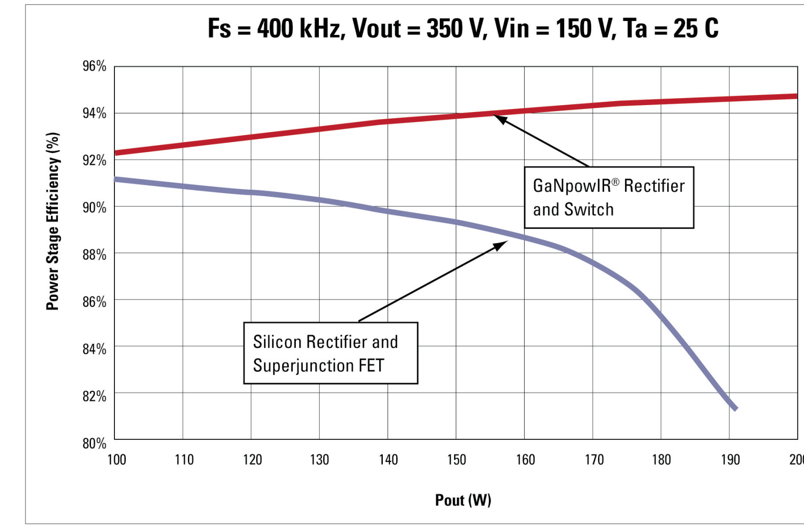

Figure 4 : The measured room temperature efficiency for a nominally 200 W power factor correction boost power stage, including inductor losses, operating at 400 kHz with Vin = 150 V and Vout = 350 V using either IR's GaN based devices or best in class silicon alternatives.

circuit layout, so as to effectively minimize ringing often associated with very fast switching. Demonstrating excellent device robustness beyond the nominal device dc bus rating of 480 V, such devices exhibit very clean switching behavior from a 600V dc bus despite greater than 50 V/ns transition rate for a packaged cascade switch in a power factor correction application circuit. Similarly clean waveforms have been found for transition rates approaching 100 V/ns for nominally rated 430 V bus voltages.

The fast transition rates allow for significant reductions in the switching losses using GaN based cascade switches. This can be seen in Figure 4, showing the efficiency improvement for GaN based switches and rectifiers in a nominally 200 W power factor correction boost circuit (150 Vin to 350 Vout) operating at 400 kHz, used in the front end of an ac-dc power converter, compared to the case of a state of the art silicon based superjunction FET and fast recovery diode used in the same circuit. As is well known, the higher operating frequency allows for significant reduction in the size and cost of the output filter L and C components, providing for a much higher density and lighter weight converter.

Another example of the advantages of using GaN based devices is shown in Figure 5, where the efficiency of a resonant LLC converter of 300 Vin to 30 Vout is operated at 400 kHz using either GaN based switches on both the primary and secondary side of the transformer, or best in class silicon alternatives. As can be

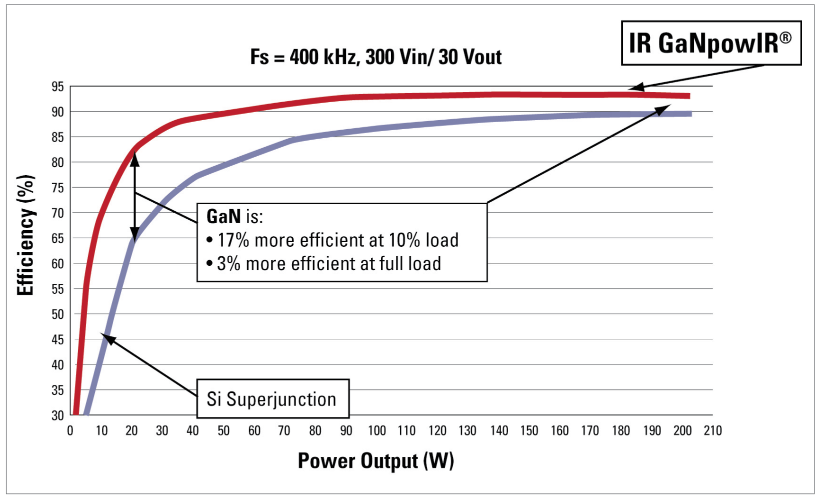

Figure 5: Measured conversion efficiency for a resonant LLC converter with Vin = 300 V and Vout = 30 V operating at 400 kHz, using either IR's GaN based devices on both the primary (600 V rated) and secondary side (100 V rated) of the transformer (with synchronous secondary side rectification) or state of the art silicon alternatives.

seen, there is significant gain in conversion efficiency at both light (17 %) and full (3 %) loads.

Such dramatic improvements in circuit efficiency and density are of course only modest examples of the potential impact of GaN based power devices on the power electronics industry. As it is expected that at least a further ten fold improvement in the performance characteristics of these devices are possible, revolutionary advances are expected in the future. Though this will most likely begin through the straightforward substitution of silicon incumbents with GaN based devices, the truly radical advances will occur when circuit topologies are designed specifically to take advantage of the unique attributes of the GaN based power devices. Besides the relatively ideal switching characteristics, recognition of the advantages of the inherently bi-directional nature of the GaN HEMT, the linear scalability of performance with voltage rating, as well as the inherent integratability of GaN based power devices will promote new architectures previously considered impractical, if previously considered at all. Given the cost effectiveness of the integratable GaN-on-Si technology platform, it is conceivable that future power conversion circuits will involve hundreds of power devices, instead of the current few. It is certainly an exciting time to be involved in the power electronics industry.

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FLYBACK CONTROLLER INCORPORATES ACTIVE PFC INTO A SINGLE STAGE CONVERTER

Power systems operating from the AC mains has an associated power factor

By: Bruce Haug

Any power system operating from the AC mains has an associated power factor defined as the way it draws current from the source. The power factor of an AC electric power system is defined as the ratio of the real power flowing to the load to the apparent power and is a dimensionless number between 0 and 1.

Real power is the capacity of the circuit for performing work in a particular time. Apparent power is the product of the current and voltage of the circuit. Due to a non-linear load that distorts the wave shape of the current drawn from the source, the apparent power will be greater than the real power.

In an electric power system a load with a low power factor draws more current than a load with a high power factor for the same amount of useful power transferred. These higher currents increase the energy lost in the distribution system and require larger wires and other equipment for transmission. Because of the costs of larger equipment and wasted energy, electrical utilities charge a higher price where there is a low power factor. Furthermore, a power supply's power factor affects the harmonics that an AC-DC supply generates on the AC mains, and so electric utilities have major difficulties distributing power for loads that include AC-DC power supplies without power factor correction. These power supplies are nonlinear loads which:

- Distort the AC waveform.
- Cause harmonics currents that can impact operation of other equipment on the same utility line.
- Can cause fires from neutral wires overheating.
- Can overstress and shorten the lives of power transformers.
- Can overload AC-power generators.

Starting in the 1980's, the European Union decided to place the burden for solving these problems upon the manufacturers of products employing AC-DC power supplies. Since then, it has

Class	Category	Remarks
A	Electronic equipment	• Balanced 3-phase equipment • Household appliances excluding equipment identified as class D • Tools, excluding portable tools • Dimmers for incandescent lamps • Audio equipment • All other equipment not classified as B, C, or D
B	Portable tools	Non-professional arc welding equipment
C	Lighting equipment	Except incandescent lamp dimmers
D	PC, PC monitors, radio, or TV receivers	Input power from 75 to 600W and ≤16A/phase

Table 1. IEC 61000-3-2 Classifications

undergone several revisions to set standards for limiting the amount of current products may draw at harmonics (integer multiples) of the powerline frequency. This resulted in the IEC61000-3-2 Harmonic Line Current Emissions standard classifications as shown in Table 1.

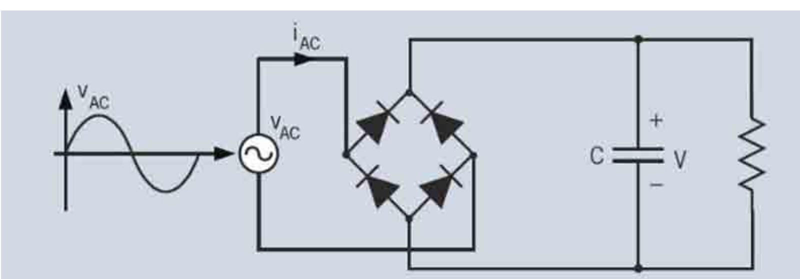

Figure 1. Switching Power Supply Input Circuit

A typical off-line power supply loads the AC mains power line with a diode bridge driving a capacitive load as shown in Figure 1. This load is nonlinear due to it primarily charging a capacitor and this type of load draws line current only during the peak of the sinusoidal line voltage, resulting in line current input peaks that cause power line harmonics.

Power Factor Correction (PFC)

One way to improve the power factor is to use a filter. This is commonly referred to as passive PFC. It is possible to design a filter that passes current only at line frequency (e.g. 50 or 60 Hz). This type of filter is normally used for low power requirements and reduces the harmonic current, which means that the non-linear device now looks like a linear load and the power factor can be brought to near unity, using capacitors or inductors as needed. However, this type of filter requires large-value high-current inductors, which are both bulky and expensive.

Active PFC

Active PFC is a power electronic system that controls the amount of imaginary power drawn by a load in order to obtain a power factor as close to unity as possible. In most applications, active PFC controls the input current of the load so that the current waveform is proportional to the mains voltage waveform (a sine wave). Active PFC normally consist an extra switching boost converter power stage that requires a control IC, switching MOSFET and power inductor. Active PFC puts the voltage and current nearly in phase and the reactive power consumption approaches zero. This enables the most efficient delivery of electrical power from the power company to the user. Figure 2 shows what the current to an off-line switching power supply looks like without PFC and what it looks like with active a PFC of 1.0.

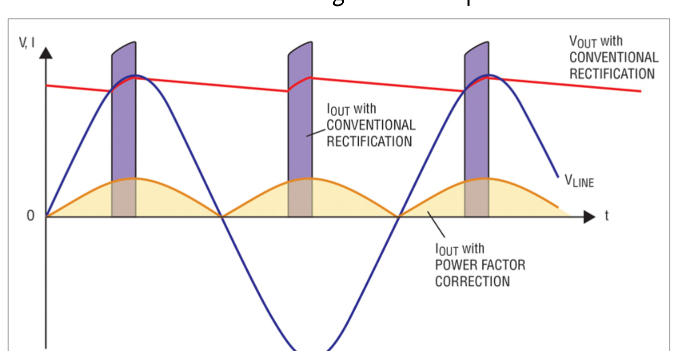

Figure 2. AC Voltage & Current Waveforms with & without Active PFC for a Capacitive Load

Up until now power supply designs have required the used of an addition power stage to incorporate PFC. Whether it's active or passive PFC, additional components have been required which increases the cost, circuit size and complexity. However, Linear Technology recently announced a revolutionary isolated flyback controller that combines active PFC into a single stage converter without the need for additional components.

Introduction

The LT3798 is a constant current/constant voltage isolated no-opto required flyback controller with single stage active PFC. A power factor of greater than 0.97 can be achieved by actively modulating the input current, eliminating the need for an extra switching power stage and associated components. In addition, no optocoupler or signal transformer is required for feedback since the output voltage is sensed from the primary-side flyback signal.

A LT3798-based design easily complies with most Harmonic Current Emissions specification. Efficiencies greater than 86% can be achieved with output power levels up to 100W. The device's input voltage range is dependent on the choice of external components and it can operate over a 90VAC to 307VAC input voltage range and can be easily scaled to higher or lower input voltages. Furthermore, the LT3798 can be designed into high input voltage DC applications, making it well suited for industrial, EV/EHV automotive, mining, and medical applications. The LT3798 utilizes critical condition mode operation enabling the use of a smaller transformer compared to continuous conduction mode designs, further reducing the solution size. The LT3798 is comes in a thermally enhanced 16-pin MSOP package.

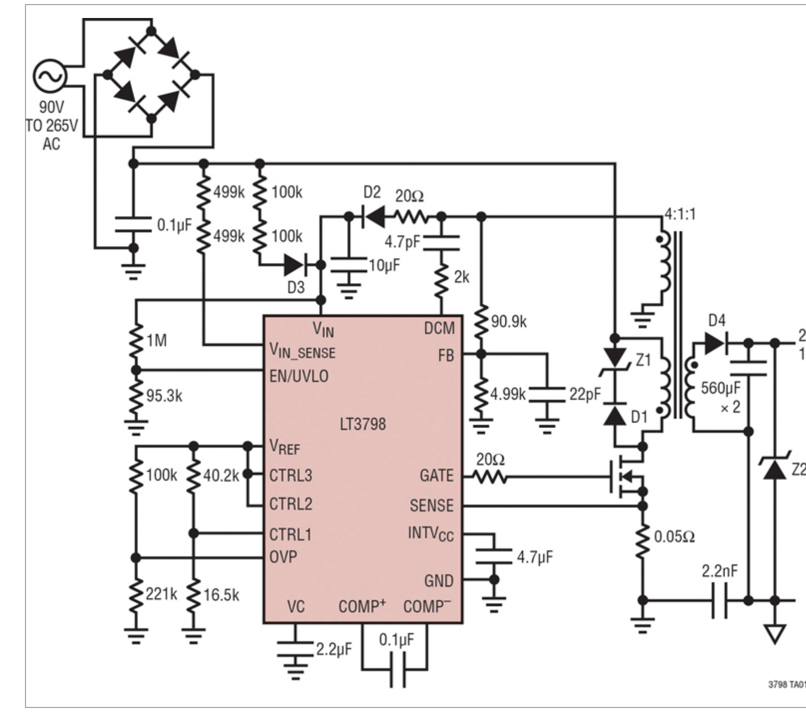

Figure 3. LT3798 as a Universal Input 24W PFC Bus Converter

Figure 3 shows a typical application circuit for the LT3798 which converts a 90 to 265VAC input voltage to 24V @ 1A output. This IC is a current mode switching controller that is specifically intended for generating a constant current/constant voltage supply with an isolated flyback topology. To maintain output voltage regulation this design senses the output voltage from the second primary-side transformer winding.

The LT3798 eliminates the need for an optocoupler, opto driver and secondary-side reference voltage, all while maintaining isolation between primary and secondary with only one part having to cross the isolation barrier. It also employs a primary-side sensing scheme that is capable of detecting the output voltage through the flyback primary-side transformer winding. During the switch off-period, the output diode delivers the current to the output, and the output voltage is reflected to the primary-side of the flyback transformer. The magnitude of this reflected voltage is the summation of the input voltage and output voltage, which the LT3798 is able to reconstruct.

During a typical cycle, the gate driver turns on the external MOSFET so that a current flows in the primary winding. This current increases at a rate proportional to the input voltage and inversely proportional to the transformer's magnetizing inductance. The control loop determines the maximum current and a comparator turns off the switch when it reaches that current. When the switch turns off, the energy in the transformer flows out the secondary winding through the output diode, D4 (refer to Figure 3).

LT3798 Power Factor Correction

The LT3798's VIN_SENSE pin connects to a resistor divider from the supply voltage. The lower of the two error amplifier outputs is multiplied with the VIN_SENSE pin voltage. If the LT3798 is configured with a fast control loop, slower changes from the VIN_SENSE pin would not interfere with the current limit or the output current. The COMP+ pin would adjust to the changes of the VIN_SENSE. The only way for the multiplier to function is to set the control loop to be an order of magnitude slower than the fundamental frequency of the VIN_SENSE signal. Operating offline, the fundamental frequency of the supply voltage is 120Hz so the control loop unity gain frequency needs to be set less than approximately 12Hz. Without a large amount of energy storage on the secondary side, the output current will be affected by the supply voltage changes, but the DC component of the output current will be accurate. An internal multiplier enables the LT3798 to achieve high power factor and low harmonic content by making the peak current of the main power switch proportional to the line voltage. A LT3798 design enables a power factor greater than 0.97 for most applications and will comply with most Harmonic Emission requirements.

Transformer Design Considerations

The transformer specification and design is a critical part of successfully applying the LT3798. In addition to the usual list of caveats dealing with high frequency isolated power supply transformer design such as low leakage inductance the following information should be carefully considered. Since the current on the secondary side of the transformer is inferred by the current sampled on the primary, the transformer turns ratio must be tightly controlled to ensure a consistent output current. A tolerance of ±5% in turns ratio from transformer to transformer could result in a variation of more than ±5% in output regulation. Fortunately, most magnetic component manufacturers are capable of guaranteeing a turn's ratio tolerance of 1% or better. Linear Technology has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the LT3798 and this list of transformers are shown in the LT3798 data sheet.

Conclusion

The significance of power factor lies in the fact that utility companies supply customers with volt-amperes, but bill them for watts. Power factors below 1.0 require these companies to generate more than the minimum volt-amperes necessary to supply the real power (watts) which increases generation and transmission costs that are passed on to the consumer.

The LT3798 is a unique revolutionary new part for its ability to provide off-line isolated power conversion with active PFC in single stage flyback converter and is done without the need for an optocoupler to sense the output voltage. This combination significantly simplifies the design, reduces the line voltage harmonic distortion and solution size, improves the power factor and reduces the cost of the converter that can be used for a wide variety of off-line and high DC-input applications.

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Power Products
Linear Technology Corporation

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UNDERSTANDING COMMON-MODE NOISE IN LOW-POWER OFFLINE SUPPLIES

Offline supplies for mobile phones need to be simple, low cost, and highly efficient power converters

By: Vladimir Alexiev

Yet the ruggedness of the underlying technology makes the core designs attractive to a much wider audience, such as industrial users who need low-power supplies for DIN-rail and similar equipment. But while industrial applications stress long-term reliability over cost and have few constraints on form factor, minimal cost and size are essential in the consumer space. EMI suppression then becomes very difficult, with no Earth connection or X/Y capacitors, few input-filter components, and arbitrary power-cable lengths.

Methods exist to mitigate these issues, but rarely in isolation from other contributors. For instance, twisting the power cable's conductors theoretically makes length less critical. But as any EMC test engineer knows, cable length and layout heavily influence results. At another level, a modified topology such as the resonant discontinuous forward converter (e.g. CamSemi C2470 controller family) that softens primary-side switching eases meeting regulatory requirements with minimal EMI-filter hardware. Applicable standards include EN 55022 for conducted and radiated emissions, and ETSI EN 301 489-34 for conditions that apply to mobile phone chargers as defined by IEC 62684.

Yet the touchscreens in today's smartphones are highly susceptible to noise that can be present at a supply's output. Typically, this becomes apparent when using the phone during a charging cycle. Connections to ac-line create a competing noise current path that may swamp the user's connection to Earth, which the touchscreen relies upon for sensing user inputs. Due to consumer requests for a common charger that suits all data-enabled mobile phones, the 'MoU initiative' targets interoperability issues and the environmental impact that results from disposing of countless special-to-type chargers. Because common-mode noise affects different touchscreens to varying extents, resolving this issue is crucial for interoperability.

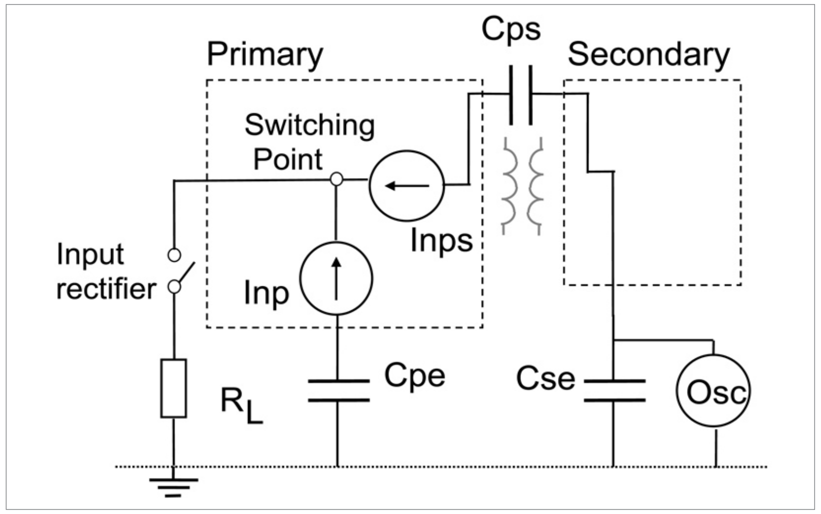

Figure 1. A flyback converter's main common-mode noise sources and transfer paths.

Currently in its first edition, IEC 62684 is the MoU initiative's standard for ensuring interoperability between phone-charger power supplies. It specifies criteria such as universal-input ac-line operation, USB Micro-B cabling, compatibility with the USB-IF standard for device-detection and protection, environmental operating conditions, and the charger's dc output characteristics. This last section states that the output voltage shall be 5.00±0.25 VDC from no load to a full output current level that must lie between 500 and 1,500 mA. It also lays the foundation for common-mode noise limits and demands some specific tests.

Mechanisms that create common-mode noise

The flyback topology dominates low-power ac/dc conversion as it is simple, efficient, and inexpensive. We will consider two periods within any switching cycle - the 'charge' period during which energy builds in the transformer's core, and the 'discharge' period while this energy releases into the secondary circuit.

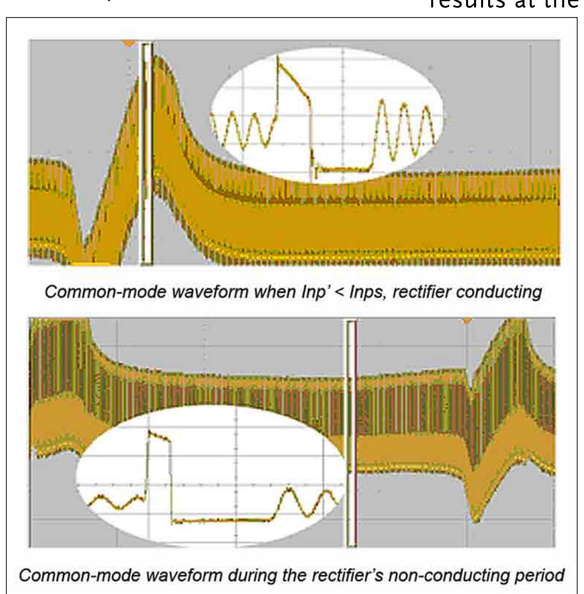

Figure 2.
Top trace— common-mode waveform when Inp < Inps
Bottom trace—the waveform during the rectifier's non-conducting period

The common-mode noise waveform at the dc output differs substantially during the Bridge Conduction Time (BCT period) when the input rectifier is conducting from the remainder of the ac-line cycle, when it is non-conducting (Bridge Non Conduction Time, BNT). With the switch on the left-hand side of figure 1 representing the input rectifier, we see the two circuits that operate during these periods:

During the BCT period, the switch connects the transformer's primary to ground, causing a common-mode noise current Inps to flow between the secondary and primary to become the dominant noise term. The common-mode signal that results at the charger's output is proportional to the difference between Inps and Inp, which is the noise current that transfers from primary to Earth. There are two possible conditions:

1. Inp > Inps—the resulting waveform is the same shape as the switching signal
2. Inp < Inps—the waveform is proportional to the inverted switching signal—see the top trace in figure 2.

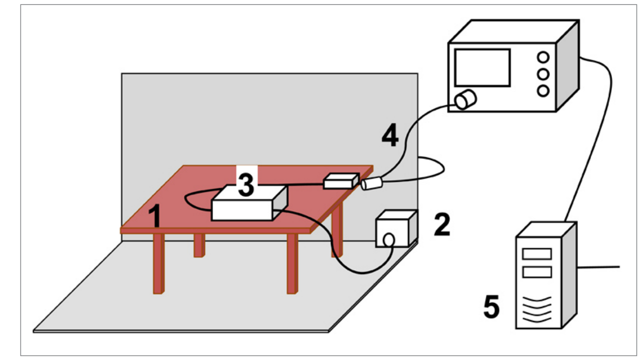

Figure 3. Common-mode noise measurement set-up:

1. *Non-conductive table*
2. *LISN and EPS supply cable*
3. *EPS, output cable, and mobile terminal*
4. *8 pF/10 MΩ probe to the oscilloscope*
5. *Computer*

As the bottom trace in figure 2 shows, the waveform during the BNT interval will always be the inverted switching signal, as the main noise source is the primary pushing current to Earth through capacitor Cpe.

The main switching components differ between the BCT and BNT periods together with the high-frequency signal content. Because the largest peak-to-peak voltage Vpp can appear anywhere in the ac-line cycle, quantifying Vpp demands identifying the worst-case levels in multiple frequency bands. The key to optimizing conducted emissions lies with precisely balancing the two conditions during the BCT period.

Test configuration set-up

Common-mode noise measurement accuracy depends on test method and setup. To test the external power supply (EPS), we use the set-up that EN 55022 defines together with these modifications from IEC 62684:

- 30 cm distance from the EPS cables, loads, and mobile terminal to Earth
- 10.00 ± 0.01 Ω load
- EPS powered by 253 VAC -1% / +0% at 50 Hz ± 1%
- 1 m cable from EPS to the load.

The LISN (line-impedance stabilization network) decouples the EPS supply from other ac-line connected equipment. It balances line and neutral, provides a suitable point for measuring high-frequency signals, and makes the Earth connection that IEC 62684 stipulates.

Measurement method

An objective within IEC 62684 is to measure the worst-case Vpp signal amplitude over a 20 msec ac-line cycle at 253 VAC, as common-mode noise tends to worsen at high input voltages. CamSemi's approach exploits a digital oscilloscope to acquire the line-frequency signal frame in four million samples. This data passes through digital filters and frame-scan measurements to find the worst Vpp signal in each frequency band.

> Recently, the MoU initiative published a "Guide on Implementation of Requirements of the Common EPS" to support IEC 62684: The Guide exempts many of the common-mode noise tests in IEC 62684, recommending instead measurement of all pulses longer than 250 nsec. This effectively results in a single frequency band from below the switching frequency to 4 MHz.

Test results and possible compensation strategies

Examining the common-mode noise shapes and amplitudes after filtering can help identify interference sources and suggest approaches to mitigating the problem. A two-stage approach minimizes noise at source before applying a signal of opposite phase and amplitude

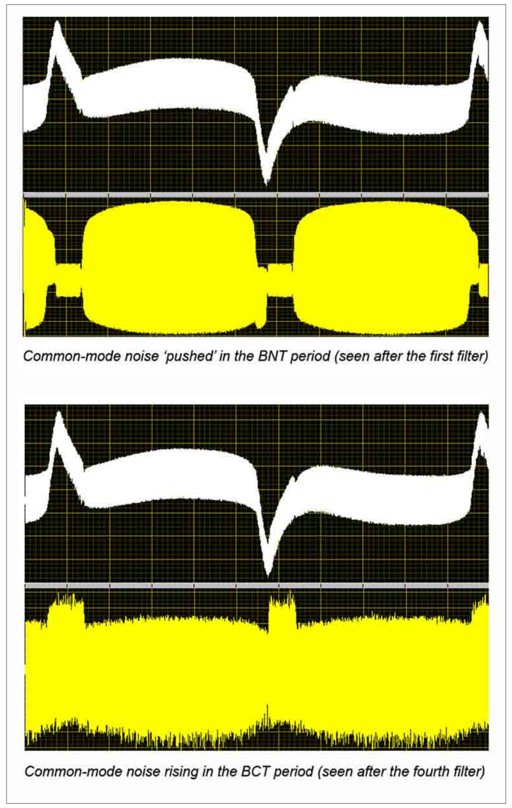

Figure 4.
Top traces— common-mode noise pushed in the BNT period (after 1st filter)
Bottom—common-mode noise rising in the BCT period (after 4th filter)

to the remaining noise signal. A range of suitable mechanisms for achieving this are discussed in CamSemi US patent 8,023,294 www.google.com.tr/patents/US8023294.

Compensation methods include balancing the transformer's design to "push" noise between BCT and BNT periods. The top traces in figure 4 show the result of pushing the common-mode noise signal during the BNT period.

All compensation methods suffer from signal inaccuracies that worsen as frequency increases. The relationship between the signals in the high-frequency area can be completely different from the main switching frequency band, and the extent of the difference within this relationship is one measure of the quality of the compensation. The bottom traces in figure 4 show the 1 to 100 kHz and 1 to 100 MHz frequency bands for the same signal, revealing the onset of increasing common-mode noise during the BCT period due to signal delays and inequalities in compensation.

Conclusion

While it may not necessarily optimize conducted emissions - adjusting the compensation to drive the signal amplitudes during the BCT and BNT periods to being as close to equality as possible is the best method for minimizing common-mode noise.

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ENERGY BOOST CONVERSION

Small, battery-powered medical analysis equipment presents a challenge to the power circuit designer.

By: Andy Fewster

In meeting this challenge an understanding of the way boost conversion is implemented in today's power ICs will be extremely helpful. Medical devices can gain marketing benefits from the promise of long battery life.

But this article is aimed at clarifying the designer's choice by illustrating the particular characteristics of two different approaches to boost conversion in low-load applications such as personal medical equipment: a hysteretic converter, and a Pulse Width Modulated (PWM) converter; their two different sets of characteristics are well suited to two different kinds of load profile. Designers can streamline the component specification process by matching the load profile of their application to the right converter type.

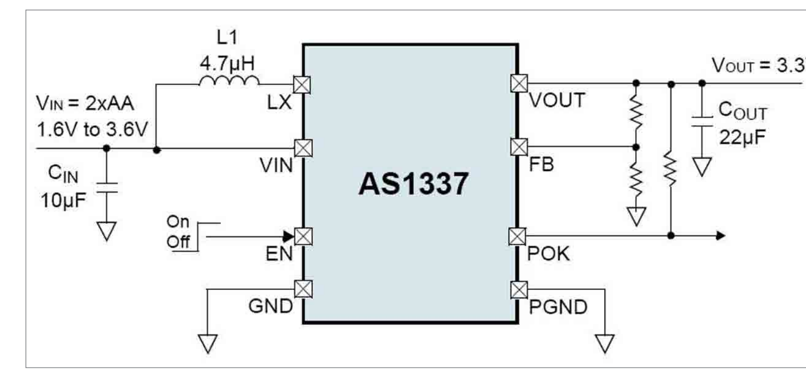

Figure 1: Typical application circuit, using 2 AA batteries and a regulator IC, the AS1337, to produce a 3.3V output

The operating environment for the converter circuit

Battery power in the types of medical devices in question usually comes from one of:

- Lithium coin cells (2-3V per cell)
- Alkaline primary cells (0.9-1.5V per cell) in AA or AAA outlines
- Lithium primary cells (0.9-1.7V per cell) in AA or AAA outlines
- NiMH rechargeable cells (0.9-1.25V per cell) in AA and AAA outlines

Single and dual series connections are common with AAA and AA batteries. In this article, it is assumed that the power management circuit must provide at least 3.3V from a single or dual alkaline cell (see Figure 1), and that long battery life and low bill-of-materials cost are equally important objectives for the design.

Important additional features

The basic requirement of the converter IC is to boost the voltage accurately and efficiently to the required level. But other capabilities can also enhance the operation of the power circuit.

- Output supervisor: the output supervisor can produce an output reset pulse for the device's controller (normally an MCU) after a time period measured from the point at which the output voltage approaches the desired output value.

- Input supervisor: usually an uncommitted comparator input used to monitor the battery voltage. Useful for providing a 'low battery' warning just before the battery is fully exhausted. Sometimes this is a shared function with an output 'power OK' flag.
- Quasi step-down mode: this is useful when the terminal voltage of a fresh battery is slightly higher than the output regulated voltage. It allows the battery voltage to decay until boost-only operation commences. Quasi-step down mode, either switched or 100% duty cycle, entails some loss of efficiency. But it is convenient, because it eliminates the requirement for a more complex buck-boost converter arrangement – and the period in which Vin is greater than Vout is normally short.

Efficiency and long battery life

Achieving long battery life depends on a number of factors, but two dominate:

1. Conversion efficiency
2. Load characteristics, such as duty cycle and peak current.

A meticulous approach to power management, powering down components such as the display and the controller whenever they do not need to be active, will have a marked effect on battery life.

The load characteristics will also affect the designer's approach to optimising conversion efficiency. There is no such thing as a perfect boost converter, and each type has its strengths and weaknesses. Of particular importance are:

- The value of the average load – some converter types supply light loads more efficiently, while others are better suited to heavy loads
- The duty cycle – again, some converter types are better suited than others to applications that have long periods of no activity followed by short bursts of active operation.

To define the load characteristic, the designer should measure the load current over time (assuming a constant supply voltage) under a variety of conditions, including different usage modes and different temperatures. The magnitude-versus-time envelope can then be converted to an RMS (root mean squared) value, from which the time-averaged power dissipation is calculated.

Common load current profiles are shown in Figures 2 and 3, calculating the RMS power dissipation. T is the overall time between repetitive current profiles, and D is the duty cycle.

The shorter the duty cycle, the lower will be the RMS current of the load. For these applications, the designer must take into account not only the typical load profile, but the periods of non-activity: here, the contribution of the converter IC to quiescent current becomes crucial. Of two conversion techniques implemented in the latest boost converters from austriamicrosystems, one – hysteretic, implemented in the AS1310 – has a far lower quiescent current than the other, Pulse Width Modulated (PWM) technique implemented in the AS1337.

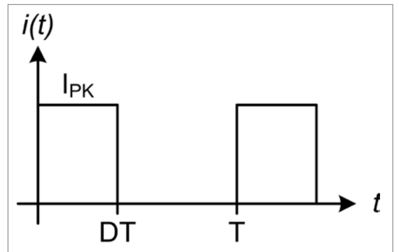

Figure 2: Fixed current demand over time

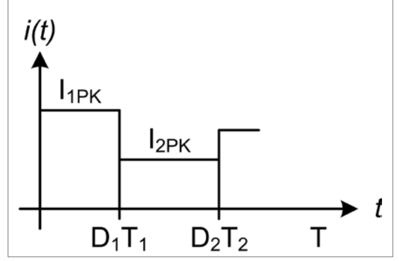

Figure 3: Variable current demand over time

Hysteretic control, also known as ripple control, achieves a lower quiescent current because it eliminates the other converter type's clock-based PWM core, employing a simple comparator instead. In Shutdown mode, the AS1310 draws less than 100nA. Other advantages of this operating scheme include low operating current, simplicity – since there is no need for the PWM scheme's closed-loop frequency compensation – and fast transient response. The AS1310 is optimised for light loads (60mA), at which it achieves efficiency of up to 92%.

On the other hand, the designer must be prepared to accept the hysteretic technique's downsides: load-dependent variable operating frequency, and output ripple. In fact, output ripple is fundamental to the operation of the hysteretic converter, and is broadly equal to the hysteresis value set by the comparator. In addition, discontinuous current operation in the inductor produces higher peak input currents than the equivalent fixed-frequency current-mode PWM converter operating with a continuous inductor current.

The alternative current-mode PWM control scheme, as implemented for instance in the latest AS1337 IC, provides exceptional line and load regulation. The continuous inductor current reduces peak input currents compared to a hysteretic control scheme. PWM conversion also offers higher efficiency at moderate and heavy loads than a hysteretic scheme.

In the case of the AS1337, an automatic power-save mode, initiated if the output load current falls below a factory-programmed threshold, also improves efficiency at light loads, by removing power from all circuitry not required to monitor the output voltage, and operating in an intermittent PWM mode.

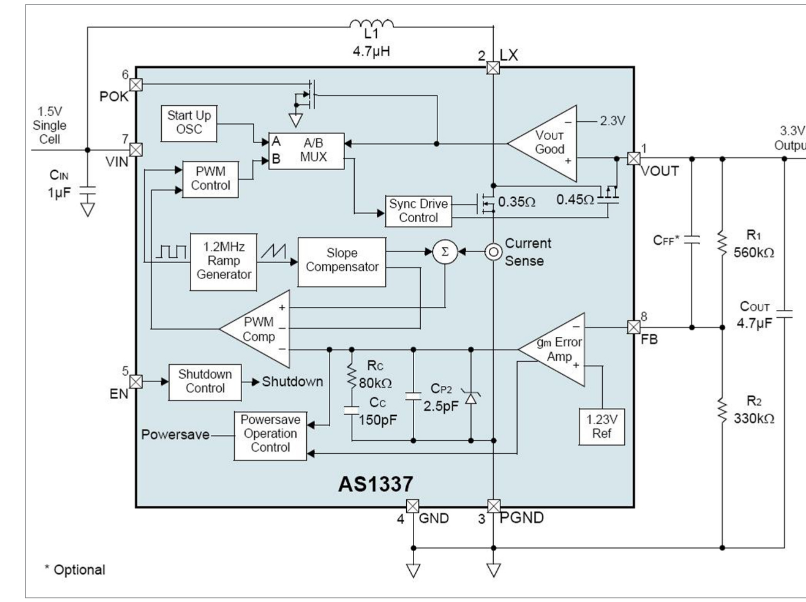

Figure 4: Block diagram of AS1337 PWM boost converter IC

Additional design guidelines for efficient conversion

Conversion efficiency depends in part on constraining resistive losses in the main storage inductor, at least to a value below the resistive losses of the integrated power switch and must be able to handle the peak current of the dc-dc converter without saturating – and in a hysteretic mode converter this peak current will be higher than in the equivalent PWM converter. High-frequency ferrite core inductor materials produce lower frequency-dependent power losses than cheaper powdered iron types, and this results in improved converter efficiency.

Another factor is the equivalent series resistance of both the input and output capacitors (see Figure 4): this should be minimised in order to reduce ripple at the output, and to reduce peak current and conducted noise at the input.

Conclusion

The load demand data will inform the choice of converter IC. Advanced new converter ICs from austriamicrosystems implement hysteretic and PWM voltage regulation schemes: understanding the different characteristics of these two schemes will help the designer ensure the chosen converter type best suits the power demands of the application.

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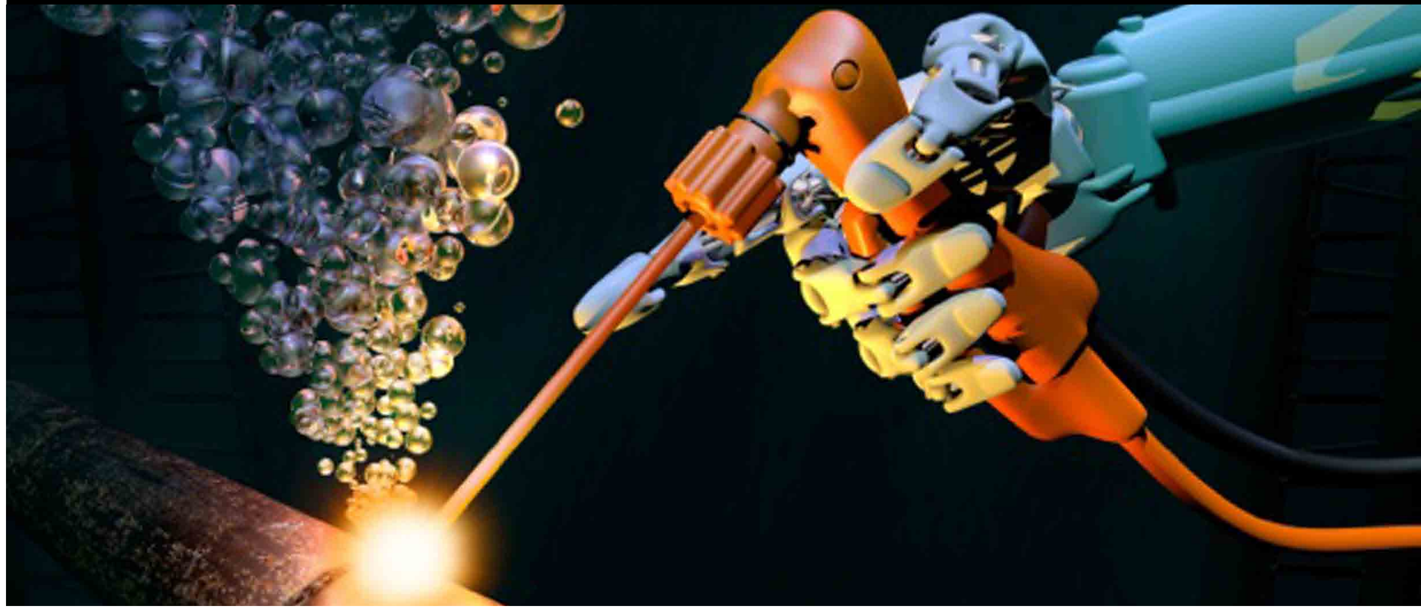
Special Report:
Motor Drive, Robotics & Control

PSD EUROPE

Power Systems Design: Empowering Global Innovation



Inside:

INDUSTRIAL CONTROL

Do you really need that CPU in your microcontroller?

By: Mark Ainsworth

In most microcontroller architectures, there is a 'smart' CPU surrounded by a set of relatively 'dumb' peripherals.

Peripherals have limited functions; converting data from one form to another. For example, an I2C peripheral basically converts data between serial and parallel formats while an ADC converts signals between analog and digital. The CPU has to perform all the work to process the data and actually do something useful with it. This, plus close management of the peripherals, can result in great complexity in the CPU's firmware and may require a fast and powerful CPU to execute that firmware within real-time timing constraints causing more obscure bugs, more complex and expensive debugging equipment.

If the peripherals were complex enough, flexible enough, and ultimately "smart" enough to effectively relieve the CPU of many of its tasks, a complex design could then be restructured as a group of simple designs distributed among the CPU and the peripherals, giving the CPU fewer tasks and fewer interrupts to handle, making bugs easier to find and fix. The overall design would become more robust, and portions of the design more easily reused. A CPU with less to do may be run at a slower speed to save power, or that available bandwidth could be used for additional tasks. However, the peripherals would still need to be designed in a cost-effective manner or the overall microcontroller might become too expensive.

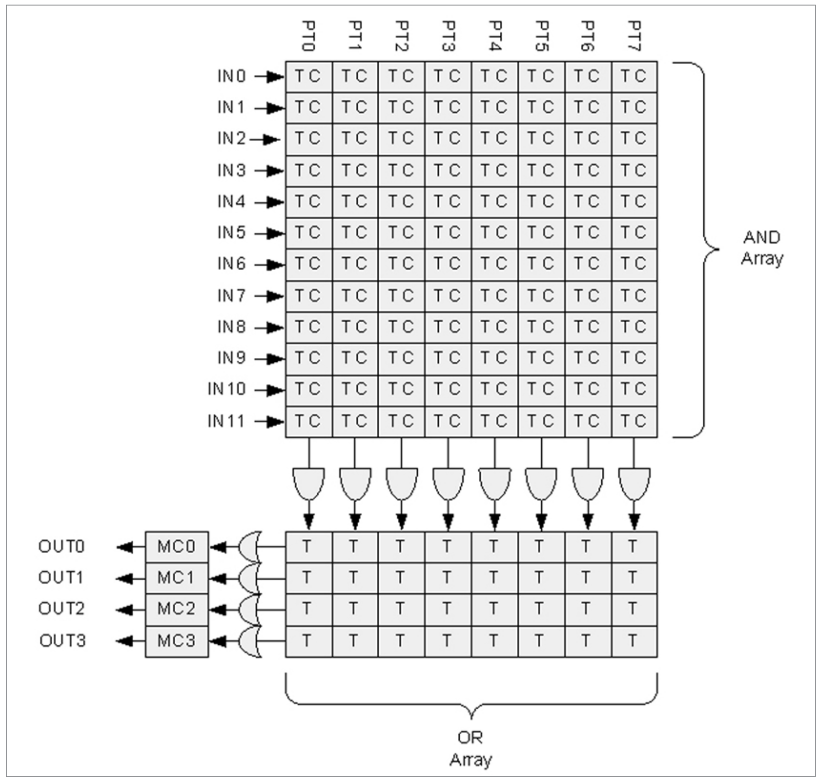


Figure 1: Example PLD, with 12 inputs, 8 product terms and 4 macrocells PLDs can have hundreds of macrocells with up to 16 product terms driving each macrocell. The AND and OR gates within the product terms can be interconnected to form highly flexible custom logic functions. The macrocells are typically clocked, and their outputs can be fed back into the product term array. This allows state machines to be created.

There are two general ways to construct a smart configurable peripheral. The first is to use a Programmable Logic Device (PLD). As shown in Figure 1, a PLD has a sum-of-products logic gate array driving a number of macrocells. The "T" and "C" notations indicate that each product term can generate either a true or complement (inverted) output, so that both positive and negative logic can be supported.

Large-scale PLDs can be used to form complex logic functions. However, a lot of gates may be needed to implement even simple logic functions and it can become expensive to scale up a PLD-based solution for more complex functions. At some point, it makes more sense to just use an actual CPU.

A very simple form of such a CPU is a datapath based on an arithmetic logic unit (ALU), also known as a "nano-processor". A datapath implements just a few common functions but does so more efficiently than an implementation using PLDs. Figure 2 shows a simple datapath with an ALU. A typical ALU can do a variety of operations, usually on 8-bit operands: count up (increment), count down (decrement), add, subtract, logical AND, logical OR, logical XOR, shift left, and shift right. There are two 8-bit accumulators that can act as either input data registers or storage for ALU output. A single operation takes place on the edge of an input clock signal. A function select register is used to control what operation takes place, the source register(s) for that operation and the destination register for the output. Depending on the specific design of the datapath, it is possible to do a series of complex operations.

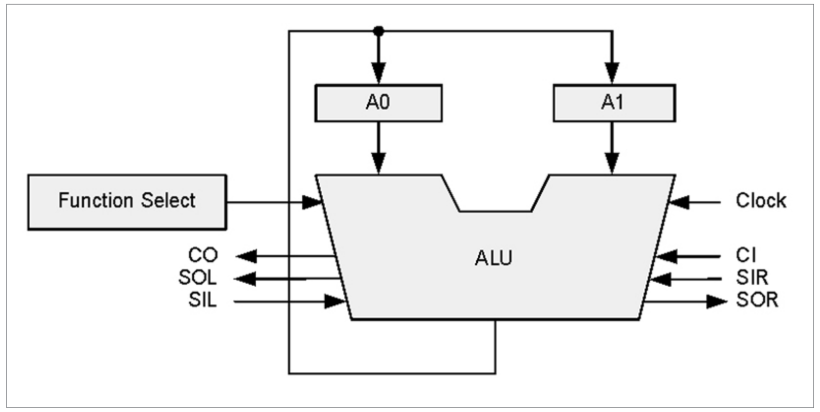


Figure 2: A simple example of an ALU-based datapath, with accumulators, function select, clock, and carry and shift chaining signals

A function select block can actually be a small SRAM, preloaded with the desired function select bits, and the SRAM's address lines can be used to select which operation is to be done. Finally, multiple datapaths can be chained together with carry and shift signals so that operations can be done on multi-byte operands.

Since a datapath does only a few specific functions, it is possible to optimize its design so that it is inexpensive to build. However, a datapath is not nearly as flexible as a PLD for implementing complex logic. Separately neither one works well but together they can work very well.

Although UDBs have a lot of features in common with both the PLDs and datapath, signals can be routed among the PLDs and datapaths throughout the entire set of UDBs. Elsewhere in the device, to form a complex fabric called the Digital System Interconnect (DSI). There are similar routing features for analog signals, as well as interfaces between the analog and digital domains and the device pins.

In a basic example, we can use one UDB datapath to create an 8-bit counter with reload

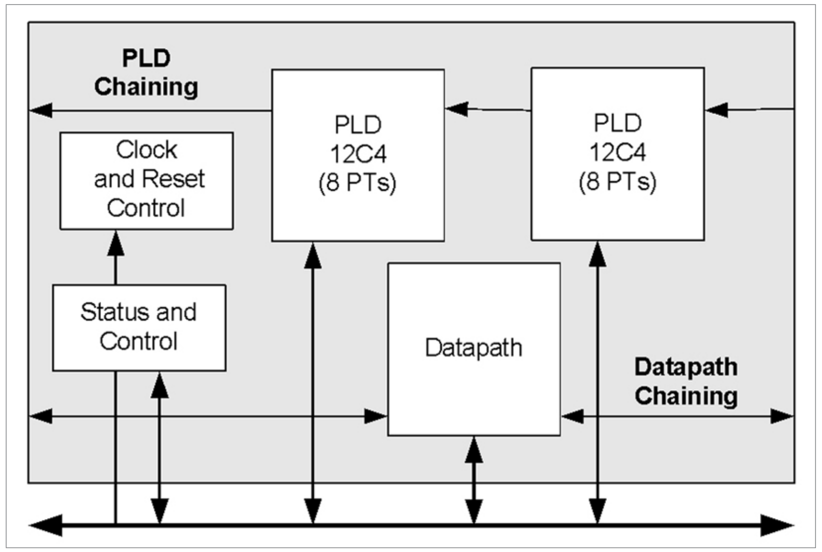


Figure 3: UDB Datapath Configured as a Counter with Reload

capability. To do this we connect one status condition back to a control store SRAM address line (Figure 3)

In this design, A0 is the counter register and D0 is the reload register. We need two functions, one to decrement the counter and one to reload the counter from the period register; these functions are preloaded in the Control Store RAM.

The logic is as follows. When A0 is not zero, the condition output will be low and the decrement operation at address 0 will be executed. When A0 is zero, the condition output will be high and the reload operation at address 1 will be executed.

All operations take place on the rising edge of the clock input, allowing the number of clock edges to be counted. The clock input can be routed from a variety of sources. The condition output can be routed throughout the DSI, including to DMA and interrupt request inputs. Using datapath chaining and a mask block, the size of this counter can be any number of bits, and is not limited to a multiple of eight bits.

This simple design can be expanded, with the use of PLDs, to create a more complex application. Consider a traffic light controller. A traffic light controller cycles through three states, green, yellow and red, so a state machine is required. Each state lasts for a certain amount of time before changing to the next state, so a counter is also required. For simplicity, assume that the "green" time is the same as the "red" time but that the "yellow" time is different.

The operations to be saved in the Control Store RAM are:

A0 = A0 – 1 // count
A0 = D0 // reload "green" or "red" count value
A0 = D1 // reload "yellow" value

The state machine is implemented in the PLD. The datapath condition output is fed back to the PLD to indicate that it's time to change state. The PLD also has logic that based on the current state and the signal fed back from the datapath, controls which datapath operation to perform and which traffic light to activate.

Smart, flexible, low-cost peripherals can be created using an efficient combination of PLDs and datapaths. If so much functionality can be offloaded to peripherals then in many cases, there is not much for the CPU to do. A more realistic solution is to use the CPU in the traffic light example to (a) detect when a vehicle goes through a red light, (b) use the camera to photograph the license plate, (c) extract the text from the photo, (d) look up the owner in the state database, and (e) send a ticket to the owner.

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SETTING NEW EFFICIENCY BENCHMARKS FOR NEXT GENERATION MOTOR CONTROL APPLICATIONS

Electric Motors Are Continuing to Evolve, As Market Requirements Grow.

By: Matthew Tyler, Product Line Manager, ON Semiconductor, & Mats Sandvik, Applications Engineer, Stegia

Electric motors are continuing to evolve, as market requirements grow for more compact, higher performance solutions which exhibit greater resilience to the often harsh environmental settings in which they find themselves. Though modern bi-polar stepper motors are capable of delivering both improved reliability and better accuracy than conventional motor offerings, OEMs and systems integrators still need to ensure they use all the tools and techniques available to them to maximize the effectiveness of these electro-mechanical devices. The following article discusses the merits of mapping system performance and how the employment of advanced adaptive control algorithms can raise efficiency levels and subsequently boost performance metrics.

The use of adaptive control algorithms enables the full efficiency of the motor system to be gauged, taking into account the adverse conditions that the specific application may inflict upon it. This allows a much more comprehensive assessment of the system's ability to cope with its surroundings (whether these are industrial, automotive, or some other scenarios with exacting demands) and greater assurance of how well it will perform than would be possible by simply consulting the datasheets for the various constituent components it is made up of.

In order to gain maximum

efficiency, it is necessary for the boundary conditions of the complete motor system to be mapped. System variables such as motor speed, motor acceleration/deceleration, system temperature, mechanical degradation and supply voltage all need to be taken into consideration. The system architecture utilized will also have an effect on whether stipulated performance goals are reached. The possibility of resonance occurring is endemic to stepper motor systems. It can result from the motor running too close to its natural frequency. Ensuring that resonance does not take place is vital, otherwise the motor could lose steps or even stall.

Motor Control Systems

There are two basic types of motor control systems. These are:

1. Open Loop Systems – Here it will typically be necessary to stimulate the motor with the worst case current drive and velocity profile, as a result efficiency is not really a design goal. Mapping can be a long drawn out process, because the system has to be verified for all possible variables at which it will operate (to avoid possible risk of resonance) - supply voltages, temperatures, velocities, etc. Furthermore, pinpointing conditions where the stalling of the motor could arise can prove very difficult in an open loop system.
2. Closed loop systems – These consist of either a sensor-based arrangements, that use optical or magnetic sensing mechanisms, or sensor-less arrangements, which tend to detect the voltage generated by the motor windings moving through the motor's magnetic field. For sensor-based systems variation in the characteristics of the sensor must be considered when performance mapping is being undertaken. For sensor-less systems the data acquired is relative to the motor's physical motion. This simplifies system complexity and cost (as no external sensors are called for), although it does require a more in-depth knowledge of electro-mechanical theory.

In sensor-less systems, through use of back electromotive force (EMF) it is possible to acquire detailed diagnostic data on the motor system. Between motor drive current pulses, the motor windings inherently produce a voltage as they move through the motor's magnetic field.

ON Semiconductor's AMIS-30522 micro-stepping controller IC (as shown in Figures 1 and 2) is designed specifically for use with bi-polar stepper motors serving the automotive, industrial, medical and marine sectors. As it provides a speed and load angle (SLA) output, stall detection algorithms can be created. The mapping of the SLA pin of an AMIS-30522 which has been incorporated into a Stegia stepper motor is described in Figure 3. The data used to compile this was collected during a frequency sweep of the NXT

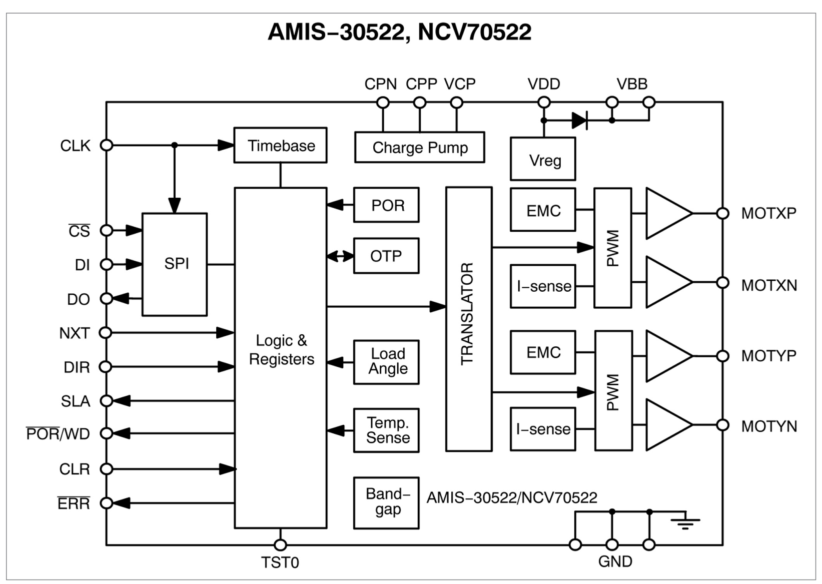

Figure 1: AMIS-30522 Functional Block Diagram

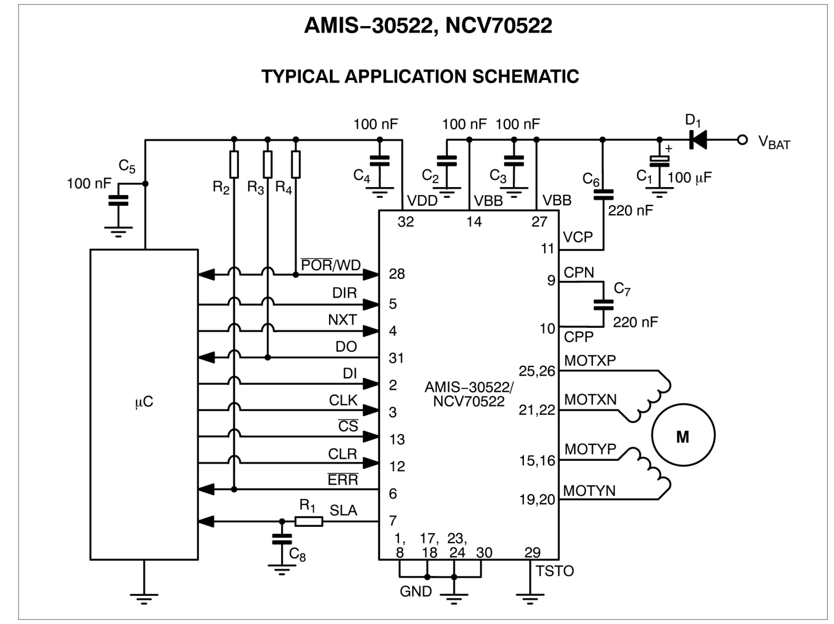

Figure 2: AMIS-30522 in Stepper Motor Control Application

clock input. The frequency of the motor stimulus increases as it moves from left to right and the various regions of operation can be analyzed in detail.

The capacity of the AMIS-30522 (and the other devices in this series) to measure the motor characteristics of a complete system gives OEM design teams much greater visibility. Rather than just being able to locate where motor resonance might occur, they can obtain knowledge of the complete mechanical system - how its performance changes with relation to the alteration of the many different variables involved and where the regions that may lead to operational issues lie.

The motor system can continuously sample the voltage produced by the motor windings via the SLA pin and can rapidly respond should there be any issue that could have an unwanted effect on system performance. As back EMF has a direct relation to the rotors speed it can be employed to measure the external load on the output shaft and regulate the current being supplied to the motor. In addition, creation of an algorithm which is able to rapidly detect entry into a resonance region means the system can accelerate the motor out of this region until it is returned to a speed which is safe.

The red area found on the left of Figure 3 highlights a resonance in the system. This could be due to a number of different factors, such as the physical mounting of the motor, or the motor's fundamental resonant frequency between steps. These are usually regions of commutation speed to be avoided and can be easily mapped through the back EMF approach. This can reduce the strain placed on the motor system and lower concerns about reliability.

Figure 3: NXT pin frequency sweep while monitoring the SLA pin

The red area on the right of Figure 3 highlights where the current drive is above the system's RLC time constant, leading to residual current flow within the motor windings. This gives the maximum speed limit that is recommended for the motor system.

The recommended operating region for the motor is found between the two red areas. In addition, this mapping technique can be used to spot a stalled condition in which the motor does not commutate and, therefore, no back EMF is generated. Such conditions can easily be dealt with by the system controller through configuration of a minimum threshold during motor stimulus.

Applying Mapping Data to Improving System Design

After the mapping process has been completed and the optimal velocity profile has been identified, the SLA value that offers the best overall performance metrics can be chosen – this denotes the system's most efficient operating point. The variables listed earlier (such as motor acceleration, motor speed, etc) can be dynamically adjusted to ensure that issues that could impinge on system efficiency (like resonance) can be avoided.

As motor systems continue to require ever higher precision and greater reliability, the need for diagnostic feedback is certain to grow. This means that highly integrated, feature-rich semiconductor solutions will be needed for supporting stepper motor devices. As sensor-less control loop systems can deliver feedback that is not of a binary nature, they can be used to draw detailed diagnostic information about the motor without additional system complexity needing to be added. This means that subtle changes in SLA output can be utilized for real-time compensation before step loss or stall situations are arrived at.

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EASY TO USE DIGITAL PFC

Supplements motor control applications

By: Frederik Dostal

Many AC powered systems above a certain power consumption level require power factor correction (PFC).

This is demanded by either utility companies or by governments. PFC sits right at the input of a system behind a diode bridge rectifier but before any input capacitors. The PFC circuitry is intended to make sure that the voltage and current on the input are in phase with each other. In other words, PFC is the ratio of average power delivered to the circuit load to apparent power.

This article introduces an easy way to design very flexible and feature rich PFC circuits with Analog Devices ADP1047 and ADP1048 digital PFC controllers with monitoring. This design work is done by using an intuitive graphical user interface. Also the benefits of such an approach in combination with a motor drive application are reviewed.

Different PFC circuits

PFC circuits typically use a boost DC to DC converter topology right behind the AC rectifier bridge. This topology forces the input current to be in phase with the input voltage. The result is that the load looks like a pure passive load resistor to the AC source. For higher power levels, an interleaved topology can be used. The most common is a two channel interleaved operation. This is nothing different than having two boost converters in parallel and making them share the load. Similar approaches outside of PFC are called multi phase. Step-down (buck)

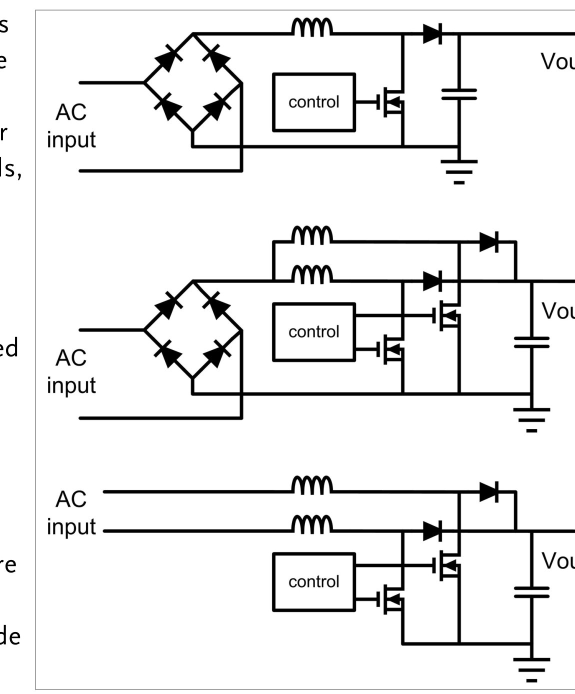

Figure 1: Different PFC circuits

type regulators would use the term 'multi phase' if current is distributed amongst different parallel step down circuits and the outputs are combined. In PFC the term 'phase' is not used for this function, since it can create a lot of confusion. 'Multi phase' is used for PFC circuits for more than one phase of AC supplies coming in. This is why the term 'interleaved' is more common to describe the distribution of the load power on multiple parallel boost topologies.

For very high power efficiency one can also go bridgeless. In this case the diode bridge rectifier can be omitted. In the interleaved operation with a diode bridge rectifier, the two channels are alternating after each switching period. In the bridgeless topology however, one channel switches during the positive half wave of the AC input voltage and the second channel switches during the negative half wave. Figure 1 shows a principle circuit diagram of these three basic circuits. The top shows the easiest implementation, the middle the interleaved concept and the bottom the bridgeless configuration. Of course many more circuits are possible. For high power and very efficient operation one can combine interleaved operation with a bridgeless setup for example. Obviously such designs require many components and can become quite complex. The ADP1047 is intended for single channel PFC while the ADP1048 offers the capability for interleaved and bridgeless operation. For this purpose it offers a current sharing function as well as two different PWM output signals.

Flexibility of using a digital PFC controller

Most PFC converters are analog type systems. With today's digital derivates however such as Analog Devices ADP1047 and ADP1048, a designer can take advantage of the great flexibility digital can offer. The loop stability can be optimized for high speed and sufficient stability using a programmed digital filter rather than hardware components. While these devices implement the average current mode control loop, there are actually different loops which can independently be programmed. There is a low and high line current filter as well as fast voltage compensation filters.

The output voltage of the PFC can be programmed so that it varies based on the load current. This can increase the power conversion efficiency in the overall system. Also soft-start behavior can be modified in great detail.

Monitoring of voltage and current at the input of a system is valuable

Besides the digital control loop, the ADP1047 and ADP1048 offer accurate voltage and current monitoring. The input and output voltages are sensed as well as the input current. These sensed analog values are digitized using analog to digital converters. The inductor current which equals the input current is either measured with a current sense resistor directly for highest accuracy or indirectly using two current transformers in series with the power switch or boost diode. In any type of sense method, the sensing can be calibrated in the system to increase the measurement accuracy. Such calibration is typically done together with production testing and the calibration values are stored in the EEPROM of the ADP1047 and ADP1048. Besides voltage and current it is also possible to calibrate an external temperature sensor.

The measured information about the voltages and current are used for the operation, control and protection but can also be supplied to other circuitry in the system via PMBus for monitoring purposes. Especially the input power of the PFC is very interesting since it gives information about potential faults in the system. Different interrupt like flags can be set which contribute to a safe and reliable operation of the setup. The voltage and current information as well as register settings can be accessed via the integrated PMBus interface.

Graphical user interface avoids the need for programming skills

Since experienced power design engineers typically are not excellent code programmers, the approach of this PFC solution is to reduce the digital aspect of the circuit to an easy to use graphical user interface (GUI). Figure 2 shows a screenshot of the software. All parameters which can be influenced are graphically shown on the different setup and monitoring screens. This way evaluating and programming the ADP1047 and ADP1048 offers additional safety since the internal state machine of the chips reduces the room for user errors compared to programming a general microcontroller or digital signal processor.

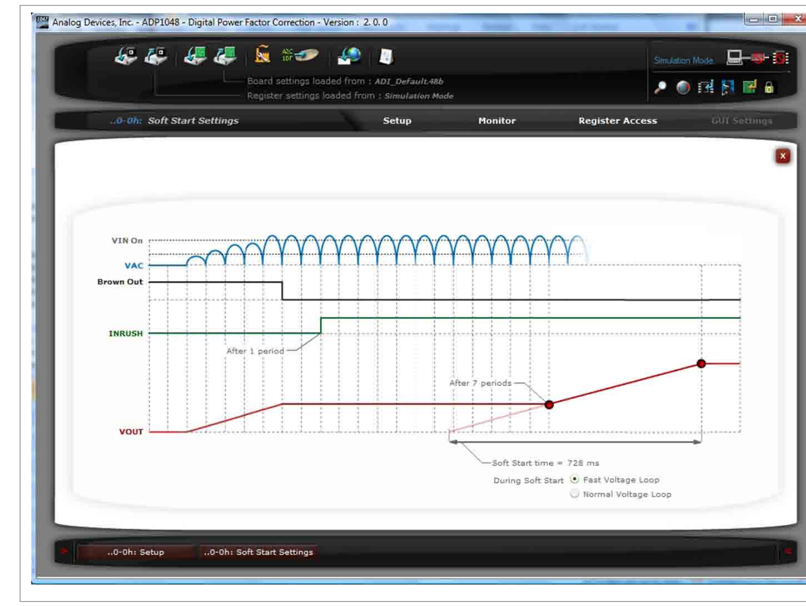

Figure 2: Graphical user interface makes design easy

One example of the GUI's capability is adjusting the soft-start. By the click of a mouse button, the input voltage threshold for start-up can be adjusted. The inrush current time delay setting is set afterwards. Inrush control is used to pre-charge the output capacitor of the PFC circuit before the circuit starts up. This is often implemented via a relay or MOSFETs. Figure 2 shows in the middle of the screenshot how this inrush timing can easily be adjusted. On the bottom diagram in figure 2 one can adjust the behavior of the soft-start function itself. For this, additional delay time before startup as well as the rise time of the output voltage can be adjusted.

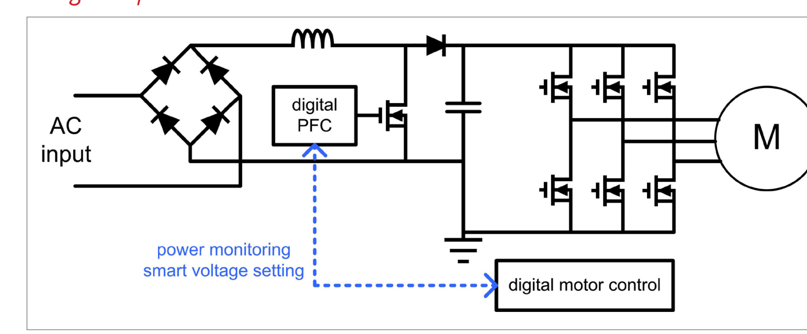

Figure 3: Motor control application

Benefits for motor control applications

In motor control applications, there are two ADP1047 / ADP1048 features which are especially beneficial. One is the precision power monitoring to detect faults in the system, the other feature is the capability to adjust the output voltage of the PFC on the fly. Depending on the state of the motor drive, the voltage can be adjusted to increase efficiency without compromising performance. These 'smart voltage settings' can be used for cases where the motor is paused or in cases where it is running at very low power. Figure 3 shows the principle diagram of the PFC included into a motor control architecture.

PFC easy to use

Implementing a digital PFC solution does not necessarily require a steep learning curve if the right controller IC with the right kind of support software is used. Such an implementation is especially valuable for dynamic applications such as in motor control.

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MCU WITH FPU ALLOWS ADVANCED MOTOR CONTROL SOLUTIONS

By: Dr Yashvant Jani and Graeme Clark

Engineers increasingly are moving their designs to the more efficient three-phase Brushless DC motor (BLDC) and Permanent Magnetic Synchronous motor (PMSM).

Motor control algorithms for efficient motors often employ vector and sensorless vector control involving complex transformations and control loops for speed and position. Industrial applications typically employ sensor-based control because higher accuracy is required, while consumer applications generally use sensorless solutions.

Vector control provides efficient and accurate control of the motor's speed and torque. This is done by decoupling the three-phase stator currents of AC electric motors into a flux component and a torque component. Torque and flux can then be controlled directly (similar to a DC motor) allowing fast dynamic response and excellent steady-state performance. Vector control enables the performance of BLDC motor drives to be comparable or even superior to DC motors.

Sensorless vector control (SVC), which eliminates the speed sensor from the design, makes estimates of the motor's speed and rotor position from the observed stator currents. SVC uses complex coordinate transformations and mathematical models, which require a detailed calculation. Thus SVC, like VC, necessitates a high performance MCU.

Until recently several factors prevented these advanced motor control techniques from wider acceptance:

1. Complicated mathematical modeling,
2. Complicated implementation strategy, and
3. Traditional micro controllers (MCU) and Digital Signal Processors (DSP) implementing vector control use fixed point calculation as they usually do not have a hardware floating point unit (FPU).

An FPU makes vector control implementation simpler and faster as mathematical functions, can be more efficiently carried out using floating-point values. This article provides performance test data comparing an implementation using Renesas's RX600 series MCU with FPU against a fixed-point MCU.

An embedded FPU provides easier development, higher efficiency and uses less power. Several key computations using fixed point and floating point implementation show the FPU provides an advantage for PI and PID control loops, Park and Clarke transforms, ADC measurements converted to current values and encoder data processing.

Four key areas where the FPU can have an impact:

The first is the PID and PI loops for current and speed variables. A PID (proportional–integral–derivative controller) is the most commonly used feedback controller in control systems. A PI Controller (proportional-integral controller) is a special case of the PID controller in which the derivative (D) of the error is not used.

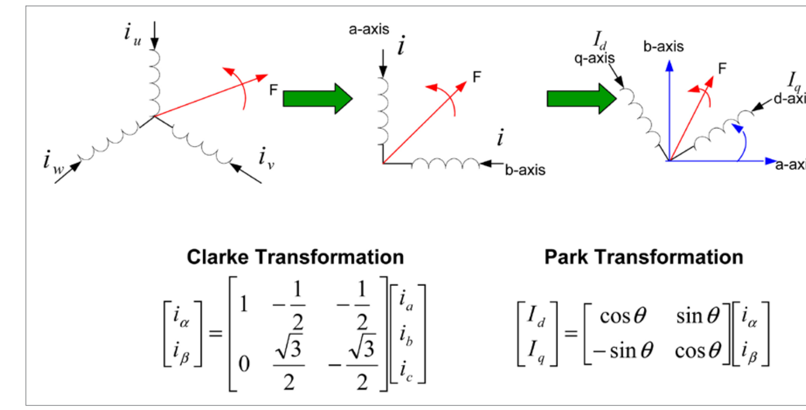
	Fixed-Point Method	FPU Method	Ratio
CPU bandwidth (μsec)	3.5	2.75	0.79
Code size (bytes)	237	134	0.57

Table 1: Test comparison for PI Loops

Measurements performed with the Renesas RX62N for two current controllers and one speed controller implemented as PI loops are shown in Table 1. The FPU-based implementation provides a definite advantage in CPU bandwidth and significant improvement in code size.

The second area is the coordinate transformation known as Clarke and Park transforms. The goal of vector control formulation is to equivalently transfer the three-phase AC motor into DC and then control the AC motor like a DC motor to directly control motor flux and torque.

To transfer three-phase currents into two phase DC currents the first transformation is known as the Clarke transformation shown as αβ→abc In Figure. 1. It converts the three balanced currents in the three-phase stator frame into two phase-balanced currents in an orthogonal stationary frame in the same plane as the stator frame but the angle between the two axes is 90 degrees instead of 120 degrees. The transformation equation is given in Figure. 1.



$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad \begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$

Figure 1: Clarke and Park Transforms Used in Vector Formulation

The second transformation dq→αβ is called a Park transformation and is given by the second equation in Figure. 1. This transfers the stationary frame to the rotor frame to make the AC currents into DC currents. F is the Magneto Motive Force, and θ is the angle between the d-axis and the α-axis, also known as the rotor angle.

We performed measurements for the Clarke and Park transformations combined, and the results are shown in Table 2 demonstrating a significant improvement in CPU bandwidth and code size.

The third area is the angle estimation based on current measurements. These calculations are quite involved and the results are shown in Table 3. Here, CPU

	Fixed-Point Method	FPU Method	Ratio
CPU bandwidth (μsec)	10.7	6.55	0.61
Code size (bytes)	173	89	0.51

Table 2: Test comparison for Clarke and Park Transformations

	Fixed-Point Method	FPU Method	Ratio
CPU bandwidth (μsec)	11	6.8	0.62
Code size (bytes)	119	93	0.78

Table 3: Test comparison for Position Estimation

	Fixed-Point Method	FPU Method	Ratio
CPU bandwidth (μsec)	2.65	1.9	0.72
Code size (bytes)	83	49	0.59

Table 4: Test comparison for Sensor Measurements

bandwidth has improved while the code size has small improvement.

The fourth area is the conversion of ADC measurements into proper current values. Results are shown below in Table 4, showing an improvement for both measurements.

For the overall test we implemented a complete sensorless vector control algorithm in fixed point and FPU format. Using the RSK62N evaluation board, we tested the complete algorithm for CPU bandwidth and code size. Results are shown in Table 5. For CPU bandwidth, an improvement of nearly 35% is achieved, while the code size is reduced 45%. We found that the FPU makes vector

	Fixed-Point Method	FPU Method	Ratio
CPU bandwidth (µsec)	40	26	0.65
Code size (bytes)	13816	7597	0.55

Table 5: Test comparison for Overall Algorithm

control transformation, and the position and speed estimation easier and more accurate. The RX62N has a very simple FPU with only 8 instructions, and yet its makes a significant performance impact.

Renesas FPU-enabled MCUs
The Renesas RX600 CPU architecture is a Complex Instruction Set Computing (CISC) architecture (Figure 2) with 16 general-purpose 32-bit registers and 9 control registers to handle fast interrupts. The architecture has on-chip debug, DSP instructions (48-bit and 80-bit MAC, barrel shifter) and a hardware divider.

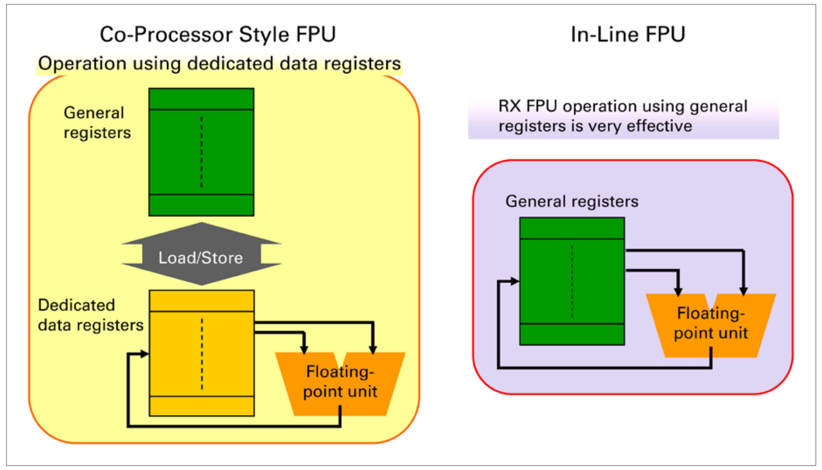


Figure 2: RX600 FPU implementation uses general registers to execute all instructions

The RX600 core includes an IEE-754-compliant, single-precision 32-bit FPU, tightly coupled to the CPU, sharing the same registers (Fig. 2). Competing architectures need an extra step of loading operand values into the general registers first and then moving them into the floating point's dedicated registers. The results of the floating point unit are subsequently moved to the dedicated register and back to the general registers to be then stored into memory.

The RX CPU achieves 165 DMIPS (Dhrystone 7 MIPS) and 32-bit multiplications can be performed in, at best, a single cycle (divisions require 2 to 8 cycles), so vector calculations for motor control are extremely quick. Motor control algorithms developed using tools such as Matlab, can be directly ported to the FPU for system testing.

Summary
An FPU closely coupled to the CPU core brings higher performance and simpler software development to motor control applications. The CPU bandwidth usage of the FPU SVC is reduced significantly compared to fixed-point SVC. The code size of the FPU SVC is only half of the fixed-point SVC, which makes it possible to use an lower cost MCU with smaller flash size. Adding an FPU in an MCU allows computationally advanced algorithms, improving motor control efficiency and saving energy while extending system capability.

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PE ENGINEERS FACE COMMON CHALLENGES IN MOTOR DRIVE DESIGN

By: David G. Morrison

In my last column, I discussed trends in the development of industrial drives and the challenges those trends pose to power electronics (PE) engineers developing motor drives for that marketplace. In this issue, I look more broadly at the field of motor drive development and the design challenges faced by PE engineers working across a wide spectrum of applications.

Motors drives represent a truly diverse field taking in everything from aerospace to appliances, automotive to industrial, and more. But despite the many disparities among the various end products, there are some commonalities among motor drive requirements in different areas. These include demand for higher efficiency, the choice of modular versus discrete design, the potentially game-changing nature of GaN and SiC devices, and the question of how to make the most of advanced control methods. Two engineers well versed in the development of motion control ICs and their applications explain how these issues are among the biggest motor-drive design challenges for PE engineers.

The Quest for Higher Efficiency
As in most areas of power electronics, efficiency is a top priority in motor drive design. But according to Aengus Murray, motor control systems engineering manager at Analog Devices, existing designs have already achieved a high level of efficiency.

"Efficiency is still the number one priority in power inverter design," says Murray. "The challenge is how to make improvements in what is already an almost fully optimized system. In higher-power systems, PE engineers need to start looking at second- and third-order effects to secure the extra energy savings."

Discrete versus Modular Design
Whether it's the pursuit of greater efficiency or some other improvement, PE engineers depend on the development of new components to achieve their design goals. However, even as the new parts address a need in one area, they create new issues that must be addressed in other areas.

That would appear to be the case with the development of integrated power modules for motor drives. "Integrated power modules are expanding in power range and functionality," says

Murray. "This has simplified the power circuit layout and mechanical design tasks but has created a new set of challenges. The PE engineer does not have access to all nodes of the power circuit and must rely on vendor information or modeling tools to validate the thermal and electrical design."

And despite the benefits of integrated power modules, their use may involve tradeoffs in factors such as cost when compared with discrete components. Ali Husain, a system manager in International Rectifier's motion control group, says that his customers, who are mostly focused on appliance design, encounter this dilemma. Growth in the appliance markets is closely tied to the development of high-volume products for developing countries, where product pricing is a critical issue.

"In such places, there is strong pressure to reduce the price, while keeping the performance up or improving it over generations of the product," says Husain. "So there's a constant tradeoff between using components with more integration, such as modules for motor drive inverters, versus doing it with discretes. Making that kind of tradeoff is one of the critical things I see customers struggling with a lot."

The issue of whether to use modules or discretes affects motor drive design in many application areas. In part, this is because the development of modules for one market segment affects another. According to Murray, appliance needs are driving the development of lower power modules, but industrial drive developers also stand to benefit from the size reduction made possible by these modules. In other words, says Murray, "The appliance market has the volumes to justify development of cost-effective modules that also meet industrial market needs."

Aside from the modules, in general, new components mean designers have more choices to evaluate, which necessarily makes certain design decisions more complex. Safety isolation is an example, and Murray observes that achieving safety isolation in motor drives remains a challenge for PE engineers because of the difficulty of meeting the many required standards. This task is further complicated by the variety of possible solutions for achieving isolation.

"These days, the PE engineer has a number of additional options available beyond traditional optical isolation," says Murray, who notes that newer chip-scale transformer technologies provide isolation with better channel matching, smaller size, and other benefits. "However, the engineer must perform a full evaluation to make sure he secures all the technical advantages without losing any of the performance or functions of the older technology."

Preparing for Compound Semiconductors

Perhaps the greatest challenge at the component level is yet to come as new power switches based on GaN and SiC materials are being prepared and promoted by power semiconductor suppliers.

"These technologies are not yet mature enough for production but the PE engineer must be ready to take full advantage of them when they are ready. He does not want to have to start learning how to use them after he discovers them inside a competitor's product. He would also like to avoid wasting time evaluating suboptimal technology," says Murray, who notes that "PE engineers will soon be revisiting their semiconductor materials texts and starting to look at power device physics again."

Husain concurs that the new power switches are not yet ready, but also notes that they are not that far away from being viable in motor drives, even the appliance designs that his group focuses on. Nevertheless, there is still much uncertainty regarding what their actual impact will be.

"Silicon carbide and gallium nitride will very much change the footprint of an inverter for a particular power level," says Husain. "Though they're starting to appear on the market now, I think those devices are still at least three to five years away from broad adoption. However, it's still not 100% clear if they will be useful for a broad variety of motor drives."

According to Husain, some of the skepticism or uncertainty regarding the possible impact of GaN or SiC devices stems from the fact they will exhibit different switching characteristics than the existing silicon power switches and the full impact of those characteristics on the motor drive design is not yet understood. For example, says Husain, "the new materials are not well characterized in terms of the EMI they're going to produce."

Echoing Murray's comments, Husain discusses how PE engineers will have to understand the operation of these components thoroughly in order to use them. "When they [SiC and Gan devices] come out, if you really want to get the most out of them, you'll need to know more than simply 'are they going to cut my losses by 50%' or 'I have this much less thermals so I can cram it [the inverter] into a smaller space.' There are more subtle effects that you should note about the way these new devices switch."

Ultimately however, there will be a strong incentive to master an understanding of how SiC and GaN devices work. "When GaN and SiC power switch technologies mature they will change the rules of the game," says Murray. "The PE engineer who best understands the new rules can gain the competitive advantage. The last time there was such a change in inverter switch technology for drives was when the IGBT was introduced to the market. It will be interesting to see what emerges as the IGBT replacement over the next number of years."

Leveraging Advanced Control Methods

Control schemes present other challenges to motor drive designers. The trend in recent years has been a move away from simple types of open-loop control such as volt-hertz to the more complex, closed-loop methods such as field oriented control (FOC). According to Husain, the adoption of FOC has required companies to either bring FOC expertise in house or to outsource the work to a design house. He notes that the implementation of FOC becomes very application specific.

"In field oriented control, you have a lot more information about what the motor is doing and the state of the motor—how much torque it's supplying, the speed ripple, and so on. So you can actually infer something about the characteristics and behavior of your load," says Husain.

FOC opens up new possibilities in terms of motor drive features that may add value to the end product. But this also means there are more decisions to make about the design of the overall system.

According to Husain, the designer must ask, "Now that I have this extra information, what am I going to do with it to improve my application? For example, in a washing machine, you can do unbalance detection just by observing your motor control parameters. And then in air conditioners, it may be something like vibration suppression or noise reduction. So, first, there are the technical challenges of designing the system and having the expertise to do it. But then the next step is making the most of that control system to enhance your specific application performance."

Again, in appliance design, these decisions will be affected by the price points that companies are trying to reach in designing products for the developing world. "Now appliance makers are really looking at the developing world as the target customers. How do you create something that's cost effective for them, but has the performance they have come to expect from their exposure to products made for the developed world?"

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TOWARDS ZERO STANDBY POWER-DESIGNERS MEET NEW ENERGY REGULATIONS

By: Andrew Smith

In order to meet ever-more-stringent energy consumption limits, designers of an increasingly wide range of products have to change their design practices and spend more time researching solutions and new technologies. This pattern is a worldwide trend with tough standards being driven out of China, Europe and the USA. Additionally, the global nature of business in 2012 means that no region stands in isolation and many products must be designed to meet all international regulations. Initially, regulators targeted external power supplies because they are easy to separate from the system that they supply. Now, however, a much wider portfolio of products is being considered including computers/displays, imaging equipment, laundry driers, vacuum cleaners and even domestic coffee machines. And in Europe, there is already a long list of other products that will be investigated, analysed and eventually be subject to mandatory efficiency performance standards.

When agreeing on minimum efficiency performance, the energy regulators tend to map the efficiency performance of a cross-section of the market and base performance targets on what is being achieved by a percentage of the best-performing products that are currently available.

One particular issue that has been bothering regulators worldwide is the amount of energy that products consume whilst in standby mode, and many of the emerging efficiency formulae are split into two parts examining elements for standby and no-load power, as well as for full operational mode consumption.

The target is, of course, 'zero no-load', where a product consumes absolutely no power when idle. Currently there is no international standard that requires zero standby power usage for any products; however, there is a clear move in this direction, and a genuine commitment to drive down energy consumption within the electronics industry and certainly among the major OEMs. The IEC has even defined "zero power" as less than 0.005 W (IEC62301 Clause 4.5 rounds standby power use below 5 mW to zero).

The good news is that reducing standby power is really a matter of careful design and appropriate power IC choice, which costs nothing more than the will to change and an innovative attitude. Whereas system designers may be limited in what they are able to achieve, IC designers have much more flexibility to innovate new solutions.

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