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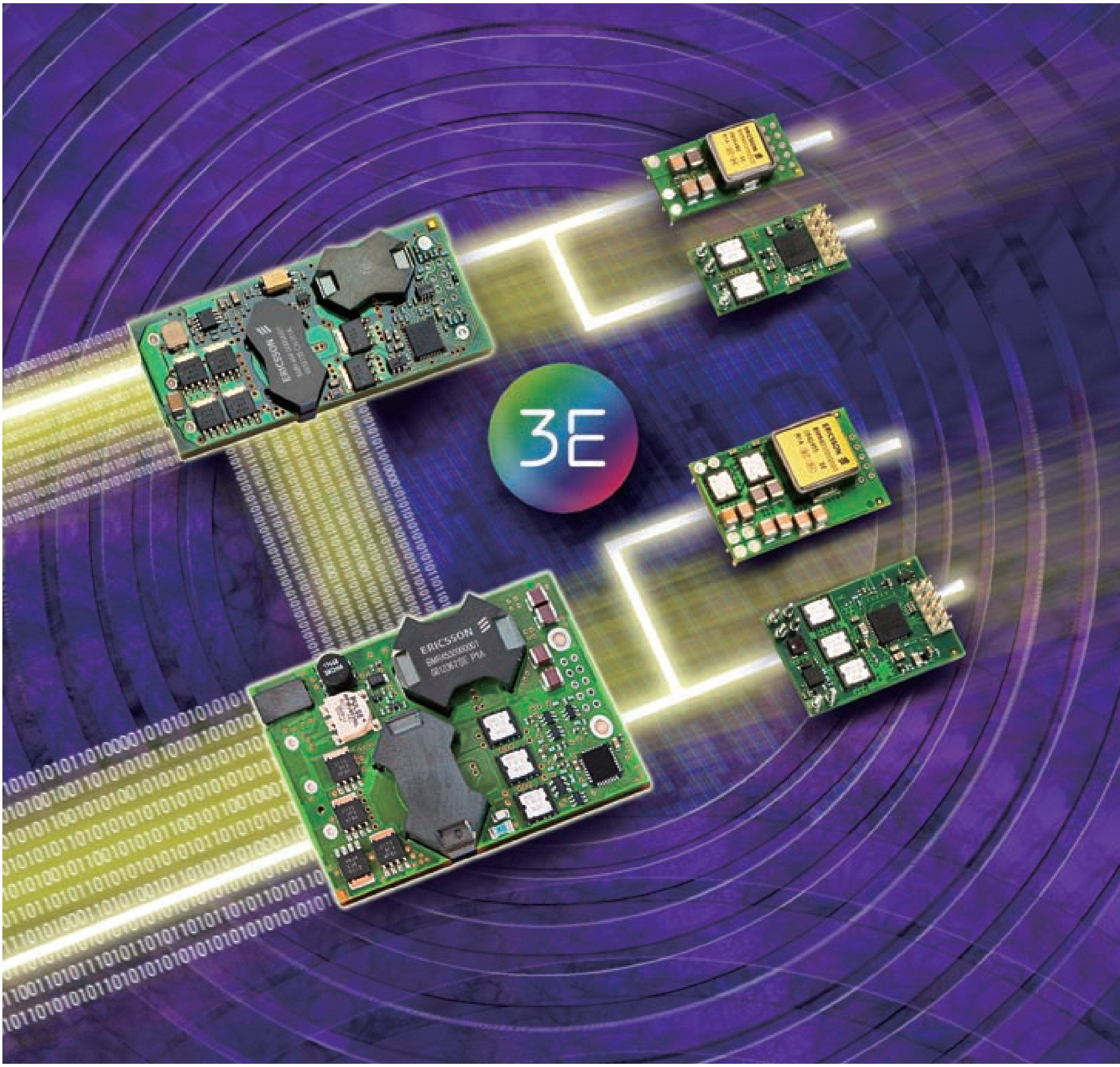

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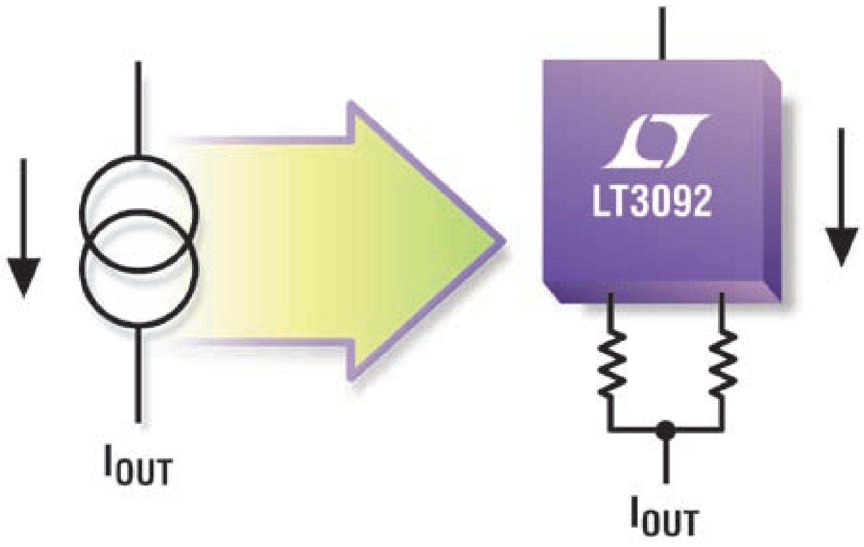

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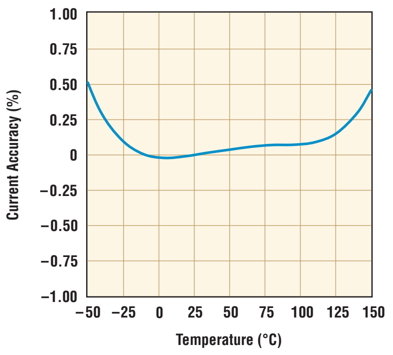

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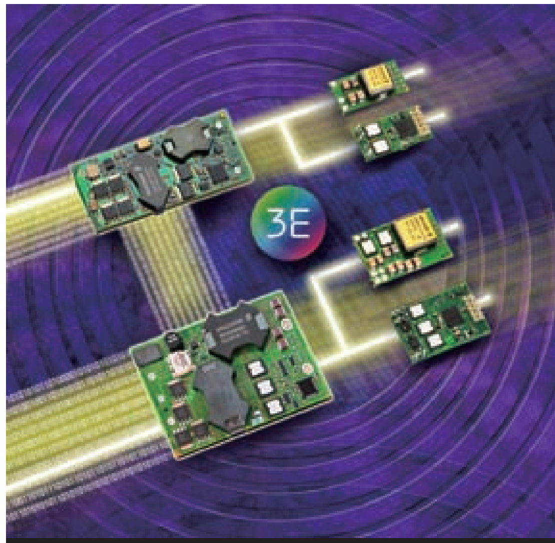

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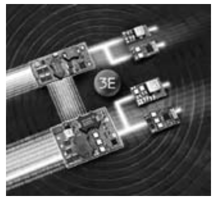

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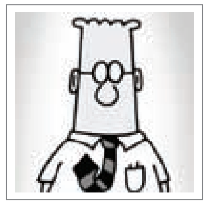

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Volume 2, Issue 6

THE COMMUNICATIONS CONUNDRUM

Welcome this special issue of PSD where we run a feature on 'Powering Communications'. We hope you like the new look of our magazine and the advanced features of our new website.

It is just incomprehensible to imagine the way we live and work today without the richness and connectivity that modern communications systems provide. We can be connected by our cell phones, tablet PCs, computers and even our home entertainment systems as never before. Communications systems need to provide a wealth of features and dependable bandwidth, all of which require sophisticated power management for base, remote or portable operation.

Powering these feature-and-connectivity-rich devices with increasing demand on power, and importantly, its management has become a critical issue. Manufacturers want to differentiate and provide their customers with a wide variety of applications and yet the power unit, normally a battery, has a very limited capacity. Battery technology is not moving as fast as we would like and therefore engineers must be frugal in their designs.

Global subscribers to wideband telco services such as Fiber To The Home (FTTH) and VDSL are expected to rise at more than triple the rate of ADSL during the next few years as carriers seek to boost their networks' performance, according to iSuppli Corp. The telco broadband market is undergoing a seismic shift in technology as technologies like ADSL begin to give way to wideband services like FTTH and VDSL. While ADSL will continue to dominate most telcos' broadband installed bases for years to come, subscribership has begun to contract in many developed countries such as the United States, Japan, Korea, Canada and Germany.

Rising competition from other industries is compelling the telcos to turn to wideband technology. Telcos around the world are facing stiff competition from competitive access suppliers, cable providers and wireless operators. This competitive pressure, which has resulted in stagnating revenues and subscribers eroding by as much as 10% per year, has caused telephone companies to rethink how they do business in the residential space. Virtually all carriers, as well as competitive access suppliers, have chosen a strategy of deploying value-added services, such as IPTV, in combination with their core residential business of voice and data in order to stop subscriber erosion and to increase subscriber Average Revenue Per User (ARPU).

Among bandwidth-intensive applications, IPTV is one of the few that has proven to be successful with subscribers. However, telcos plan to offer other services to boost revenue during the next few years, including 3-D HDTV, cloud-based Digital Video Recording (DVR), distance learning, video telephony, home automation and remote home networking management.

Enjoy the issue. Your feedback is valuable to us, and do check out Dilbert at the back of the magazine.

All the best,

Cliff
Editorial Director & Editor-in-Chief, Power Systems Design
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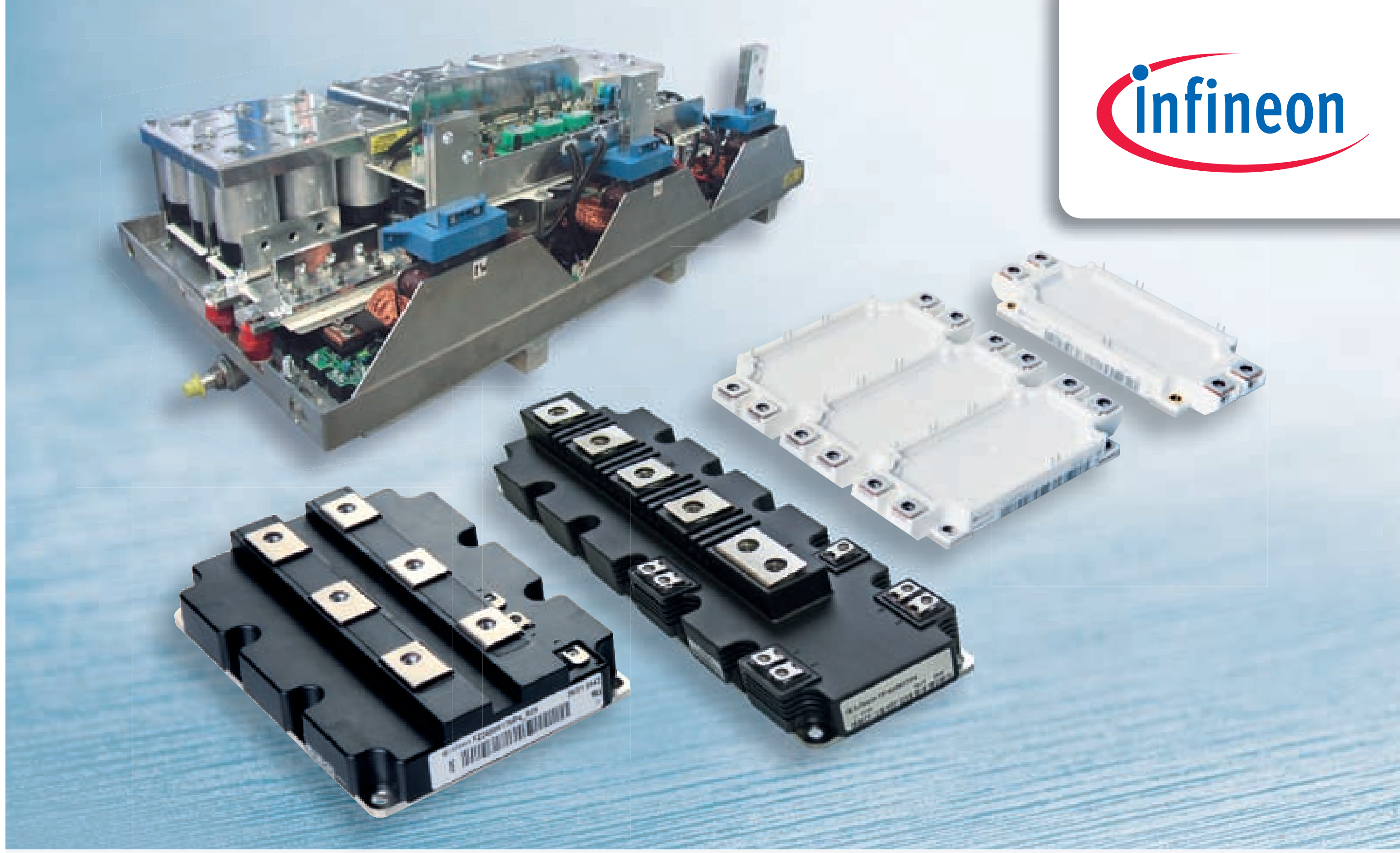

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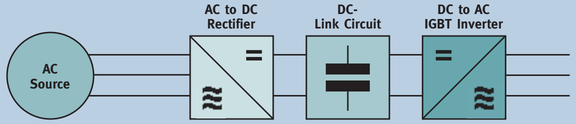

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REDUCED POWER AND COST OF POE

Silicon Laboratories introduced the Si348x family of power management ICs, enabling reduced system cost and improved efficiency in power over Ethernet (PoE) power sourcing equipment (PSE). Complementing its Si3452 PSE controllers, the new PoE power management ICs provide an easy-to-use, energy-efficient and small-footprint solution for streamlining power delivery in managed and unmanaged switches and routers, iPBXs, IP-based security systems, set-top boxes and power injectors.

The PoE+ standard allows up to 30W per port to be sourced by the PSE, requiring 720W total in a 24-port system. At any given time, most of these ports may not be in use or drawing full power. Silicon Labs' Si348x power management ICs' real-time voltage and current monitoring capabilities of the Si3452 PoE controller apply active power management based on actual consumption, enhancing the efficient use of switch ports beyond simple classification schemes.

For compact systems of eight ports or less, the Si3480 provides a pin-programmable, stand-alone solution that does not require an interface to an intelligent host, making it ideal for unmanaged switches or other applications where the user wants full-featured active power management without having to write or integrate system software.

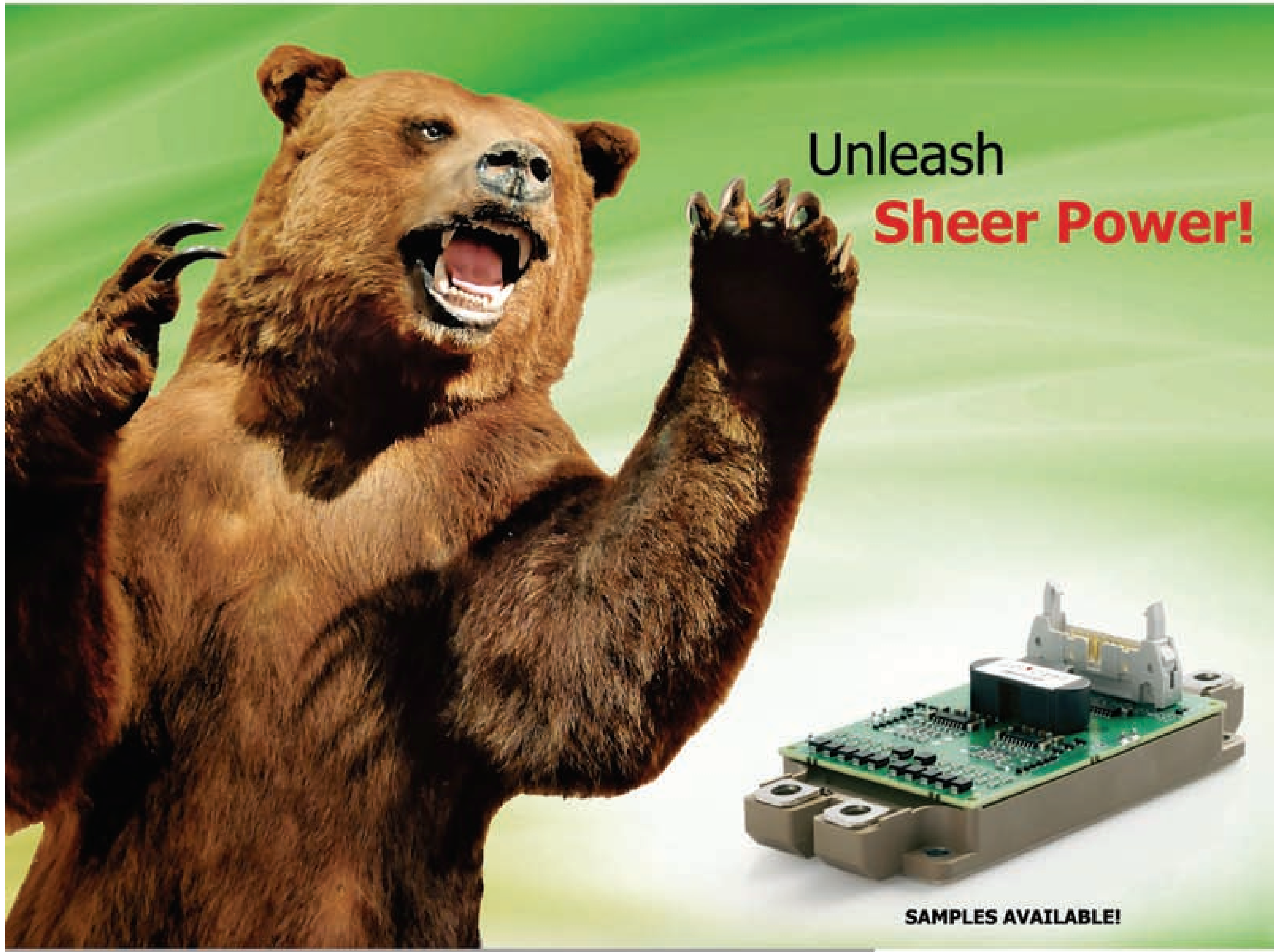
For larger PoE systems, the Si3482 leverages the real-time voltage and current monitoring capability of the Si3452 controller to manage up to 48 ports with as many as three power sources. The Si3482 can be programmed by its host via a serial peripheral interface (SPI) or universal asynchronous receiver/transmitter (UART) interface, setting the power supply capacity, port power configuration, port priority, detection timing and fault recovery protocol. Once programmed, the Si3482 can operate without host intervention using the saved configuration data and also facilitate link layer discovery protocol (LLDP) agents in the host, to dynamically adjust the amount of power granted to a PD during a connection.

Silicon Labs offers a complete suite of development tools including a graphical user interface (GUI)-based software development tool to enable quick evaluation and design with the Si348x ICs and companion Si3452 devices. The Si3480MS8-KIT development kit implements an 8-port midspan power injector with an intelligent power management LED display, enabling detailed evaluation of the Si3452 in conjunction with the Si3480 8-port power manager. The 24-port SmartPSE24-KIT power management evaluation kit supports SPI or UART-based interfaces and includes comprehensive power management functions to simplify designing with the Si3482 IC.

Quad-port PSE Controllers and Power Managers for PoE+
Si3452
Si3480
Si3482

For users who prefer a software-only solution, Silicon Labs offers a power manager software development kit (SDK) for systems that include an intelligent controller such as an Ethernet switch SoC. This SDK includes a power management kernel, GUI tool and an application programming interface (API). The SDK facilitates rapid porting to the switch controller, providing a turnkey power management capability for high port-count systems, leveraging the real-time monitoring capabilities of the Si3452 controller.

www.silabs.com/pr/PoE



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POWERING WIRELESS COMMUNICATIONS

By Fred Zust

The recent increased demand for 3G smart phones and wireless-enabled PDA-type devices will continue to drive the increase of mobile data traffic in the enterprise and consumer market spaces. The requirement for more data consumption for a richer multimedia experience will encourage service providers to add higher capacity 3.5G and 4G base stations to their existing wireless infrastructure mix, be they WiMAX or 3G LTE.

In 3.5G and 4G base station architectures, the increasing data rate and the push for a higher capacity of users per base station led to increasing backplane speeds between radio and baseband cards. This overall bandwidth increase, in turn, requires more multi-core digital signal processors (DSPs) interconnected in a standard cluster configuration on the baseband card with FPGAs and embedded processors in a peer-to-peer networking cluster.

Multi-core DSPs now offer architectures with three to six cores, operating in the Gigahertz-per-core range. Data rates between processing elements and the back plane can range from 1 gigabit to as high as 10Gbps, all of which are supported by semiconductors that use the RapidIO 1.3 standard. Continued demands for greater bandwidth have resulted in a market need for higher data rates between processing elements, while at the same time, maintaining low latency, deterministic reliable packet delivery plus an easy-to-manage memory map. All of these are attributes supported by RapidIO 1.3

The above market drivers led to the Serial RapidIO® 2.1 standard. Leading wireless infrastructure equipment providers are adopting this technology in their next-generation platform designs to increase overall system performance and support more subscribers per base station with more revenue-generating, real-time multimedia features. But Serial RapidIO 2.1 is not limited to the rollout of new platforms or upgrades of base stations to 4G standards.

In some cases, Serial RapidIO 2.1 is ideal for cost-reduction and power-saving measures in legacy platform updates because Serial RapidIO 2.1 can support more bandwidth per serial link, doubling the baud rate on a link from 3.125Gbaud in Serial RapidIO 1.3 to 6.25Gbaud in Serial RapidIO 2.1. Moreover, it can be transmitted up to 100cm over two connectors, making it ideal for cascading multiple chassis co-located in one physical rack, immediately expanding the processing capacity of a base station.

Serial RapidIO 2.1 also adds support for Virtual Channels (VCs) and Virtual Output Queuing (VOQs), improving overall traffic management and allowing OEMs to support more bandwidth in the network with differentiated classes of service, ideal for 4G networks being developed today.

Improvements to Quality of Service (QoS) will appeal to carrier-grade communications applications. Within the physical layer, the new standard additions receive equalization capabilities that will allow it to support extended long-reach (100cm) traces at the full data rate. This can even be done with conventional FR4-based PC board materials.

In embedded systems, all of the above features are only supported by RapidIO. While 10 Gigabit Ethernet offers some of the attributes that RapidIO 2.1 offers, given that it originates from the LAN/WAN networks, using it in multiprocessor embedded systems for peer-to-peer processing can be difficult due to its higher latency, non-deterministic packet delivery, large packets sizes (causing system-level congestion) and large processor overhead in terminating the protocol, reducing processor cycles for application implementation. The 10 Gigabit Ethernet raw data rate is only half of what is available with Serial RapidIO 2.1. Wireless system OEMs, as well as those in other embedded markets, have chosen to continue from their existing RapidIO 1.3 investments and are moving forward with Serial RapidIO 2.1.

The continuous advances in the wireless infrastructure create the need for significant increases in system capability and bandwidth. The industry has responded with the evolution of its most successful interface standard to meet the needs for more bandwidth, more flexibility and better quality of service. Serial RapidIO 2.1 addresses all of these needs and maintains backward compatibility with the previous versions of the specification — helping to keep the installed infrastructure base from becoming obsolete.

Author: Fred Zust
Vice President & General Manager, Communications Division
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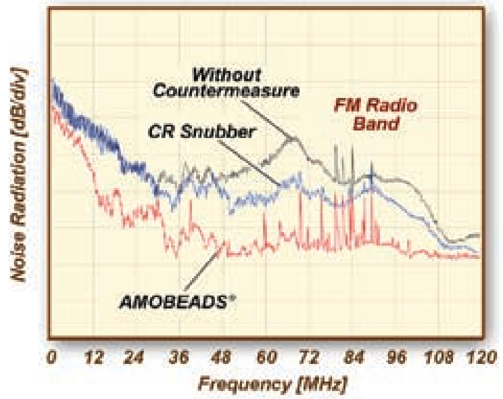

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IN-FLIGHT CONNECTIVITY IS HERE TO STAY

By Matthew Towers

Historically, the aerospace market has been something of a niche, with most electronics confined to cockpit and flight operations functions, and addressed by specialist electronics manufacturers.

In recent years, electronics content has started to mushroom. At first this was driven by growing demand for personal "in-seat" entertainment systems. These were introduced initially into premium cabins but have rapidly moved into economy/coach for long haul travel, providing a plethora of entertainment facilities including video, audio, and gaming. The newest generation of systems from leading suppliers, such as Panasonic and Thales, are more advanced, offering bigger and higher quality displays, new functionality, and better reliability. In the newest Boeing and Airbus aircraft, the cost of the in-flight entertainment system can now sometimes exceed the cost of the engines, thus becoming the second biggest hardware expense after the air-frame.

Looking ahead, further innovation is on the way that will drive even more electronics into the aerospace market. Connectivity is the current buzz-word in the industry and North American carriers are leading the way when it comes to in-flight Wi-Fi capability. Over 1,000 aircraft are now fitted out with Aircell's Gogo in-flight internet – meaning that approximately one-third of all North American flights offer the ability to go online while in the air. Many more are set to introduce this functionality in the coming years with low-cost carriers Southwest and Jet Blue the latest to announce deals with Row 44 and Viasat respectively.

> Although in-flight Wi-Fi on North American flights has now become relatively commonplace, this is not the case in other regions.

That said, a raft of airlines including Lufthansa, Emirates and Cathay Pacific have recently committed to providing access to the internet during flights in the near future, whilst many of the world's biggest airlines are still to make announcements.

However, unlike their US counterparts who are restricted by stringent FCC regulations, airlines operating out of Europe, for example, are able to offer cellular as well as Wi-Fi connectivity on-board their flights. As such, many have partnered with companies able to provide in-flight mobile connectivity such as Aeromobile and OnAir so that their passengers are able to use their mobile phones to text and call in the air.

The introduction of connectivity in the air will offer passengers even greater entertainment options whilst in-flight. Activities such as email, SMS messaging, web-surfing, live TV and on-line shopping will all become a reality. There are, however, still quite a number of issues to resolve. These include:

- Bandwidth – bandwidth into and out of the aircraft is still limited and this will restrict functionality initially.
- Investment – up-front investment required by the airlines can be large. At a time when the industry as a whole is not very profitable, this is making some airlines think very carefully before committing.
- Passenger attitudes – it is still unclear how passengers will feel about their close neighbour being able to place and receive cell-phone calls whilst in-flight.
- Regulations – FCC regulations in the US currently prohibit cell-phone calls in the air whilst over US airspace.

Despite these barriers, it appears that in-flight connectivity is here to stay, and in the longer term will become increasingly sophisticated and widely available.

One potential knock-on effect of the move to in-flight connectivity is that it will drive greater demand for in-seat power. Many airlines expect passengers to take advantage of connectivity in the air using their own devices – whether cell-phones, iPods, notebooks, netbooks or tablets like the iPad. Although battery life for many of these products continues to extend, it will still be highly convenient for passengers to have in-seat power provided so that batteries do not become exhausted or too depleted during long flights.

One thing seems clear. The days of executives "escaping" unconnected into the air for 10 hours, and enjoying some respite from the pressures of phone and email are numbered. Personally, I will be sorry to see them go!

Author: Matthew Towers
Senior Research Director - Communications
IMS Research
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POWER SUPPLY DEVELOPMENT DIARY

Part V

By Dr. Ray Ridley, Ridley Engineering

This article continues the series in which Dr. Ridley documents the processes involved in taking a power supply from the initial design to the full-power prototype. In part V, attention is turned to the secondary side of the converter, where snubbers and clamps are added to protect the output rectifiers.

Secondary Catch Diode Ringing Voltage

In Part IV of this series of articles [1], the primary voltage spikes on the switching FETs were properly controlled with improved layout and high-frequency bypass capacitors. This greatly improved the ruggedness of the converter.

Voltage spikes and ringing can also be seen on the secondary of the converter. Figure 1 shows the ringing across the catch diode with 100 VAC applied to the primary of the converter (maximum voltage rating is 280 VAC). This ringing must be suppressed before higher voltages can be applied to the converter. A peak voltage of 175 V is seen at the leading edge of the waveform, more than three times higher than the anticipated square wave voltage of 50 V. If this is not controlled, the secondary rectifiers will fail when full voltage is applied.

Secondary Catch Diode RCD Clamp Network

A simple RC snubber applied across the catch diode of the converter is not able to sufficiently control the peak of the ringing waveform. Instead, an RCD clamp is used, as shown in the schematic of Figure 2.

RCD clamps are most often applied on the primary of an offline converter where the peak voltage must be tightly regulated to avoid failures. However, they can also be used on converter secondaries, especially when the output voltages. The clamp diode and capacitor must be placed very close to the terminals of the catch diode for maximum effectiveness.

Figure 3 shows the effectiveness of a well-designed RCD clamp. The peak voltage is reduced to 90 V from 175 V.

Design of the components is quite straightforward. The capacitor is chosen so that it retains a relatively constant voltage over each switching cycle. A 600 V multilayer ceramic capacitor was used with a value of 68nF.

The diode of the clamp needs to be either a schottky, or a fast recovery type. In this converter, a Fairchild 3A ultrafast diode with a

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rating of 600 V was used (ES3J).

The value of the RCD resistor can be selected according to the process in [2], or can be chosen experimentally. The smaller the value of the resistor, the harder the voltage across the diode is clamped, at the expense of higher dissipation. Full analysis of the RCD snubber can be found in [2]. Although this article is specifically for the flyback converter, the procedure is the same.

The power dissipation in the RCD clamp can be reduced by connecting the resistor to the output voltage, instead of ground, as shown in Figure 4. Depending on the topology used, this can result in significant power savings. For the two-switch forward, approximately 40% of the energy is recovered at low line with this alternate connection. With this approach, the RCD clamp dissipates just above 1 W when the power supply operates at an output of around 400 W.

For very high power converters, you may also consider using a switching converter to discharge the clamp voltage. Active clamp networks can also be used but these add complexity and are beyond the scope of this article.

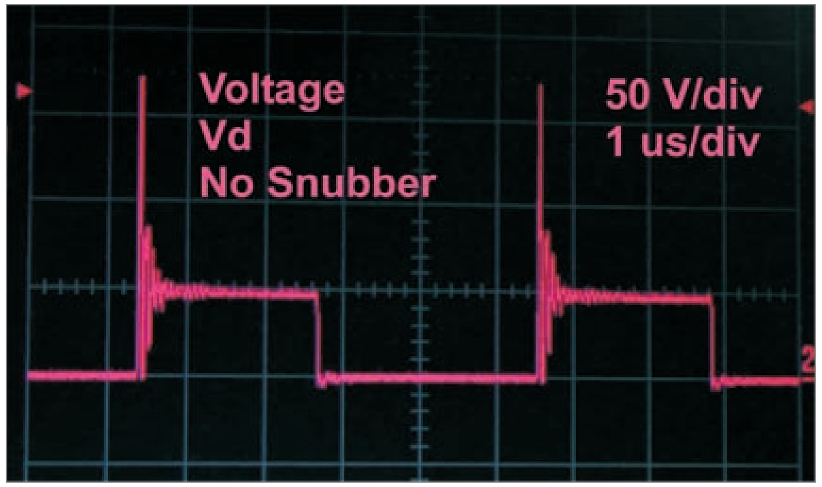

Figure 1: Secondary catch diode voltage waveform, VD, with 100 VAC applied and no snubber

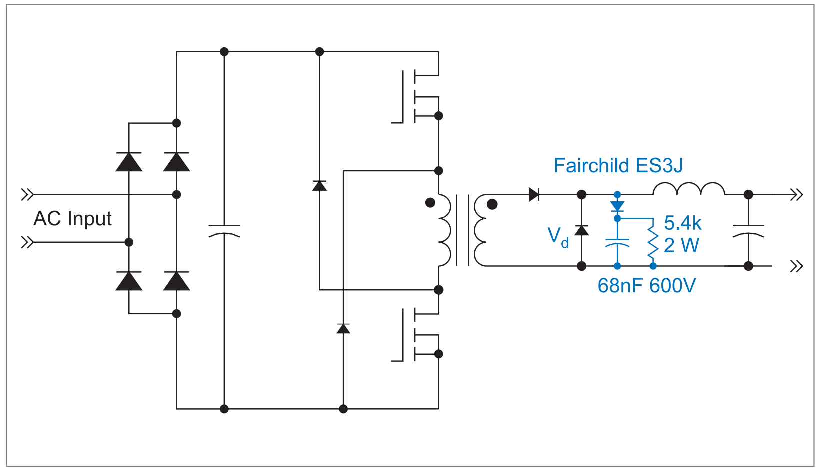

Figure 2: Schematic showing location of Secondary RCD clamp. Only one of the three outputs is shown for clarity.

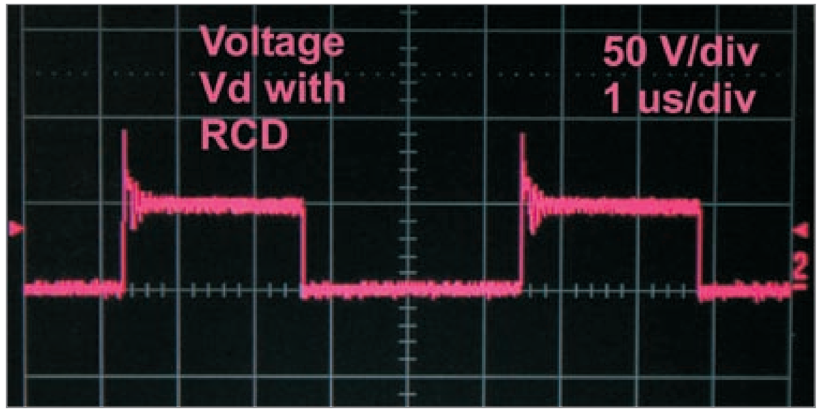

Figure 3: Secondary catch diode voltage waveform with 100 VAC applied and with RCD clamp

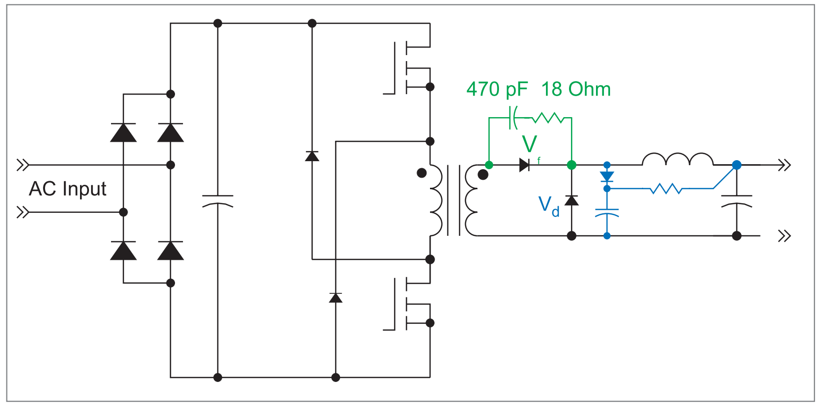

Figure 4: Schematic Showing Improved RCD clamp with lower dissipation, and RC Snubber added to protect the forward diode.

Secondary Forward Diode Waveform

The RCD clamp only protects the catch diode of the forward converter. It is also necessary to add a snubber across the forward diode on each of the converter outputs. Figure 5 shows the waveform across the forward diode before a snubber is added. The peak voltage spike seen is approximately twice the square wave value. A simple RC snubber is sufficient to reduce this spike to safe levels, as shown in Figure 6. The RC network is placed directly across the forward diode, as shown in Figure 4. The design process for these components is given in [2].

The design of the RCD clamp and the RC snubber must be replicated on the second main output of the power supply. The lower power outputs can usually be designed with RC snubbers only. However, it is important that even the lowest output power diodes be checked for ringing and properly protected if you want to maximize the reliability of your converter.

Summary

The diodes on the output of the forward converter are protected with a combination of RCD clamps, and RC snubbers. It is important that every power diode be protected with a snubber or clamp, and tested under all conditions to ensure that the peak voltage ratings of all devices are never exceeded.

So far, the power stage testing has followed this order:

1、Check gate drive circuit waveforms.A
2、Test primary circuit with resistive load.
3、Insert magnetics into circuit and verify low-voltage waveforms.
4、Design proper voltage clamps on primary switches.
5、Design proper voltage clamps and snubbers for secondary diodes.

All testing has been carried out at a relatively low input voltage – just 40% of the rated input. Before higher voltage testing is done, the overcurrent protection of the power supply must be thoroughly tested. This will be the topic of the next article in this series.

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www.ridleyengineering.com

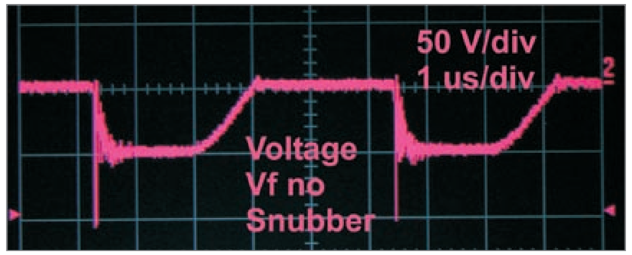

Figure 5: Secondary forward diode voltage waveform with 100 VAC applied and no snubber

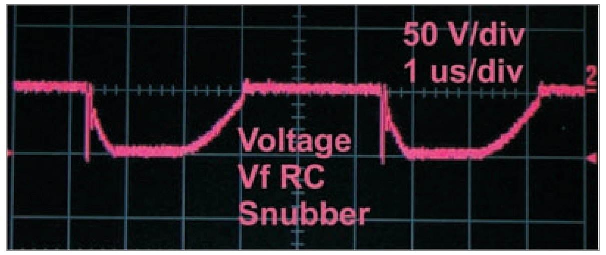

Figure 6: Secondary forward diode voltage waveform with 100 VAC applied and RC snubber.

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POWERING COMMUNICATIONS

Digital power techniques set new standards for flexibility

By Patrick Le Fèvre

Since the origin of mobile communication, various techniques based on software and hardware have been implemented to optimize energy efficiency. In every telecommunication system there are DC/DC converters and point-of-load conversion systems. The latest generation of power-modules embeds digital cores with communication interfaces to add a new functional dimension – flexibility.

Following a gestation period of several decades, digital power control techniques are rapidly gaining market share as designers increasingly appreciate the advantages that the technology offers over its analog counterpart. Despite even more uncertain economic times than those of today, estimates made by power industry analysts in August 2009 awarded digital power an approximately 20% compound annual growth rate for the next five years, and the likelihood is that this figure was somewhat pessimistic—the same analysts thought 45% more appropriate just twelve months previously. Forecast accuracy apart, the key to any technology achieving rapid acceptance and sustainable growth lies with delivering tangible benefits at competitive cost.

As many designers have discovered, the combination of digital power control and digital power management exceeds routine evolutionary expectations to represent a real, cost-effective step change in overall capability. Here, digital power control refers to implementing the inner control loop of a power converter with digital circuitry rather than using familiar analog schemes. For a simple buck converter, this means substituting an analog-to-digital converter for the traditional error-signal feedback amplifier, and deriving correction for the pulse-width modulator that drives the power switches using digital signal processing techniques in place of a voltage reference, ramp generator, and comparator.

Source: Ericsson

By contrast, digital power management denotes supervisory

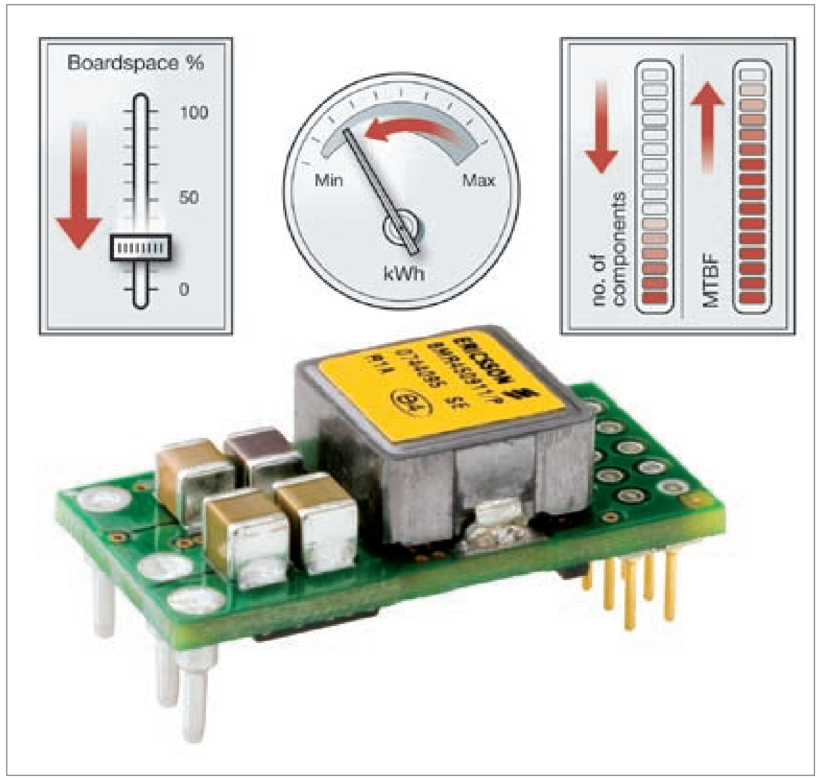


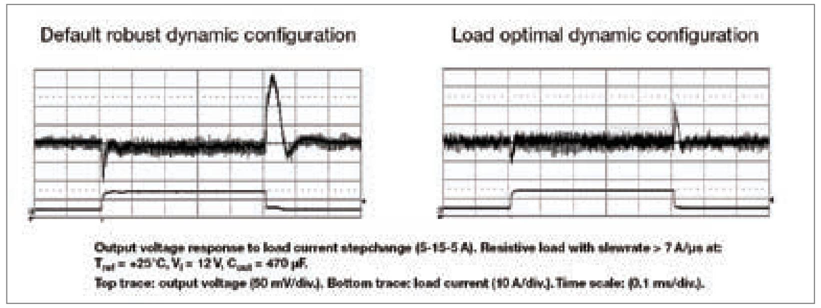
Figure 1: Highly integrated functionalities reduce board-space, increase efficiency and reliability

and control circuitry that communicates via a digital I/O scheme, which today almost invariably exploits the PMBus ™ interface that has become the power-industry standard. A converter that combines both of these digital power concepts can actively manage its conversion process to optimize efficiency for changing line and load conditions while including all of the power management system within the same package.

Digital configurability delivers life-cycle benefits

But digital power has much more to offer than bettering the electrical performance and power-density requirements that previously dominated the mindset of power supply designers. Essentially, such performance improvements are due to the ability of a digital control loop to adapt its dynamics to optimally suit line and load conditions in real time; by contrast, passive components set an analog converter's responses, which are inevitably a compromise between stability and dynamic response for the expected operating conditions. But in developing its 3E concept that embraces enhanced performance, energy management, and end-user value, Ericsson recognized that digital power could offer benefits that apply throughout a product's lifecycle.

As the digital converter's core is a mixed-signal IC it's possible to pack the supervisory measurement and control hardware together with its PMBus interface onto the same slice of silicon at negligible additional cost. This approach optimizes the electrical coupling between the converter's core and its control system, minimizes power consumption, and slashes the amount of PCB real estate that's necessary to accommodate equivalent functionality using analog-based solutions.



Output voltage response to load current stepchange (5-15-5 A). Resistive load with slewrate > 7 A/µs at: T_{ref} = +25°C, V_i = 12 V, C_{out} = 470 µF.
Top trace: output voltage (50 mV/div.). Bottom trace: load current (10 A/div.). Time scale: (0.1 ms/div.).

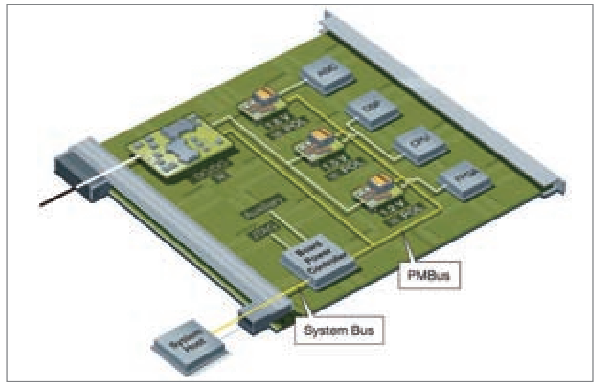
Figure 2: Reprogramming the control-loop constants in a digital power converter can optimize its dynamic performance for a given operating environment

Crucially, it's now possible to configure the digital converter when it is initially made, during the development phase of the power-system designer's application, at the distributor's depot, when the equipment is manufactured, and/or when it is operating within the end-user's equipment. This unparalleled degree of flexibility extends the programmable logic model to the power conversion industry for the first time.

Each 3E family power converter offers an array of programmable parameters that includes output voltage selection, turn-on/off delay times to implement power sequencing for multi-rail loads, slew rate control that provides inrush current protection, voltage margining for system testing, and multiple thresholds for warning and fault conditions for overcurrent, overtemperature, and under- and overvoltage. It's even possible to adjust the response of a digital converter's control loop to optimize its performance for a particular set of load and bulk output capacitance conditions.

Figure 2 shows the result of fine-tuning the constants that set the responses of a 3E point-of-load regulator's control loop to optimize its transient response for a given environment. This is the digital equivalent of moving the poles-and-zeroes in an analog converter by continuously adjusting the values of resistors and capacitors within its feedback

Figure 3: PMBus makes it easy to monitor and control compatible power-system devices such as the 3E family



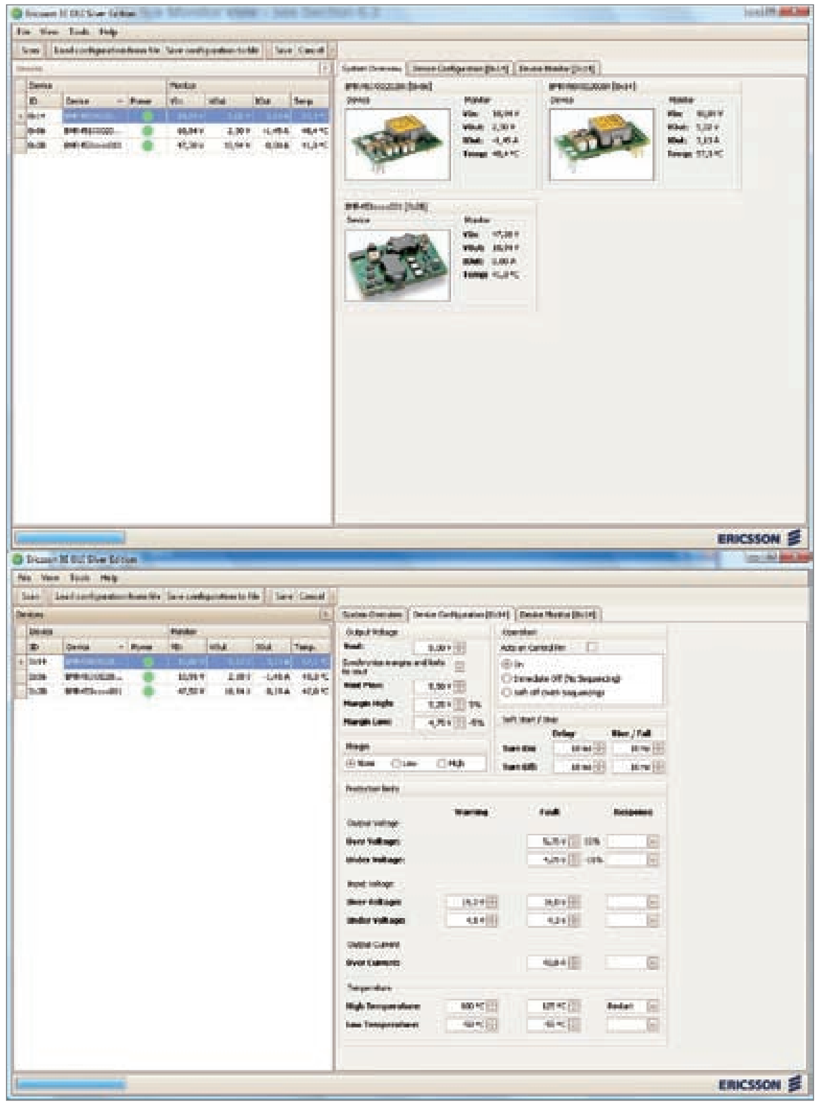


Figure 4: The 3E graphical user interface software greatly simplifies device configuration

loop, which is practically inconceivable.

PMBus™ is a key enabler

The PMBus can be invaluable during product evaluation and development. Here, the board power manager that controls PMBus-compatible devices might be a PC connected to a prototype board via a suitable adapter. Because the physical layer of PMBus relies upon SMBus—which is a development of I2C—PMBus is generally limited to the board domain, leaving designers free to implement their choice of backplane connectivity. Figure 3 shows the general scheme.

To make development immediately available, Ericsson developed a PC-compatible evaluation kit for 3E products that includes a USB-to-PMBus adapter and driver software that substitute for the board power manager. The PC and the kit's application software then assume the role of system host and user interface. This approach provides an extremely fast method for experimenting with parameters such as output voltage settings, power sequencing routines, voltage margining, and fault handling without any need for hardware changes on the board-under-test. When the designer is satisfied with a set-up, the application software can save a configuration file for each 3E device for later use.

While customers can request specific configurations, Ericsson most often delivers 3E parts pre-programmed with a default configuration that reflects a converter's typical application profile. For instance, users can order a point-of-load regulator such as the 20A-rated BMR450 preset to output 1.0, 3.3, 5.0, or 5.5VDC.

It is subsequently possible to reprogram the device to any level from 0.6 to 5.5VDC with 1mV resolution via the PMBus (it's also possible to set the product's output voltage from 0.7 to 5.0VDC in 25 steps with a resistor). As a result, one device covers a range of output voltages, permitting inventory reductions and easing logistics management. It's also worth noting that the BMR450 and its 40A companion BMR451 can share a common PCB layout, allowing designers to exchange converters as a system's power needs evolve. Similar benefits apply to all 3E family power converters.

If a one-time change of output voltage or any other programmable parameter is all that's necessary, a logical time to do this is at the ATE phase of board manufacture. Alternatively, a distributor may offer a programming service. Assuming a simple end-user application such as upgrading an analog design, it's possible to dispense with board power management logic on the target board. However, including full PMBus connectivity vastly improves the range of options that are available to power-system designers. As the PMBus requires just four conductors and a low-cost microcontroller easily accommodates the board power management logic, this approach is well worth considering.

Implementing PMBus connectivity allows the system host to monitor each PMBus-compatible device throughout the equipment's lifetime. Depending upon the sophistication of the system's supervisory software, this data-gathering ability might form the basis for energy cost analysis, root-cause failure analysis, or satisfy other user-specific functions. It may also help avoid system failures. For instance, if the supervisory software detects an unusually high pattern of warning conditions for a particular device, it may signal a service alert to swap out the suspect device before it fails. Similarly, if a power converter's output voltage drifts slightly over time or as a result of wide temperature variations, supervisory software could adjust the device back into full specification.

Another possibility that monitoring a board's power consumption offers is dynamic energy conservation, where supervisory software intelligently varies the output voltage that the intermediate bus converter supplies to the point-of-load regulators. Because virtually all power converters are least efficient at low loads, reprogramming the advanced bus converter from say 12VDC down to 9VDC saves power dissipation while the point-of-load regulators are running under light load.

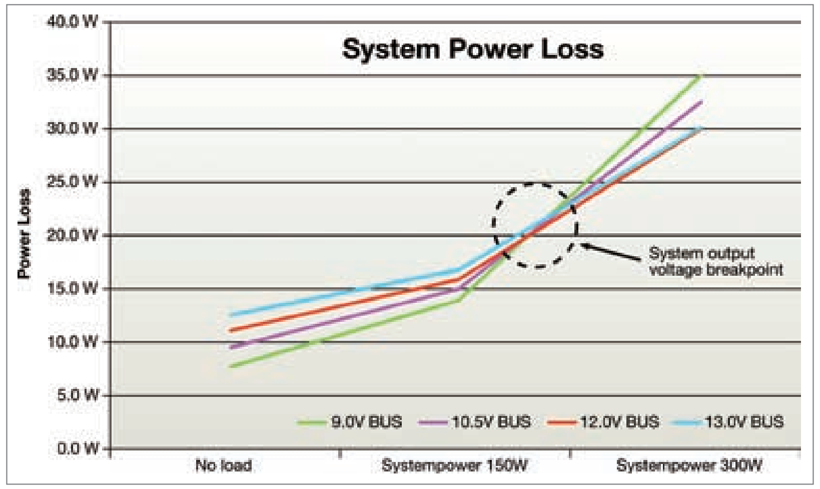


Figure 5: Adjusting advanced bus converter output voltage to payload condition reduces energy consumption

When more power is required, supervisory software can seamlessly ramp up the intermediate bus voltage to its optimal level for the new load conditions. Where a pair of power converters operate in a parallel current-sharing arrangement, it will save energy to turn off one if the load level falls within the capability of a single converter. This active approach to power management particularly suits systems that spend significant periods under widely different load conditions.

This is just the beginning

It's important to emphasize that these example scenarios represent just a few of the possibilities 3E power converters with PMBus connectivity make possible, and innovative designers will doubtless find new ones. Also, any of these converters can upgrade analog designs with no special effort on the designer's behalf. They can easily operate stand-alone as they offer analog-style functions such as output voltage adjustment via a single resistor, remote voltage sensing, and single-pin hardware on/off control. The "set-and-forget" capability that PMBus mandates also means that any 3E power converter can be pre-programmed with user-defined parameters that the device then retains for its lifetime or until re-programmed. This makes it possible to fine-tune a converter for a particular application without requiring PMBus in the target system.

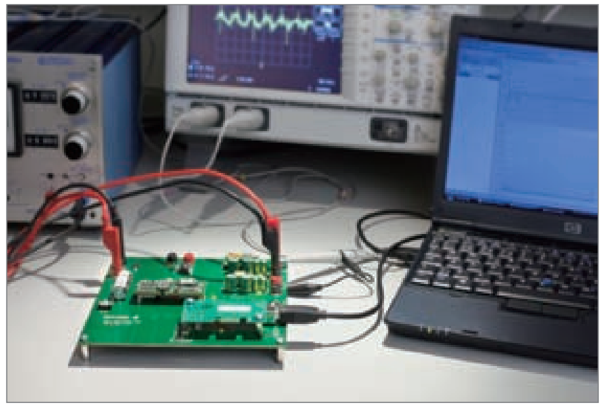


Figure 6: 3E evaluation kit simplifies learning, testing and programming

Compared with well-known analog techniques, the downside of digital power conversion is the very substantial amount of R&D effort that's necessary to produce a production-worthy digital converter—which is a prime reason for selecting proven, pre-qualified solutions. To help ease users into the digital power environment, Ericsson offers application engineering assistance and complements its evaluation kit with a large archive of technical papers and application information.

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OPTIMIZING POWER MODULES

The pursuit of industry best-in-class performance

By Werner Obermaier

In a world where energy efficiency is king, engineers, managers and purchasing departments alike need to examine carefully the route their company takes in the development of new products. It is no longer just a case of going back to the usual module suppliers. Total optimization is now absolutely vital and this can only be achieved cost-effectively with careful forethought and the right module manufacturer.

The market for power modules has proven to be highly successful and has taken a huge load off companies' purchasing and engineering departments by providing a compact, affordable solution which works right first time.

EMI and matching issues are all taken care of with negligible tweaks required. This is a giant leap forward from the traditional method of using discrete components which often required several expensive and time-burning iterations of laborious design to become optimized.

But now the market's requirement is not just for a fast and convenient solution. With the burgeoning adoption of UPS and solar energy sources and the proliferation of so-called solar farms, inverter efficiency takes on a completely new dimension. Every fraction of a percentage-point increase in terms of efficiency and reliability equates to profit. These systems are installed with the acknowledged expectation that they will run continuously (in the case of UPS) and maintenance-free for a predicted lifetime of up to twenty years. The individual components and topologies selected at the outset, determine the profitability of the operating system. It is a vitally important strategic, purchasing and technical decision to make - and one that cannot be taken lightly. Going back to regular suppliers in the belief that everything is optimized is an assumption that may result in a lost opportunity in the market differentiation of the final product.

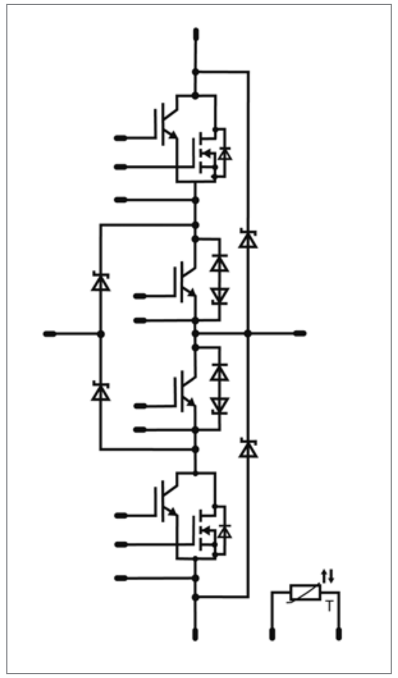
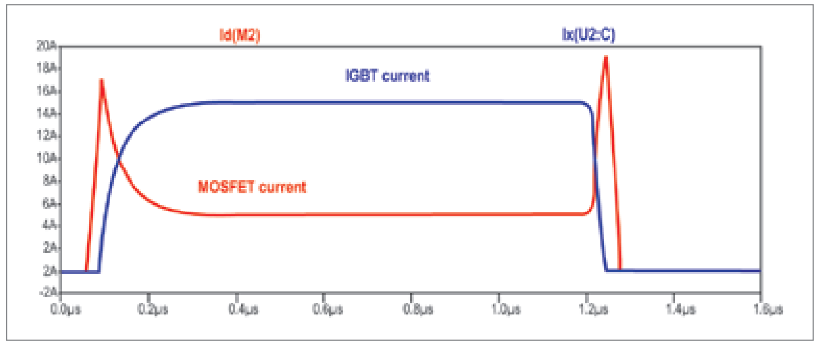


Figure 1: Circuit diagram of flowNPC 0 module FZ06NPA070FP with parallel switch (combination of MOSFET and IGBT) as outer switch

Figure 2: Typical current flow of MOSFET and IGBT in the parallel switch during one switching cycle



Most of the larger companies supplying power modules are constrained in their selection of individual components by corporate edicts and long term alliances, resulting in an adequate, although not necessarily optimum, solution.

With the hugely diverse range of components now available, the power module designer with no constraints on component selection is the only individual with the ability to truly optimize a system to maximize efficiency, reliability and profit for the end customer. Such scenarios are, however, rare. Working with general suppliers always results in a compromise solution.

Nothing less than the Optimum

While in the past a good product which could provide the required performance was good enough, with the globalization of the market and increased competition, this has changed significantly. Companies now have to develop the best possible product to maintain competitiveness. This, in turn, increases the attention to and demands on the individual components used in the product, which is especially true for components providing higher integration levels like power modules.

While power modules have become the standard power component for frequency inverters in industrial drives due to their high reliability, low assembly cost and long usable lifetime -and because of their high load cycle capability in combination with high power capability, this has not been the case in other areas such as solar inverters. The solar inverter market is still driven by the goal to reach the highest possible efficiency. This is normally achieved by using innovative although increasingly complex topologies like HERIC®, H5, NPC, mixed voltage NPC or similar, combined with state of the art semiconductors. In the past this was achieved in most cases by selecting discrete semiconductors from a variety of vendors to achieve the optimum solution. With today's increased complexity of these circuits, the higher power levels handled and the larger production volumes, the use of a power module as a subsystem would, in theory, become the obvious next step if it were not for one huge limitation: Most power module manufacturers are at the same time power semiconductor manufacturers making it almost impossible for them to use devices in their power modules from competitors - even where these would be a better, more efficient choice for the targeted application or topology.

Vincotech is in the unique position to focus on power module manufacturing only, which allows the company to choose from the widest range of semiconductor suppliers. This enables the company to provide modules with a completely optimized chip selection. One example of this is the flowNPC 0 module FZ06NPA070FP. Here, a combination of MOSFET and IGBT from different vendors is used to build an optimum

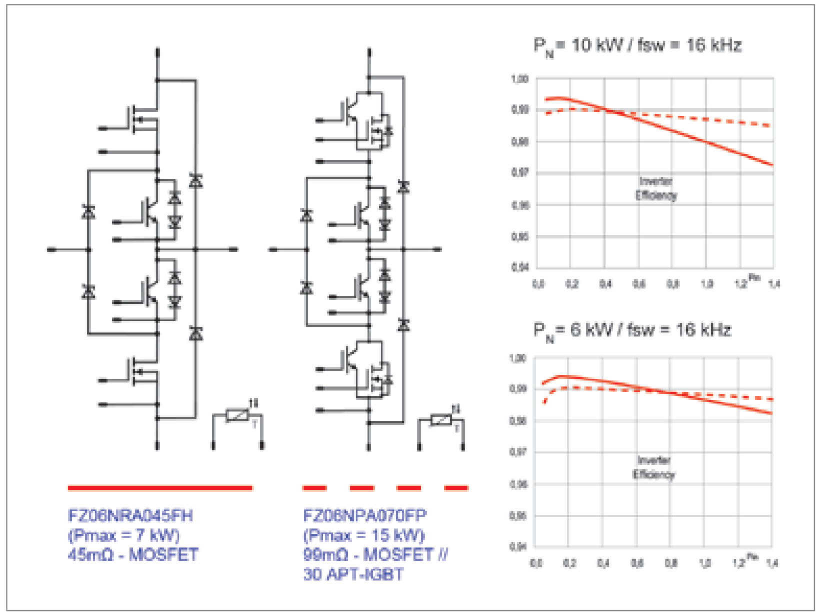


Figure 3: Comparison of module efficiency for MOSFET and parallel switch based modules at 6 and 10kW output power per phase

product, outperforming both a pure MOSFET and IGBT solution.

Figure 1 shows the circuit diagram of the FZ06NPA070FP module which contains the semiconductor for one phase of a 3 phase clamped neutral point inverter. The outer switch is built by a combination of MOSFET and IGBT and is used to generate the high frequency PWM signal. In this arrangement the MOSFET will be turned on first providing low turn on losses due to its high switching speed, while the IGBT will be turned on afterwards, adding high current low conduction loss capability during the most of the on-time. The turn-off will take place in the opposite sequence; turning off the low speed IGBT first, thus avoiding the normally present tail current with its inherent switching losses. The current waveform for the two devices during one cycle showing the current sharing can be seen in Figure 2.

Most IGBTs used in parallel switch configuration suffer from the effect in that the stored carrier will not recombine during periods where no collector emitter voltage is present, resulting in additional tail current when the MOSFET is turned off, which in-turn results in additional turn-off losses. This can be avoided by using Fairchild's PT-IGBTs as parallel switch.

Figure 3 shows a comparison of module efficiency at different nominal output power levels for the FZ06NPA070FP with the parallel switch and the FZ06NRA045FH with the single MOSFET switch. Both modules are using the same total chip size for the switch. The module with the pure MOSFET switch provides slightly higher efficiency at light load due to the resistive characteristic of the MOSFET, while the parallel switch provides higher efficiency over a wide output power range, resulting in a higher overall efficiency and in turn higher output power capability.

Conclusion

Power modules can provide benefits to power electronic equipment such as solar inverter and UPS, especially at higher power levels for more complex circuits and if high reliability levels have to be achieved. For optimum system performance, the combination of a variety of semiconductors, carefully selected from a broad range of semiconductor vendors is required - especially for the upcoming solar inverter market. Vincotech as a specialized power module manufacturer with its wide semiconductor supplier range, is best positioned and equipped to serve and deliver on these requirements.

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THERMOELECTRIC ENERGY

Harvesting and storage solutions

By Dave Koester

Advances in distributed sensors and sensor networks have led to an increased interest in renewable and autonomous power sources. The use of waste heat is an attractive source of energy for many applications where power on the order of μW-mW is required.

The implementation of a thermoelectric power conversion and energy storage system requires several basic elements in addition to an assumed heat source and electrical load. These elements, shown in schematic form in Figure 1, are: 1) a thermoelectric power generator (TEG), 2) a heat sink, 3) a power conditioning circuit that provides voltage up-conversion and regulation, 4) an energy storage device such as capacitor or battery, and 5) a power (load) management circuit. The interaction of these elements is critical to the performance of the system. The following provides further detail about each key element of the system and issues that affect system optimization.

Thermoelectric Power Generator (TEG)

The direct conversion of heat into electrical energy can be accomplished through the Seebeck effect in which heat flow through a thermoelectric device produces a voltage and current.

The basic building block of any TEG is the PN couple. The PN couple consists of a single element of P-type and N-type thermoelectric material that are connected electrically in series. Heat carries the

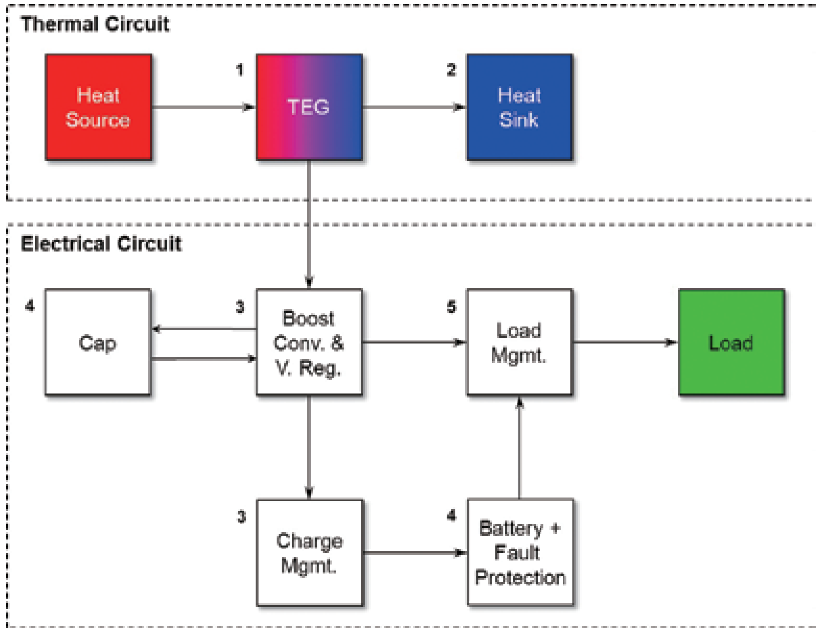


Figure 1: The design and optimization of a thermoelectric energy harvesting system is highly dependent on the relationships of these elements

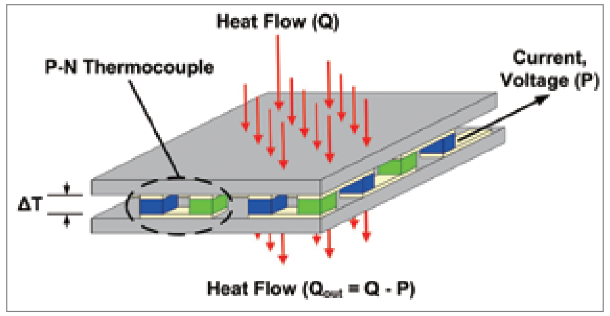
majority carriers from one junction to the other producing a current and voltage. By placing many PN couples in series electrically and in parallel thermally (see Fig. 2), a TEG can be constructed that generates a voltage proportional to the temperature differential (ΔT) across the elements. The current is a function of the number of PN couples.

Heat Rejection

In order to sustain a ΔT across a TEG, there must be heat flow through the device. This requires a heat source and a heat sink capable of rejecting the heat passing through the TEG.

Heat rejection can be accomplished in numerous ways including direct conduction to a large thermal mass, liquid cooling, spray cooling, phase change or simply through convection to the air using a traditional heat sink (the most common and often the lowest cost of these approaches). Heat sinks come in a vast array of sizes, dimensions and materials and choosing the proper one requires a thorough understanding of several key parameters. The parameter describing the ability of a heat sink to dissipate heat is the "thermal resistance," Θ. A low thermal resistance means the sink will do a good job of rejecting heat to the environment while a high thermal resistance will do a poor job. The thermal resistance of any heat sink is affected by the following:

Figure 2: Thermal-to-electric conversion with thermoelectrics. The ΔT across the module is related to the heat flow Q and the thermal conductance



Airflow Speed - The speed of the air flowing across the fins or pins of a heat sink plays a key role in the ability of the sink to dissipate heat to the environment. Even a small amount of air flow across a sink can substantially improve its performance relative to a case with no forced airflow known as natural convection (Fig. 3a). A fan can be used to improve performance but the fan will impact the overall conversion efficiency of the TEG system.

Size, Fin type, Dimension and Spacing - Size and geometry (such as aspect ratio), have a large impact on the performance of a heat sink (Fig. 3b). The optimal fin dimension and spacing depends on the fin material, mode of operation (natural or forced convection) and desired operating condition. Most applications seek to minimize the size of the heat sink. Such optimization requires understanding the operating boundary conditions like temperature and air flow to properly design the size, spacing and number of fins or pins.

Thermal Spreading Resistance - A large mismatch in footprint area between the heat source, TEG and base of the heat sink can lead to additional thermal resistance often referred to as spreading resistance. Performance can be improved by using a more thermally conductive material (such as copper) and/or varying the base plate thickness of the heat sink.

Gravitational Orientation - The performance of a heat sink in natural convection mode (i.e., no forced air movement) depends on the orientation of the fins relative to gravitational direction. The dependence of performance on orientation can be reduced somewhat by the use of pin fins rather than plate fins in the heat sink.

Voltage Regulation and Power Management

In cases where the ambient temperatures and heat flow are not constant, the output of the TEG will fluctuate. These fluctuations must either be tolerated by the load or eliminated by voltage conditioning and/or energy storage. Because the voltage output of a TEG is proportional to the temperature differential ΔT across the TEG, if the ΔT is small, it may be necessary to boost the voltage to the minimum usable value.

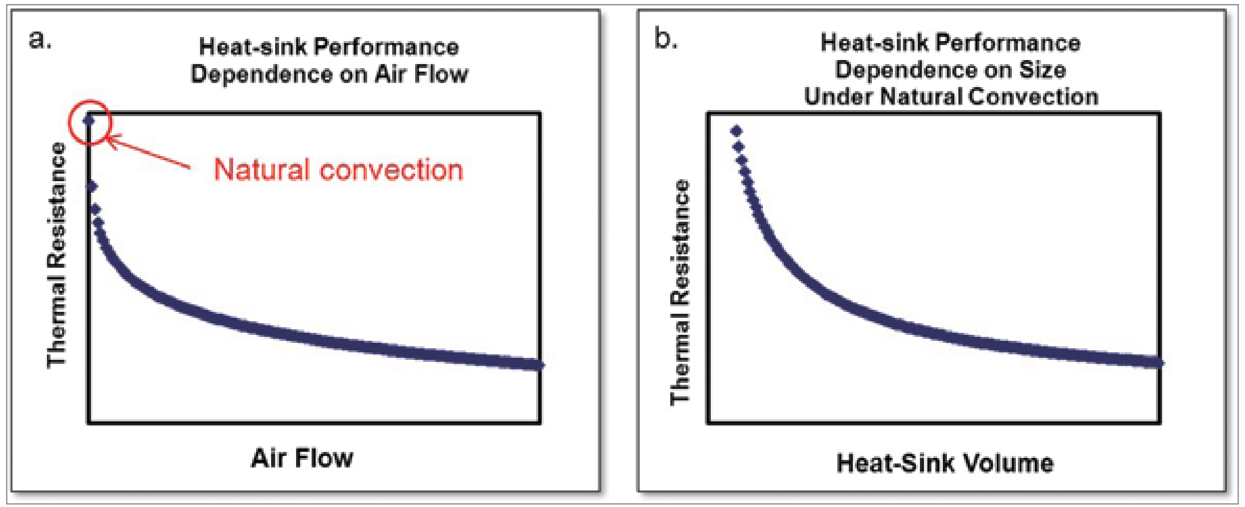


Figure 3: The performance of the heat sink is dependent on (a) the air flow with the special case being no air flow (natural convection) and (b) size

Boost Converters (>400mV) - Many of today's electronics require a minimum of 1.8V to 3V to operate but the heat source and TEG combination may be unable to generate such a voltage. Fortunately, there are numerous commercially available boost converters that can convert voltage from as low as 400mV to greater than 3V.

Micro-Power Up-Converters (>30mV) - Recent advancements in up-conversion now make it possible to up-convert voltages as low as 30 mV. This is particularly important in cases where the ΔT available from the heat sources is very low. One example of this is generating power from the human body were reasonable and achievable ΔTs are in the range of only 5-10K.

Energy Storage

Energy storage is needed when continued operation of the load is required while thermal energy is unavailable. Two general types of storage are used that offer differing characteristics. (1) Batteries (cells) provide high energy storage density but since the energy is stored chemically, the discharge rate is slow. The term "power density" is used to describe the limits on energy discharge. The other type of storage device is the capacitor. (2) Capacitors store energy physically by charging plates that can be quickly discharged. While the energy storage density of capacitors is smaller than batteries/cells, they have high discharge rates or power density making them ideal for quick bursts of power.

Systems will sometimes contain both types of storage especially if the load includes transient high-power devices such as a transmitter. Capacitors do not need any special circuitry to function well but batteries typically do. Charge management devices increase the lifetime of the battery or cell and are available from several manufacturers. They also aid in the performance of the system by allowing charging only when there is sufficient power available, in excess of what load requires.

Power Management

Lastly, power (load) management circuits switch the load between the boost convertor and the battery thereby isolating the cell from the output of the boost convertor. This benefits the cell by removing the drain and allowing it to charge when power is available directly from the boost convertor. This also minimizes the risk of a faulty or exhausted cell from shunting the output.

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POWER EFFICIENCY BREAKTHROUGH

Synchronous rectification of an LLC output

By John Stephens

With demand for high efficiency becoming part of product specification across the whole load range, design engineers are reviewing AC-DC power supply topologies with the specific aim of reducing power loss.

One such topology offering class-leading efficiency is illustrated in Figure 1. This article examines claims by IC manufacturers to have dealt with the last remaining large source of power losses in this topology: the output rectification stage.

Previous enhancements to this topology have produced improved Power Factor Correction (PFC) control ICs for the interleaved Boundary Conduction Mode (BCM) stage, and new LLC control ICs which enable more efficient designs.

So now losses in the output rectification stage of the LLC resonant converter tend to dominate the power losses budget. To make the next step forward in efficiency, synchronous rectification is required.

Two newly introduced ICs, from International Rectifier and Diodes Inc, are now being promoted as potential solutions to the problem. Before these devices reached the market, synchronous rectification for LLC resonant converters could not practically be implemented because of the complexity and difficulty of the technique.

The reality of synchronous rectification in resonant LLC circuits

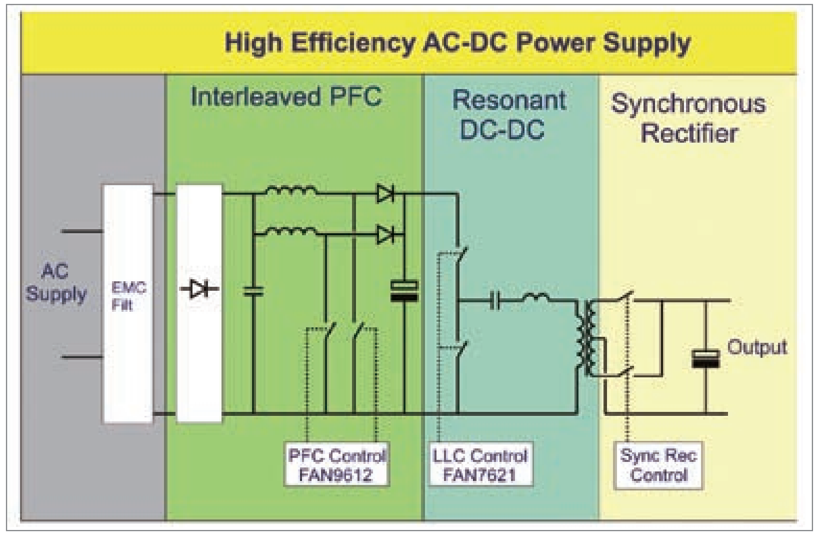

Figure 1: Topology of a high-efficiency AC-DC power supply

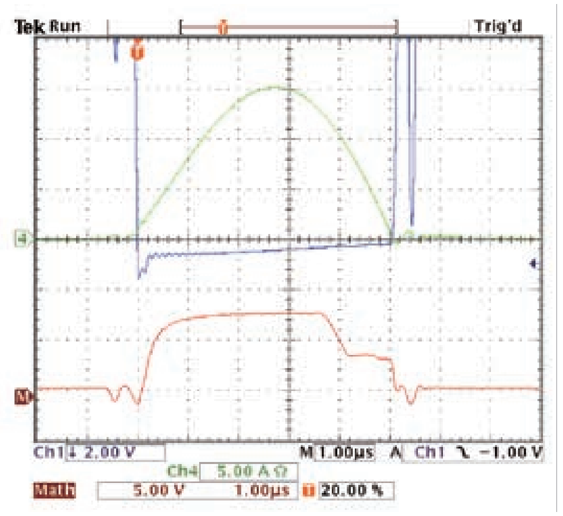

Figure 2: I_{ds}, V_{ds} and V_g 100% F.L. in ZXDG3103 circuit

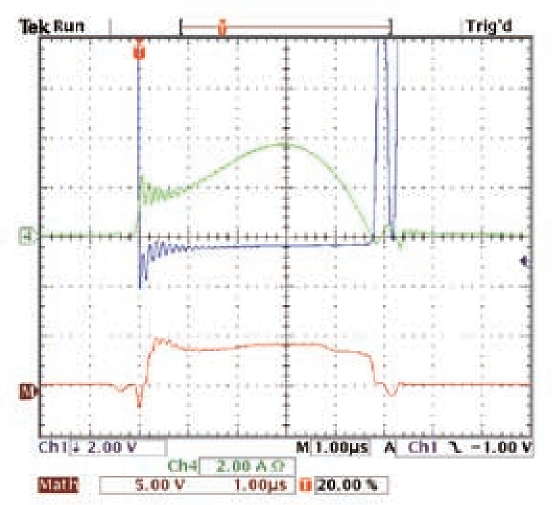

Figure 3: I_{ds}, V_{ds} and V_g at 25% of F.L. in ZXDG3103 circuit

For voltage-fed circuits, typical of the Pulse Width Modulation (PWM) or series-parallel resonant topologies, additional windings or tapping from the power transformer would suffice for driving the synchronous rectification circuits.

The LLC resonant topology is different: since it is a current-fed, capacitor-loaded structure, it cannot use the power transformer waveforms to drive synchronous rectification circuits. This is because the voltage on the secondary windings is connected to the output via the mosfet during its conduction time, and therefore holds the winding voltage until the mosfet switches off.

One method of resolving the problem is to sense the current flow and voltage around the mosfet. This requires the following functions:

- Current sensing (of I_{ds})
- Voltage sensing (of V_{ds})
- High-speed logic
- High-current gate drive

These sensing functions, and the use of their measurements, would be extremely difficult to implement in discrete components. Fortunately, two new ICs do the job for the design engineer: the ZXGD3103 from Diodes Inc, and International Rectifier's IR1168.

Both are secondary side drivers operating closely with the mosfet that replaces the Schottky diode. The ZXGD3103 is a single driver requiring two ICs, whereas the IR1168 is a dual driver requiring only one IC. Both sense the current by virtue of the drop in Vds at the mosfet, but their internal workings are different. (More details on the operation of these devices are available at www.diodes.com, and in Application Note AN-1139 on www.irf.com.)

The test circuits

To assess the extent to which these secondary side drivers can deliver power savings in the output rectification stage of LLC power supplies, a test set-up was devised based on an evaluation board developed by Fairchild Semiconductor. This is a 390Vdc input to 25Vdc output resonant LLC power supply capable of supplying 200W into a load.

To simplify the test set-up, only one half of the IR1168 – a dual driver IC - was used.

Figure 2 details the waveforms at full load (F.L.) and Figure 3 details the waveforms at 25% of F.L.
Ch1 = V_{ds} inverted
Ch4 = I_{ds} flowing to Co
Maths – V_{gs} (Ch2-Ch3) (where Ch2 – V_{dg} and Ch3 – V_{ds})

It is interesting to see in both diagrams the fast gate drive voltage. In ~200ns after detection of the parasitic diode forward volt drop within the MOSFET, Q1 turns on, reducing its voltage (Ch1 – V_{ds}).

In both tests, Q1 V_{ds} is higher than expected. This may be due to the circuit inductance and to the capabilities of the oscilloscope.

At full load, the gate drive voltage reduces as the sinusoidal current starts reducing. This is probably due to the inductance of the circuit and the inductance of the Q1 TO220 package. Improved layout and selection of a lower inductance packaging should resolve the issue.

As before, Figure 4 details the waveforms at F.L. and Figure 5 details the waveforms at 25% of F.L. for the test circuit using the IR1168 device.

Like the ZXGD3103, the IR1168 test circuits reveal a fast gate drive voltage – in <200ns after detection of the parasitic diode forward voltage drop within the mosfet, Q1 turns on, reducing its voltage (Ch1 – V_{ds}).

As before, Q1 Vds is higher than expected, probably for the same reasons.

In the full-load test circuit, the early termination of the gate drive voltage (Vgs) as the sinusoidal current starts reducing is probably due to the inductance of the circuit and the inductance of the Q1 TO220 package. As in the previous test circuit using the ZXGD3103, improved layout, reduction of resistances and selection of a lower inductance packaging should resolve the issue.

So how much power does implementation of synchronous rectification save?

The key reason for implementing synchronous rectification is to save power. The tables below detail the key parameters of interest.

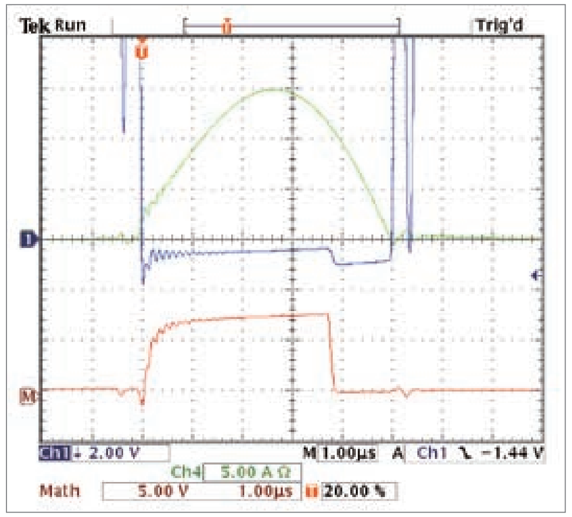

Figure 4: I_{ds}, V_{ds} and V_g at full load in IR1168 circuit

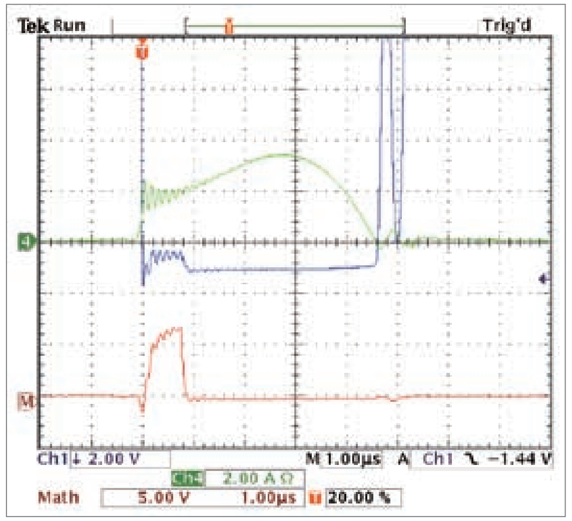

Figure 5: I_{ds}, V_{ds} and V_g at 25% of full load in IR1168 circuit

		Schottky Diodes	ZXDG3103+IRFB4110	IR1168+IRFB4110
Losses	W	13.52	8.85	9.73
Efficiency	%	93.7	95.8	95.4
Power Saving	W	reference	4.67	3.80

Table 1: power dissipation at 25% of F.L. (50W)

		Schottky Diodes	ZDG3103+IRFB4110	IR1168+IRFB4110
Losses	W	5.91	5.16	5.78
Efficiency	%	89.4	90.6	89.6
Power Saving	W	reference	0.74	0.13

Table 2: power dissipation at F.L. (200W)

With improved layout and mosfet package selection, both synchronous rectification circuits could exhibit even higher efficiency; the small differences in efficiency between the ZXGD3103 and IR1168 circuits shown in the tables are therefore not material.

What is clear is that substantial power savings are possible by implementing circuits that can be designed with little trouble by following the manufacturers' application guidelines.

What is also clear is that the threshold at which a power saving can be observed appears to be at around 25% of F.L. and above. At full load the Schottky diodes warm up the heat sink to the extent that a small fan is required for continuous operation. By contrast, the mosfet in the synchronous rectifier circuits can be operated at full load without a heat sink, and indeed in both cases was cool to the touch. This points to the possibility of a bill-of-materials savings to be made from the elimination of heat sinks and fans.

In conclusion, with the introduction of the ZXGD3103 and IR1168, the implementation of synchronous rectification of the output stage of LLC circuits has become a practical possibility. This new technique appears to deliver power savings anywhere from 25% of full load up to 100% of full load.

For more information on implementing high-efficiency power supplies, contact any branch of Future Electronics. The ZXGD3103 and IR1168 parts mentioned in this article are available to buy from Future Electronics.

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DESIGNER’S PERSPECTIVE

Semiconductor lifecycle management

By Eric Marcelot

It is estimated that 3% of the global pool of electronic components is made obsolete each month, and on a long term defence project, typically 50-70% of the semiconductor products incorporated are made obsolete before the program is even commissioned.

This is a very sobering thought for any designer settling down to spec a new system, especially so if they are working on a military or aerospace project that may take many years to delivery and then be expected to be in service for 10s of years thereafter.

This isn’t just a hypothetical scare story, it is being played out now. A case in point is the B-52 bomber, which e2v aerospace and defense Inc (previously QP Semiconductor) ships parts for on a weekly basis. This platform has been in service for over half a century and is likely to continue to be in operation for at least another 30 years. This means that a project that was initially supposed to have a 30-50 year life cycle will have exceeded 80 years by the time it is grounded.

It is therefore vital that a new approach is taken to managing and mitigating against the effects of Semiconductor obsolescence, an approach which can help with the platforms and systems being developed today as well as those already in service.

So what is being done to help?
e2v recently entered an agreement with Freescale Semiconductor to extend the useful life of 68K-series microprocessors for the military, aerospace, commercial, and industrial markets. e2v will wafer bank die based on advised customer requirements to ensure the continued supply of the devices following the discontinuance of the products by Freescale.

Programmable Logic Device (CPLD), from Santa Clara CA facility, used in high reliability aircraft requirements, and supplied in support of long term programs

Wafer storage facility in Santa Clara CA

Once Freescale ceases production of the 68020, 68882, and 68C000 processors, e2v’s portfolio of high-reliability grade products will be extended with commercial-grade versions in both plastic and ceramic packages. Based on up front forecast requirements, the Freescale products will remain available from e2v for the next 10 years, or longer. In fact, Freescale has licensed the company to deliver high-reliability versions of its products for more than 25 years.

The Freescale licence arrangement means that e2v will build and sell its own products, from the 68K family to high-performance Power Architecture devices, by sourcing commercial wafers and devices from Freescale and then repackaging, screening, characterizing, and testing at extended temperatures for military and aerospace requirements.

In April, e2v aerospace and defense also released re-engineered versions of the QP Semi QP741 and QP747 operational amplifiers, manufactured on a bipolar process to serve as drop-in replacements for the National/Fairchild LM741 used in key military/aerospace applications. (Market forecasts indicate that inventories of these military grade devices will be depleted in the near term.) Essentially, the company is extending its product range for a wider set of applications, where system redesign is complex and expensive.

But this type of activity is only part of the story

The long service life of military systems has proved a large enough issue to prompt plans to supply parts in the far future for the F-35 Joint Strike Fighter. Such is the pace of technological change compared to the much longer process from drawing board to roll out, that many of the parts that have been integrally built into the F-35 will have already generated end-of-life notices, even before entering full service. The wider public would be surprised to know that many of the components in their Government’s military platforms are no longer in regular production before they have seen one hour of active service.

Component obsolescence is therefore a growing concern for the industries they serve, as semiconductor companies discontinue products despite the need to keep platforms running for decades after their projected lifetimes - while needing to avoid issues such as spiraling costs and counterfeit goods entering the supply chain from uncontrolled sources.

It’s also not just aerospace and defence industries that have an issue to address, it is also a factor in a range of professional industries such as nuclear plants, oil drilling, rail transportation and factory automation. In fact any where there is a need for maintenance of electronic equipment for very long periods and/or where systems re-design and re-certification costs are predominant versus the cost of acquisition of the components themselves.

A High speed Complex

So, whilst there are clearly actions being taken by e2v and other companies to prolong the availability of specific semiconductors, to manage their obsolescence. But what options does this actually offer the design engineer? How can they use this information today to ensure that in 20 years time a specific semiconductor is still available, who does he tell, what can he or she do?

Lifecycle Management
The conclusion reached by e2v is that the design engineer of today can actually do relatively little with obsolescence management predominantly a reactive process which seeks to address the

Semiconductor testing in support of both new product and lifecycle management programs

shortfalls as they arise.

So whilst semiconductor obsolescence management is an established approach, the reality of support and expertise available from many suppliers in this market space is limited to fire fighting the obsolescence problem after it has occurred, with an inefficient and unreliable ad-hoc approach, risking allowing counterfeit product to enter service. It is basically a process behind its time.

e2v therefore decided to implement a new approach to the design, manufacture and through life support of aerospace, defence and long lifecycle commercial systems; in other words, to prepare for and mitigate against, the effects of component obsolescence as part of a Lifecycle Management Programme. In doing this, e2v is combining the knowledge of their teams in California and Grenoble in their Hi-rel semiconductor solutions division. Through this, they offer security of through-life supply via a new Semiconductor Lifecycle Management Programme, a process which plans for obsolescence mitigation of key semiconductor components at the start of a product or system development, rather than waiting for obsolescence to become an issue; whilst also offering assistance to existing systems in need of an obsolescence solution as, critical to managing existing platforms, is the ability of a supplier to work with OEMs and systems users to review current LTB inventory and to work to manage lifetime supply and future cost for key components.

e2v's new semiconductor lifecycle management approach offers;

- Redesign and reengineering facilities; wafer banking and lifetime continuity of supply;
- European and North-American storage, packaging, test and redesign facilities;
- Range of hi-rel semiconductor products, including hi-rel microprocessors, system interconnect and MRAM products, broadband data converters and the QP Semi IC product line;
- Secured and flexible supply chain for hi rel products, protecting against counterfeit risks
- DSCC qualified manufacturer listing.

This is the point at which the design engineer can begin to see the light in the process. Instead of designing to the best specification today and revisiting the obsolescence issues in 10 or 20 years time, the design team can work with e2v from day 1 to identify the critical semiconductors and to plan for their extended availability. It's a simple answer, but it needs a great deal of knowledge, system capacity and the equipment to store, assemble and test devices and if necessary to redesign. It is this that has been lacking from most suppliers in this market place because they haven't been asked to deliver this level of service.

So, whilst obsolescence management for high reliability systems is a clear and present issue for design engineers, there is a future option to calm the nerves and secure the operational capacity for as long as you want in e2v's semiconductor lifecycle management program.

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e2v
www.e2v.com

OPTIMIZED INDUSTRIAL SYSTEM PSUs

ACCURATE PRIMARY-SIDE-SENSING CONTROLLER

By Graham Proud

The universal drive to reduce power consumption that Energy Star and similar initiatives have so successfully promoted within consumer-level equipment is starting to take a real hold within industrial systems, and embedded controllers and their peripherals in particular.

Applications as diverse as fire alarms, process controls, and building automation systems very often operate on low duty cycles that potentially waste significant amounts of power while they await the next cycle of computation and communications activities. As a result, designers are under pressure to develop systems that intelligently power down whenever it is practical to do so, and run as efficiently as possible under the expected set of active-mode conditions. These considerations demand power supplies that offer very low standby power consumption together with the ability to quickly return to full output power while maintaining accurate regulation.

Naturally, any power supply solution must also offer a raft of complementary benefits —such as excellent electrical performance, robust fault protection, and minimal EMC issues — at the lowest cost that is consistent with reliable design.

CamSemi's recently-introduced C2163 is a universal-input, primary-side-sensing control IC that meets these criteria while offering a range of output voltages at power levels from about 8W to 18W to suit a wide variety of embedded applications. An evolution of the C2161/62 family that suits applications of up to 8W, the C2163 substitutes an output stage that is tailored for driving the gate of a

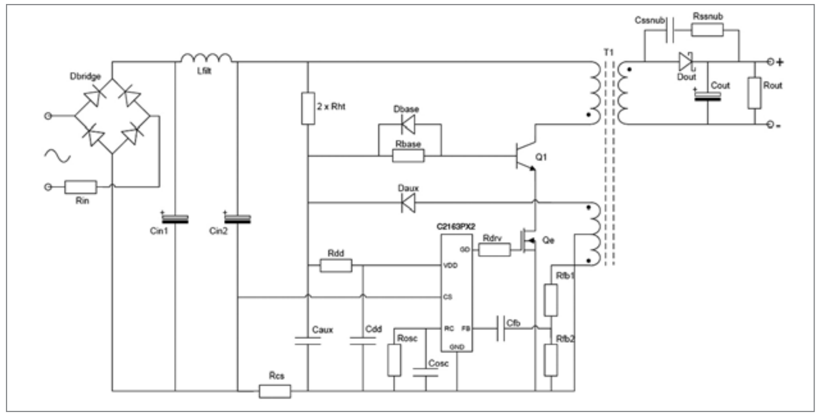

Figure 1: Basic circuit for 12W universal-input supply using the C2163

MOSFET in place of the bipolar-transistor emitter driver that appears in the original devices. This conceptually simple change allows the new six-pin SOT-23 packaged device to control substantially more power at minimal additional component count and cost while retaining all of the benefits that the original parts deliver—see Figure 1.

Operating principles

The C2163's operating principles are easily understood by considering figure 1. The general circuit arrangement echoes a conventional flyback converter that includes an auxiliary power winding to supply the controller chip and an additional winding that provides a feedback sense voltage. All power conversion occurs in discontinuous conduction mode, with the C2163 varying its switching frequency and on-time in response to load demands. The device switches the main primary winding via Q1 and Qe, where Q1 is a high-voltage bipolar power transistor (700V blocking for universal-input designs) and Qe is a low-voltage logic-level MOSFET. This cascode-connected pairing is cheaper and typically more efficient than a single high-voltage MOSFET, and it benefits from quasi-resonant switching that turns the devices on when feedback detects that the voltage across primary switch Q1 is at its minimum. Together with a degree of natural frequency jitter that spreads emissions, this "soft" switching technique eases EMI concerns to minimise the need for conducted-emissions filtering.

At power-on, current flows from the high-voltage dc input rail via the high-tension resistors Rht to supply the C2163, which enters its initialisation mode. The controller then issues several clock cycles that switch the main primary winding via Q1/Qe. This induces a potential in the auxiliary winding and operating current starts to flow via rectifier Daux. An internal shunt voltage regulator stabilises the chip's supply and the device enters run mode, with feedback being applied via scaling resistors Rfb1 and Rfb2 and coupling capacitor Cfb. The network Rosc and Cosc sets the maximum oscillation frequency, which lies between 40kHz and 66kHz at full load.

The value of Cosc also determines the C2163's integral cable compensation level that automatically allows for a variety of PSU to load cable, track, or output filter inductor resistances, with a 1% minimum being set by design. Resistor Rcs sets the range of pulse-by-pulse current control and the nominal overcurrent point. Inspection reveals that the voltage developed at the chip's CS current-sense pin is negative with respect to chip ground, which is intentional if unusual.

The output range that this basic circuit offers, spans voltage levels from 3 – 24VDC and 0.5 – 5A at power levels of up to about 18W. It betters the operating efficiency requirements of Energy Star EPS 2.0 — and its recent embodiment within IEMP Level V — with at least 2% margin and has a no-load power level below 100mW, which is a factor of three times lower than this benchmark specification requires. Importantly, a few minor circuit modifications can improve upon output power levels and drive down no-load power consumption to make the topology's application potential significantly more flexible, enabling cost reductions by amortizing design effort and rationalizing inventory holdings.

Smart sensing improves performance, lowers cost

This implementation of a flyback topology embodies multiple features that help optimise its performance while minimising build cost. For instance, a voltage reference with optocoupler feedback is traditionally necessary to meet the 5% or better regulation that commodity ICs require; without this correction, a typical primary-side-sensing controller exhibits considerable load-current dependency and may manage only ±10 to 15% regulation accuracy.

By contrast, the C2163 easily betters ±5% using a proprietary mixed-signal technique that allows the chip to precisely determine the amount of energy that is necessary to maintain regulation over the circuit's operational range (in practice, ±2% is achievable given minimal load-resistance compensation). The chip is also capable of maintaining ±7% current regulation if the application requires constant-current mode operation. This feature can also be used as a load current limit for constant voltage applications, protecting the PSU and load under fault conditions. Significantly for many industrial applications, the circuit topology is highly resistant to single-fault conditions and will protect the load by entering "hiccup" mode if the chip senses inappropriate external conditions. This action limits output voltage and current in the event of a single component failure.

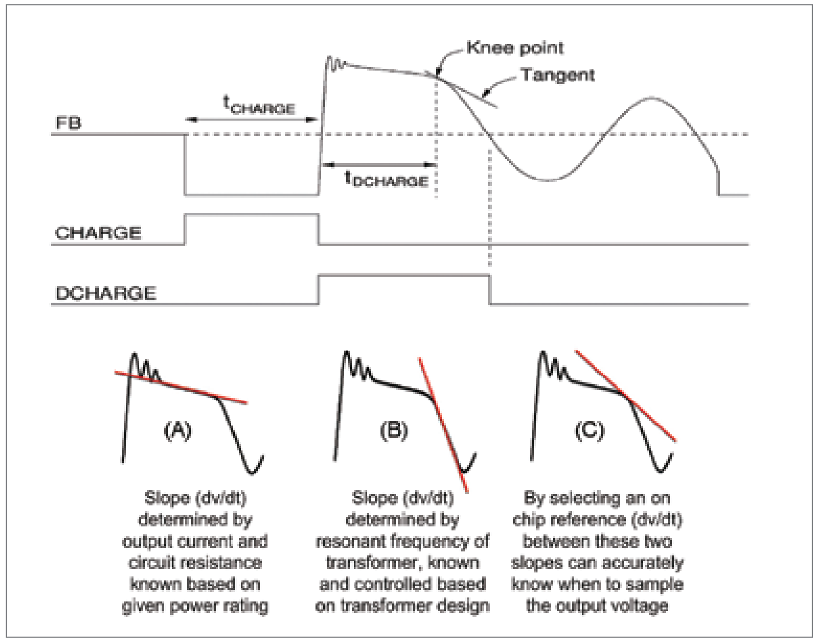
Knee point
Tangent
FB
t_{CHARGE}
$t_{DCHARGE}$
CHARGE
DCHARGE
(A)
(B)
(C)
Slope (dv/dt) determined by output current and circuit resistance known based on given power rating
Slope (dv/dt) determined by resonant frequency of transformer, known and controlled based on transformer design
By selecting an on chip reference (dv/dt) between these two slopes can accurately know when to sample the output voltage

Figure 2: Accurately determining the discharge waveform's knee point vastly improves regulation accuracy.

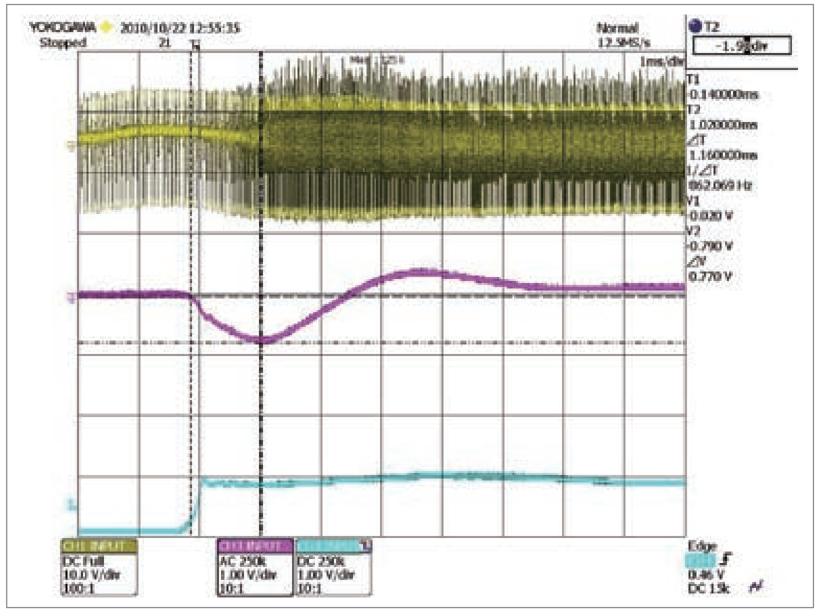

Figure 3: Recovery from a 5% to 100% load step is fast and well controlled.

The key to the C2163's regulation performance lies with the controller's ability to examine the tangent of the slope to find the knee point during the energy transfer phase, as figure 2 shows. At the knee point the secondary winding current has fallen to zero, so resistive volt drop is also zero, allowing accurate voltage sampling. The circuit's output current and circuit resistance are known by design and set the initial dV/dT slope, as in (A). Similarly, the second slope (B) is known as a function of the transformer's resonant frequency, which is again fixed by design. An on-chip reference dV/dT slope (C) then makes it possible to assess precisely when to sample the output voltage.

The ac coupling that Cfb provides allows the chip to sample the entire waveform, rather than just finding the knee point and zero-crossing points. This allows the chip to implement mains under-voltage lockout, mains over-voltage protection, and to protect the power transistor during de-saturation. Other refinements include leading-edge suppression to quash the transient that appears in the current-sense waveform at the start of the charge phase that may otherwise corrupt the chip's primary current measurement.

Lowering no-load power consumption

Dispensing with the need for

optocoupler-style feedback or linear post regulators not only saves space and cost, but also improves reliability while reducing power consumption that is especially significant for no-load measurement conditions. Clearly, industrial applications are unlikely to reduce standby current consumption to no-load levels, yet the no-load condition remains a useful benchmark for power-supply designers. In particular, the ability of a controller to recover from a no-load to full load current step is an extreme test of the circuit's dynamics, and designers can expect significantly better performance when switching from light standby-level loads to normal operating currents.

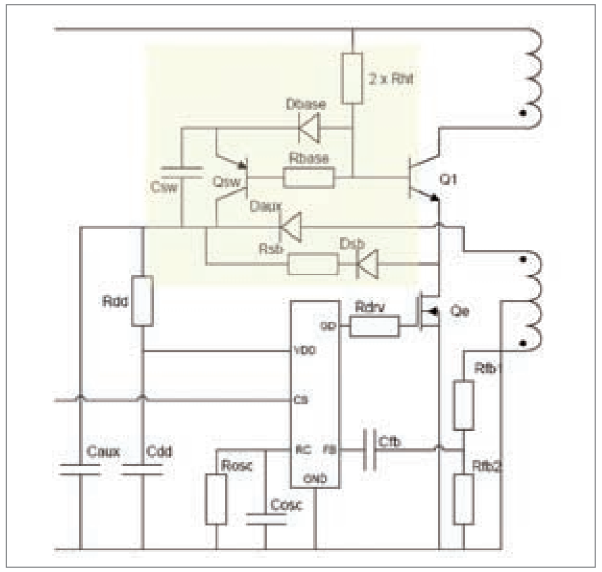

Figure 4: A few additional components can almost half the C2163's no-load power consumption.

The basic circuit in figure 1 achieves a no-load metric of <100mW by minimising the PWM waveform's on time and frequency during light load conditions, but primary-side sensing makes it necessary to pulse the output periodically in order to acquire feedback information. There is inevitably a balance to strike between the frequency and duration of these "radar echo" pulses, the speed of response to an instantaneous rise in output current demand, and power consumption. The tangent detection technique contributes here too as it allows the controller to minimise the turn-on period during unloaded operation.

For application designers, response to a low power to normal load current step becomes a function of the resistance of the output interconnection system, the amount of hold-up capacitance present on the output, and the recovery characteristics of the controller's internal loop. This last term depends upon the C2163's minimum no-load frequency, which is set by components within the chip's power supply network — the controller has no intrinsic minimum operating frequency.

Figure 3 shows a representative 50mA to 1A load recovery sequence where the blue trace is the load step, the yellow trace is the controller's switching waveform, and the purple trace is the output rail. These plots are from a 12V 1A universal-input design.

A few additional components can reduce the <100mW no-load power consumption that figure 1 achieves to typically 50 – 60mW, as the "super-bootstrap" circuit (patent pending) in figure 4 outlines. Here, the value of Rht is about ten times that found in figure 1, but the current that it provides to Q1's base is amplified with the resulting emitter current charging Caux and Cdd via Dsb and Rsb. This technique significantly reduces the static power dissipation of Rht and hence no-load power consumption. Once the circuit commences switching, the voltage level on Caux due to the charge from the auxiliary winding keeps Dsb reverse biased and prevents any further Rht-induced Q1 current flow to Caux.

Output power considerations

Assuming appropriate support components, the circuit's maximum power output primarily depends on the amount of current that Q1/Qe can handle. In practice, this holds true up to about 18W as a result of the C2163's operating characteristics. For levels of up to about 12W that involve peak switching currents of some 1.5A, the FJE3303 is preferred for Q1 while Qe can be virtually any 20V or better rated MOSFET that has logic-level drive compatibility and RDSon of 0.5Ω or less. As output power levels rise to 30W, the power switches must handle peak currents of around 4A and an RDSon value of around 0.070Ω becomes necessary to minimise losses. The recommended bipolar transistor is now an MJE13005G and designers need to ensure that voltages around the part do not exceed its reverse-bias safe-area-of-operation envelope. This consideration typically demands a simple snubber network across the transformer's primary winding.

As every power-supply designer knows, meeting EMC requirements often requires multiple iterations of circuit layout and filter-component selection. Following conventional practice, keeping layout tight around the C2163 minimizes loops that contribute towards radiated emissions while the chip's soft-switching and frequency jitter particularly helps to lower conducted emissions and reduce the values of filter-network components. As always, filter-circuit selection depends on output power level, with a single inductor Lfilt of 330µH between Cin1 and Cin2 of equal 15µF values being the starting point for the 12W design in figure 1.

Other components that contribute to constraining EMI include the MOSFET's gate-drive resistor Rdrv and the output-rectifier snubber network, Cssnub and Rssnub. Transformer construction is important too, with the C2163 allowing several possibilities to achieve the best balance between ease-of-construction and electrical performance. To assist designers, CamSemi offers extensive application support that includes reference designs and evaluation boards for 12W and 18W supplies.

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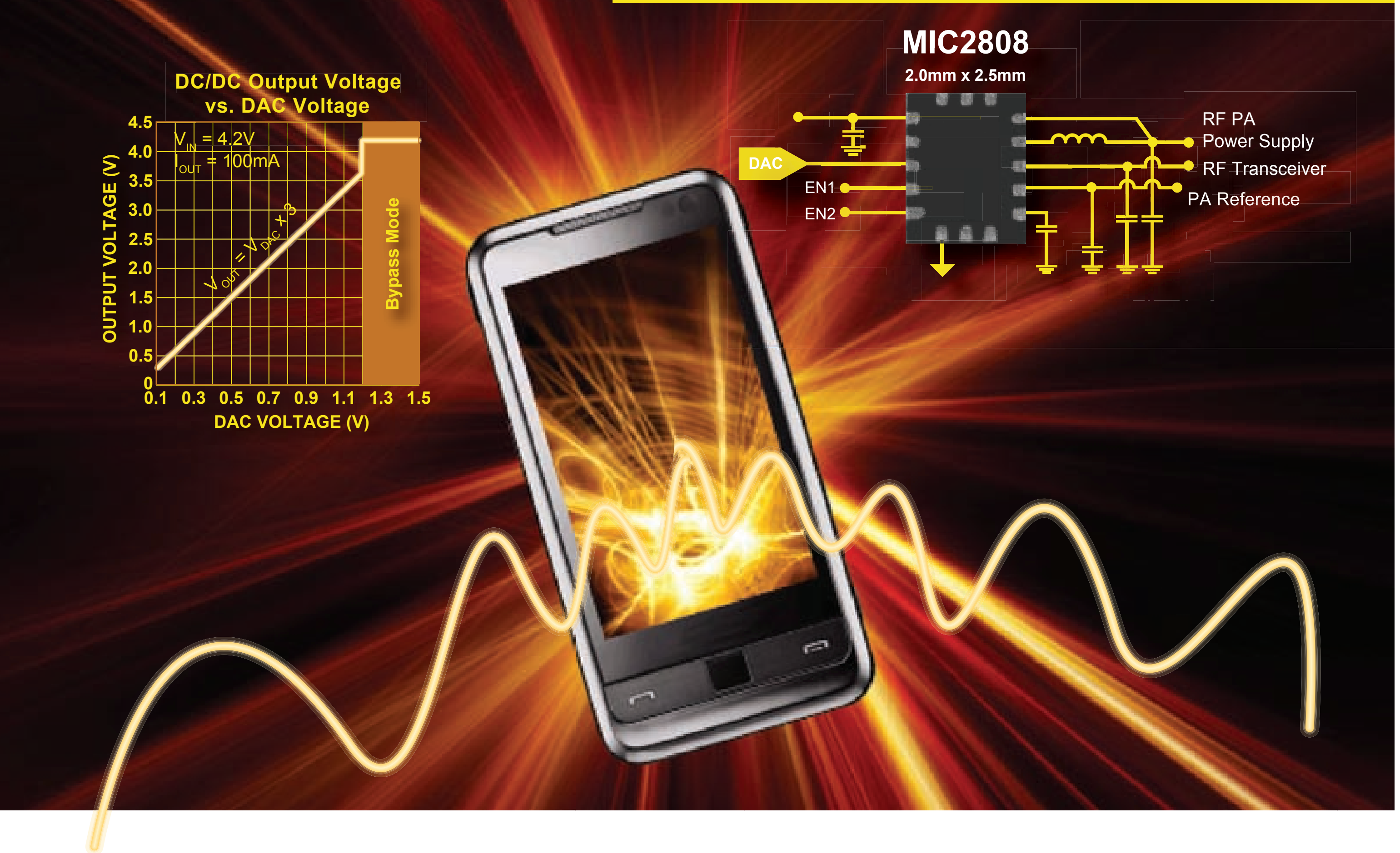
DC/DC Output Voltage
vs. DAC Voltage
OUTPUT VOLTAGE (V)
DAC VOLTAGE (V)
V_{IN} = 4.2V
I_{OUT} = 100mA
$V_{OUT} = V_{DAC} \times 3$
Bypass Mode
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
0.1
0.3
0.5
0.7
0.9
1.1
1.3
1.5
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- WiFi modules
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SPECIAL REPORT:
POWERING COMMUNICATIONS

PSD NORTH AMERICA
Power Systems Design: Empowering Global Innovation

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COMMUNICATIONS POWER SOLUTIONS

Power management improves operating time in handsets

By Wayne Seto

What is more annoying? Running out of battery or constantly needing to recharge it? With the proliferation of cellular mobile handsets, especially smartphones in the world today where people are connected 24 hours a day, 7 days a week, consumers can't seem to get enough of the voice calls, emails, text messages and surfing the web.

All of this activity on our mobile handsets consumes battery life and with this constant use, phones can go to that dreaded one bar on the battery power indicator very quickly. What can be done to prolong the usage time for these handsets so that we can use the smartphone longer? And of course, using a bigger battery is not an option as users demand smaller, thinner and sleeker handsets. Design engineers are constantly looking for ways to improve power management performance and focus on three areas where these interventions will have the most impact. The three areas outside of the baseband processor and RF transceiver that consume the most power in a handset are the power amplifiers (PAs), the display and the applications/graphics processor. Why are these three areas the focus?

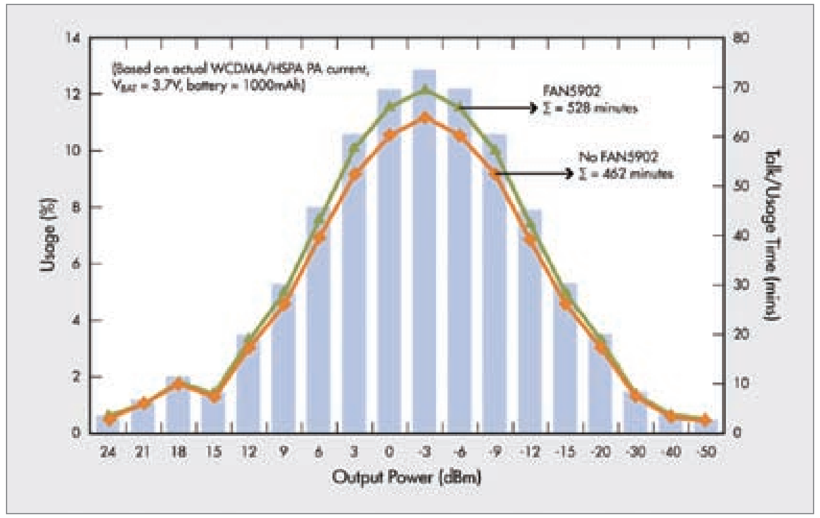
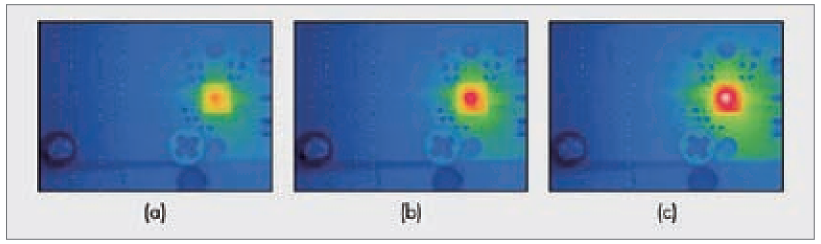


Figure 1: Talk time analysis of a 3G PA with and without FAN5902 under WCDMA signal modulation and 1000mAh Li-Ion battery. The power distribution function is DG09 and can be found in GSMA's white paper "Battery Life Measurement Technique, v4.7".

Figure 2: Thermal profile of 3G PA at POUT = 28dBm: (a) with FAN5902 at VPA = 2.97V, (b) PA only at VBAT = 3.70V and (c) PA only during battery charging at VBAT = 4.20V.



Nowadays, people talk and surf the Internet all at the same time and when you do this the display is usually on as well, plus the PA needs to be on constantly to transmit voice calls and data to the base station and finally the applications processor is running so that you can bring up the website to watch a video or enable other applications.

The PAs for 3G networks consume a lot of power especially when the reception is poor since it needs a higher output power to connect to the base station while maintaining linearity requirements to ensure 3G signal fidelity. A 3G PA will consume current based on the output power level and the higher it is, the more current will be drawn from the battery. Transmitting data requires higher output power and thus, consumes more current. There are two novel techniques used to reduce PA current consumption: DC-DC converters and envelope tracking. The use of DC-DC converters is increasingly being used in smartphones and it operates by stepping down the supply voltage for the 3G PA to a level where it will meet the required output power level but minimize the amount of current consumed. Implementing such a solution provides a two-fold benefit – longer talk/data usage time and lower heat dissipation. The FAN5902, an 800mA, 6MHz step-down DC-DC converter with a bypass mode, from Fairchild Semiconductor was designed specifically for 3G PAs to lower power consumption and extend the connection time performance.

The FAN5902 works in conjunction with both the baseband processor and 3G PA to lower the current consumption. The baseband processor will set the output power level of the PA based on information it receives from the base station and then translates it to a supply voltage for the FAN5902 to output to the PA. By dynamically adjusting the PA's supply voltage and therefore the current, the FAN5902 can extend the talk and data usage times for mobile handsets by at least 15%. See Figure 1 which illustrates the performance under DG09 power distribution function between a standalone 3G PA and a 3G PA enabled by FAN5902. Table 1 summarizes the performance under various conditions.

In addition to extending talk times, a DC-DC converter-enabled solution also helps lower the heat dissipation so that handsets or USB dongles/data cards won't get as hot. Figure 2 shows the thermal profile of 3G PA with FAN5902 and the other

Type	Parameter	FAN5902 (minutes)	No FAN5902 (minutes)	Improvement	
				Abs. Minutes	Percentage
Voice	Tx Time using 3 PA Power Modes	528	462	65	14%
	Tx Time with PA in High Power Mode	495	291	205	70%
Data	Tx Time using 3 PA Power Modes	365	280	85	30%
	Tx Time with PA in High Power Mode	361	224	137	61%

Table 1: Performance under various conditions

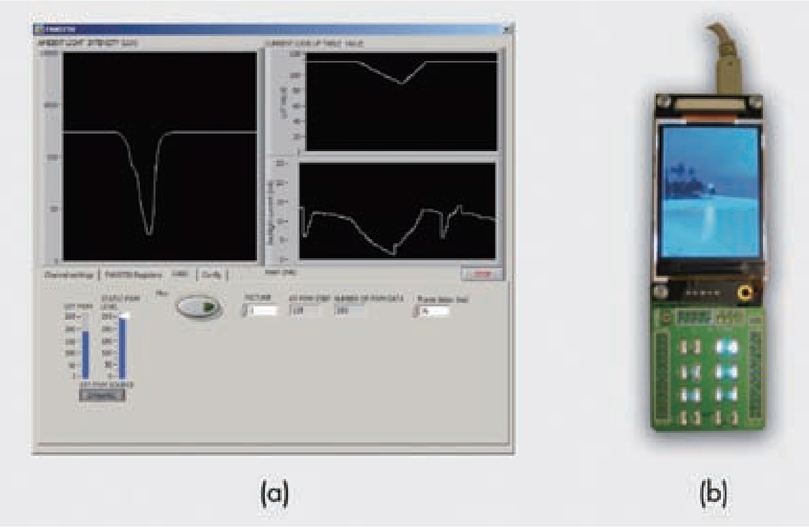


Figure 3: (a) Display that does not use ALC and DBC, (b) Display with ALC and DBC.

without it.

The display is the second major consumer of power after the PA and since it is on whether you are looking up contact information, surfing the web, reading emails or watching mobile TV/YouTube ® videos. The predominant display technology current is TFT LCD displays and it requires white LEDs to backlight it. Since the trend is for larger LCD displays, it means that more white LEDs are required to effectively backlight the display which, in turn, means more current is needed to power the LEDs as well as the display itself. In the high-end feature handsets and smartphones, dynamic backlight control (DBC) and auto luminous control (ALC) are used together to not only minimize current consumption but also enhance visual experience for the user. ALC requires the use of an ambient light sensor, which detects the amount of light in the environment and then sets the LED current based upon an algorithm programmed in the LED driver or applications processor. So depending upon the lighting conditions the LED current will be set low when it is dark or maximum LED current in direct sunlight. DBC is a technique that adjusts the LED current based upon the image/video content on the display such that a scene in a video with more dark content will have lower LED current vs. a brighter scene. The DBC programs the current based upon a pulse width modulation (PWM) signal from the graphics processor or LCD driver IC and is constantly changing with the video content that is being displayed. Figure 3a shows ALC and DBC in operation with a screen capture of software program used by Fairchild to show the ambient light level (left graph) and corresponding LED current. Though it cannot be illustrated properly the DBC is in action with the “blue bars” for external PWM and static PWM level will go up or down based on the image or video content. A photo of Fairchild’s evaluation kit demonstrating ALC and DBC is shown in Figure 3b.

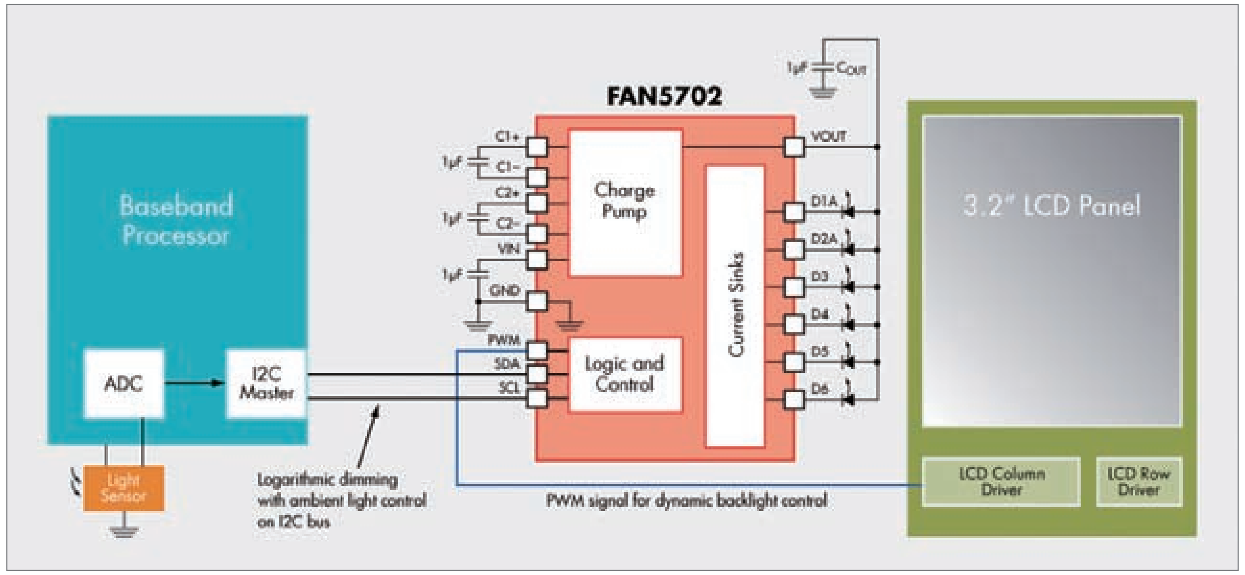


Figure 4: System block diagram of FAN5702 with ALC and DBC implemented.

Fairchild’s FAN5702, 180mA charge pump LED driver with I2C interface, can be configured to enable both ALC and DBC. The ambient light sensor is connected to the applications or baseband processor, which will take the input and determine the appropriate LED current level based on the algorithm for external lighting conditions. This data is then sent via the I2C interface to the FAN5702 and set the LED current. The PWM/EN pin of FAN5702 is programmed for PWM operation and it is, in turn, connected to the LCD driver IC, which will send the PWM signal to FAN5702 based upon the image/video content on the display. Figure 4 is a system block diagram of FAN5702 using both ALC and DBC. Adopting ALC and DBC for displays in mobile handsets will help realize up to 50% savings in power consumption.

The third area where there is significant power consumption is the applications or graphics processor; and if the display is on then this chipset will be running full tilt. However, this processor does not always run at full power all the time. To take advantage of instances when the chipset is running at lower power levels is to use a technique called dynamic voltage scaling (DVS). This is an ideal solution in mobile handsets and other portable electronics because the supply voltage can be scaled down to a lower core voltage and allows the chipset to operate at reduced clock frequency and this helps to achieve lower current consumption.

This is best illustrated by the following equation:

$$P \propto f V^2$$

Where: The power (P) is proportional to the product of the clock frequency (f) and the square of the core voltage (V). Therefore, the faster the processor clock frequency the higher the power consumption. But when the core voltage is lowered, the power consumption can be decreased quadratically.

An applications processor can be powered by FAN5365, a 6MHz, 800mA/1A step-down DC-DC converter with I2C interface, for optimum power conservation. The I2C interface is used to dynamically program the voltage between 0.75V to 1.975V in 12.5mV steps to meet the processing power requirements of the chipset. The FAN5365 would supply a core voltage of 1.2V to the applications processor for maximum processing power when watching a video on a website but once it is over it will drop down to 0.8V for lower level operation.

There are a variety of ways to improve overall power management performance of mobile handsets and in particular smartphones with both simple and complex techniques. By implementing one or all three of these power management solutions for the PA, display and processor cores into mobile handsets, designers can provide significant power savings to prolong the operating time. All of this is done in mind to keep the user happy because all they care about is not having the handset lose battery power at a critical time and that they don’t have to recharge this handset frequently.

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COMMS CONTINUITY

Fast & efficient power management solutions maximize reliability

By Shyam Chandra

The explosion in data traffic and the introduction of “Smart Phones” such as the Apple iPhone are fuelling the need for the rapid expansion of communications networks, not only at the edge but also in the backhaul networks.

Communication equipment manufacturers and suppliers must meet stringent contractual demands by the network operators for such things as Quality of Service (QOS) and Class of Service (COS) requirements. Failure to do so may lead to penalty clauses being invoked, which may mean heavy fines for the supplier. The equipment uptime requirement of 99.999%, also known as the five nines, is typically quoted for the reliability of the service.

Complex designs

Communications design engineers are increasingly using complex devices such as ASICs, ASSPs, communications processors and FPGAs to provide the right solutions in the network and switching fabric. These devices will have very different power requirements from each other, not only in voltages but in the sequencing of those voltages. Additionally, in the case of rack mounted equipment, the actual PCB can be of a substantial physical size and may contain all of the above devices. It is therefore essential that, in order to ensure the correct operation of the design, very careful thought must be given to the provisioning of power on the board. These complex devices require multiple board-mounted power supplies that need to be turned on and off in a specific sequence, monitored for faults and trimmed for voltage accuracy. In addition, the input power to the board often requires redundant power management and, in the case of plug-in boards, hot-swap functionality.

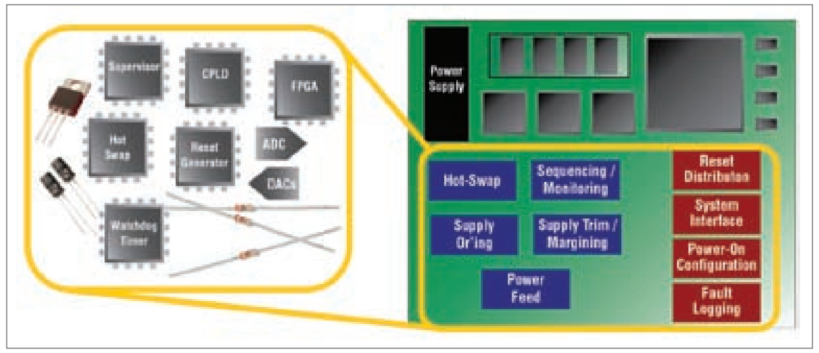

Figure 1: Traditional approach

All the functions that control various power rails comprise the need for power management.

After all supplies are turned on, the system requires digital support functions such as reset distribution, start-up configuration control for FPGAs and ASSPs, watchdog timers and a system bus interface for a microcontroller. These digital support functions require digital management. Power and digital management together are often referred to as board or platform management.

Traditional approach

The traditional approach to power management has been to use many single function ICs and discrete components in order to provide the solution; however, this approach has a number of disadvantages. The large number of devices results in a high bill of materials as well as increased board size. This has a direct effect on board reliability and may also mean that all the signals are not monitored accurately. If the board requires a re-spin of the design there could be a corresponding change in the power requirements. This approach is shown in Figure 1. The blue coloured blocks show the analogue functions and the red show the digital functions for power monitoring. The black or grey components represent the payload, or primary, function being implemented.

The programmable solution

In order to overcome the disadvantages to the traditional approach, Lattice has now introduced its third generation family of mixed signal devices, namely the Platform Manager family. These programmable devices significantly simplify board management design. The Lattice Platform Manager integrates board power management (hot-swap, sequencing, monitoring, reset generation, trimming and margining) and digital board management functions (reset tree, non-volatile error logging, glue logic, board digital signal monitoring and control, system bus interface, etc.) into a single chip. The block diagram is shown in Figure 2.

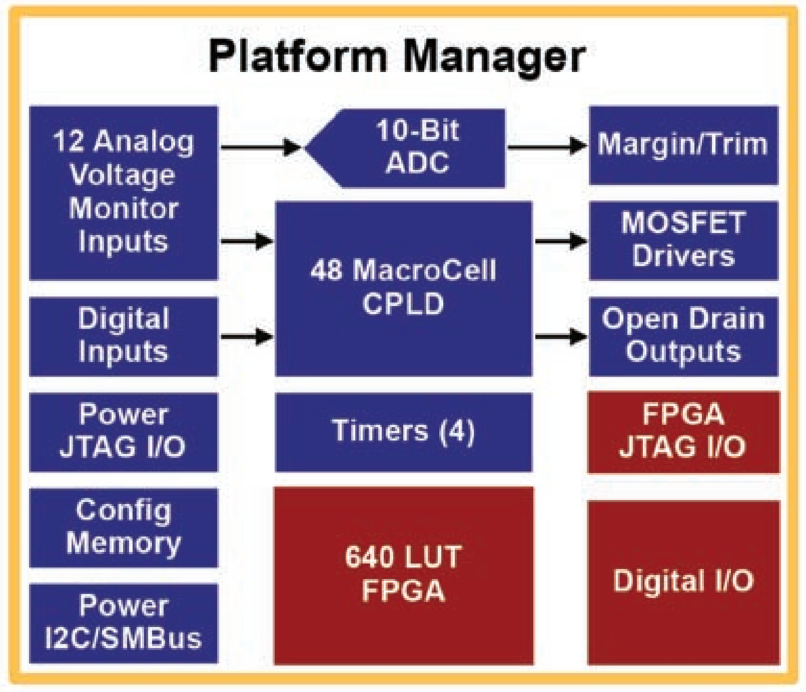

Figure 2: Block diagram

The Platform Manager can monitor up to twelve power supply test points through independent analog input channels. These input channels can be monitored through differential inputs in order to support ground sensing. Each of the analog input channels is monitored through two independently programmable comparators to support both high/low and in-bounds/out-of-bounds (window-compare) monitor functions. Up to six general purpose 5V tolerant digital inputs are provided for miscellaneous functions. The device also contains a 48-macrocell CPLD and a 640 LUT FPGA.

The status of all the comparators on the analog input channels as well as the general purpose digital inputs are fed to the inputs of the CPLD array, whose outputs then control all the digital outputs (open-drain as well as HVOUT). The FPGA section of the Platform Manger is optimized to meet the digital board management requirements and uses distributed memories for flexible and efficient

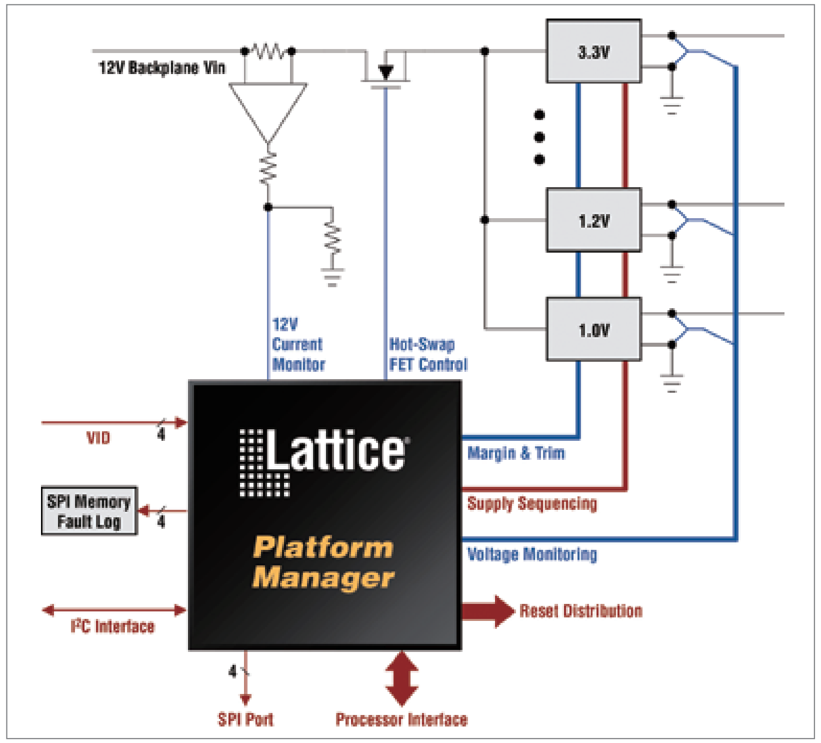

Figure 3: Typical application of Platform Manager

logic implementation. The instant-on capability enables the device to integrate control functions that are required as soon as power is applied to the board.

Instant-on

In complex systems it is essential that power be applied to the individual devices according to their precise specifications and in the correct order. If one relied on a microprocessor for this function the system would have to wait until the processor had gone through its boot sequence before the rest of the system could be powered. This could lead to a number of problems such as the delay in start up, and signals being applied to other devices in an uncontrolled manner. Platform Manager overcomes this potential problem by using its non-volatile memory for the configuration.

Backplane management and hot swap

In communications systems where rack and shelf mounted boards are common, plug in boards communicate with a shelf manager to provide information about the board configuration. The shelf manager checks to determine that the correct card has been inserted. Only after receiving the turn on command from the shelf manager is the payload turned on.

Reset tree

The Platform manager also provides an efficient mechanism for reset distribution. In many cases the individual devices on a board must be reset in a controlled manner. Various resets such as PLL Locked, Memory Controller ready, FPGA-done etc may need to be synchronised to the system clock. In other designs Reset sequencing is needed to minimise peak current consumption for a reliable start up.

Typical application

A typical application of Platform Manager is shown in Figure 3. In this example, the Platform Manager is able to detect faults across 12 supplies. These are represented by the black dots. It can trim up to 8 supplies; this is a key function and will be described more fully later. The device is also able to capture and log information to the non-volatile SPI memory. The voltage monitoring function is shown connected to the differential outputs of the various power outputs.

VID control

Certain ASIC and CPU devices that have been fabricated using 45nm or below sometimes require different core voltages in order to meet their datasheet performance. The required core voltage is encoded and can be read by the board management logic as its Voltage ID, or VID. In order to meet these sometimes stringent demands the the use of precise and expensive power supplies is typically required. By using the VID information, the Power Manager can use the Margin and Trim circuits to precisely control the various power voltages and consequently a less costly DC to DC converter can be utilized.

Design and evaluation

In order to facilitate and accelerate the design cycle, Lattice provides a number of tools and options. The family is supported by PAC-Designer 6.0 software and the starter version of ispLever design software tools. These are free tools that may be downloaded from the Lattice website. Also available are four free reference designs and three free IP cores that implement common functions, such as fault logging into Non-volatile Memory, Closed loop Margining and interface to I2C or SPI bus masters. Additionally, a low cost Platform Manager development kit containing an evaluation board complete with demonstration code and documentation is available for purchase. This board allows users to see known good hardware in about five minutes and to recompile the provided source code in order to get to a known good starting point in thirty minutes. This is an invaluable way for engineers to familiarize themselves with the capabilities of the device before beginning their own design in earnest.

Summary

The Platform Manager is a flexible, programmable device that can be customized to solve many of the problems engineers face in providing the power and control functions required in modern complex designs. By integrating many of these functions into a single device, the Platform Manager can reduce the overall system cost and, because of the reduced component count, can significantly improve system reliability.

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COMPACT ISOLATED DC-DC CONVERTER

Power-System-in-Package (PSiP) sets vital new benchmarks

By Christopher R. Swartz

System designers have struggled to determine the type of distributed power system to best meet the needs of the system while still retaining high efficiency, reliability, low cost and most of all, flexibility to adapt to the fast changing requirements, its size and power density make it an ideal solution for the challenging requirements of end-systems such as advanced telecom and wireless infrastructure, networking & communications, Power-over-Ethernet applications and high speed server platforms.

Distributed Power Architecture (DPA), for example, supplies each output load voltage by an isolated DC-DC converter appropriately sized for the load current required. This method usually produces the higher overall efficiency — in comparison with Intermediate Bus Architecture (IBA) — due to the lower number of "serial" conversion stages and lower distribution losses of the input bus, but it usually results in higher cost and larger board area requirement. IBA usually reduces the board area and cost in comparison to DPA. An isolated bus converter (IBC) decreases the high voltage down to a level that is the aggregate average sweet spot for the narrow range non isolated point-of-load converters (NiPOL) in terms of duty cycle and efficiency. Each NiPOL then operates off of this bus voltage and produces a regulated output voltage for each load.

A new high-density isolated DC-DC converter combines the advantages of both DPA and IBA topologies by delivering 60W of isolated output power in half the size of existing solutions, setting a new standard for power density by delivering over 400W/in3. It combines isolation, voltage transformation, and output regulation into a high density, surface-mount Power-System-in-Package (PSiP) platform with a tiny footprint (0.57 in2) and very low profile (0.26 inch), making it ideal for applications where board space, airflow, and height dimensions are critical.

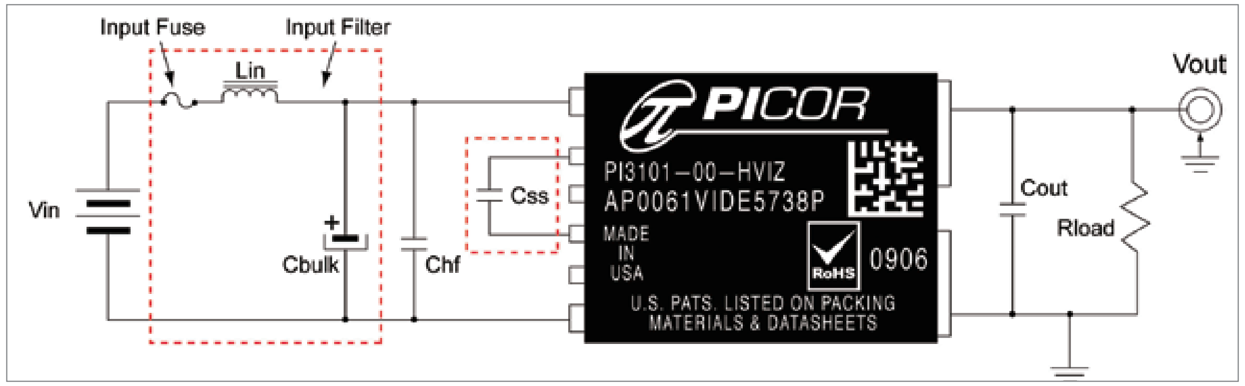

Figure 1: PI3101 complete power system

The new converter operates over a wide input voltage range of 36Vdc to 75Vdc while providing a regulated 3.3V output at up to 18A output current. It can withstand input voltage transients of up to 100V for 100ms and provides 2250V input-to-output isolation.

Looking more like an integrated circuit than a power supply, the converter, designated PI3101, owes its existence to a number of innovative technical concepts. Firstly, its patented Double-Clamped Zero-Voltage Switched (DCZVS) buck-boost topology. State-of-the-art planar magnetics are employed, which allow for extremely low leakage inductance and superior power transfer from primary to secondary. Further, proprietary control with advanced silicon integration, in conjunction with proprietary gate drive techniques, allow for precise timing and management of the high-performance power conversion stage. Together with the magnetic design, the control circuitry makes switching frequency operation in excess of 1MHz a reality. The high-density, surface-mount PSiP packaging facilitates PCB layout optimization for high switching frequency, offers the designer the opportunity to employ a variety of cooling techniques, and protects the circuit components against mechanical and ambient factors, thus improving reliability. Proprietary sampled feedback control eliminates optical isolation and external feedback-loop compensation requirements. Finally, proprietary, high performance MOSFET technology with best-in-class figure of merit attributes, contributes to high efficiency.

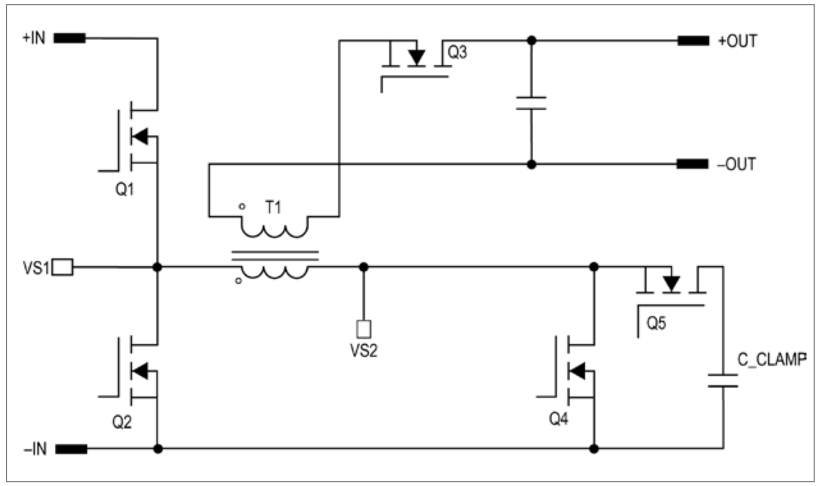

Figure 2: DCZVS topology diagram (US patent pending)

The PI3101 contains all of the necessary circuitry for a completely isolated and regulated power supply. It can be trimmed +/-10% using a simple resistor connecting the TRIM/SS pin either to the ENABLE pin, for trimming higher, or to the input –IN pin for trimming lower. For modified start up, a soft-start capacitor can be added externally. The PI3101 can be turned off and on remotely by toggling the ENABLE pin. This

Table 1: P13101 comparison with isolated power converters

Parameter	Picor PI3101	Converter "X"	Converter "Y"
Size (inches)	0.87" x 0.65" x 0.265"	1.35" x 0.95" x 0.327"	1.3" x 0.9" x 0.374"
Max Output Power (Watts)	60W	50W	82.5W
Typical FL Efficiency (%)	87%	87%	90.5%
Power Density (W/in3)	400	119	189
Input Range (V)	36V-75V	36V-75V	36V -75V
Total Accuracy Line, Load, Temp (%)	+/-3%	+/-2.5%	+/-3%
Operating Junction Temp (°C)	-40/+125	-40/+100	-40/+85
Fswitch (kHz)	900kHz	350kHz	440kHz

pin also provides the user with a 5V reference. The PI3101 contains an accurate temperature monitor function, which outputs an analog voltage proportional to the internal temperature of the product on the TM pin. The TM pin also serves as a fault alarm flag indicating that there is a problem when asserted low. The PI3101 is well protected with an array of protection features. There are two current limits to protect against short circuit and overload, input over voltage and under voltage lockout with auto restart, output over voltage protection with automatic recovery and over temperature shutdown with automatic recovery.

Figure 1 shows a typical complete power supply using the PI3101 with system fuse and optional input filter and soft start capacitor components.

The heart of the PI3101 is a proprietary Double-Clamped Zero Voltage Switched power stage topology, enabling operating frequencies in excess of 1MHz. Figure 2 shows the topology diagram for the PI3101.

The PI3101 uses four primary MOSFETS and a synchronous MOSFET that together form the power delivery subsystem. Q1 and Q4 are power switches and Q2 and Q5 are clamp switches. Q3 is the synchronous MOSFET.

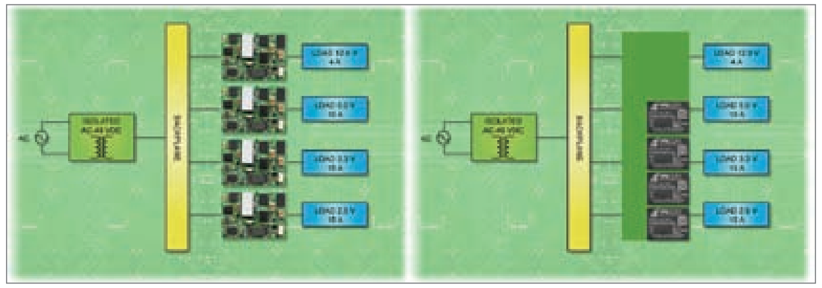

Figure 3: DPA using 4 x 1/16th bricks (left) Vs. DPA using PI3101 (right)

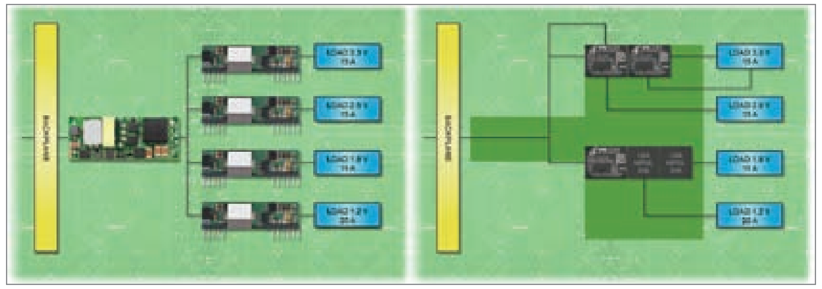

Figure 4: IBA using an isolated 1/8th brick and 4 x DOSA NiPOLs (left) vs. using PI3101

> It is useful to compare the figure of merit (FOM) of isolated power converters with respect to their relative size, power density and key performance metrics (see Table 1). Converter Y represents the best in class for the 1/16th brick form factor. Converter X represents about the mean level of performance of all converters reviewed.

It is clear that the PI3101 can be competitive when matched against converters of twice the size. The full-load efficiency is equivalent to Converter X while delivering a very significant improvement in power density. The PI3101 has better than twice the power density of the highest power 1/16th brick and nearly 3.5 times the power density of the industry average for a regulated 1/16th brick.

Consider the DPA configurations shown in Figure 3. The smallest isolated approach before the PI3101's existence would consist of four 1/16th bricks to produce the regulated output power.

Using PI310x Cool-Power family the total system size can be reduced in half. Figure 3 shows a scaled version of the actual 1/16th bricks employed on the left comparing the resulting difference in size by using the PI310x Cool-Power based solution on the right.

Similarly, the IBA solutions are compared in Figure 4. The required output power of the loads is equal to roughly 130W. If the input bus is a wide range 36-75V and a fixed bus IBA is used, the isolated converter will need to be an 1/8th brick. Each output NiPOL would be a DOSA compatible DC-DC converter.

By combining IBA with DPA using PI310x's to power the 2.5V & 3.3V loads directly and another PI310x as an IBC feeding a couple of high density NiPOLs for the 1.8V and 1.2V rails mounted vertically, an even more dramatic size reduction can be realized. The high power density of the PI310X family allows system designers the flexibility to power the ever-shrinking technology of the future.

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TELECOMMUNICATIONS SAFETY

Circuit protection using gas discharge tubes

By Matthew Williams

Telecommunications equipment must be able to survive surges and power faults as defined in the relevant standards. Survivability can be achieved by providing protection either remotely or at the terminals of the equipment, or both. In addition, or alternatively, protection can be achieved by making the equipment more robust.

When designing a circuit protection strategy, it is important to consider the complete system. To reduce cost, the capabilities of the protection scheme may be diminished, but other components must then be made more robust to compensate. In such a case, the cost of enhancing reliability of the downstream components may exceed the cost savings of a less robust protector. A good design will optimize the trade-offs.

VDSL circuit protection considerations

VDSL (very-high-speed digital subscriber line) technology facilitates the delivery of information at speeds of up to 52Mb/s. Standard VDSL deployment uses a frequency spectrum up to 12MHz, whereas VDSL2 allows for up to 30 MHz as an option.

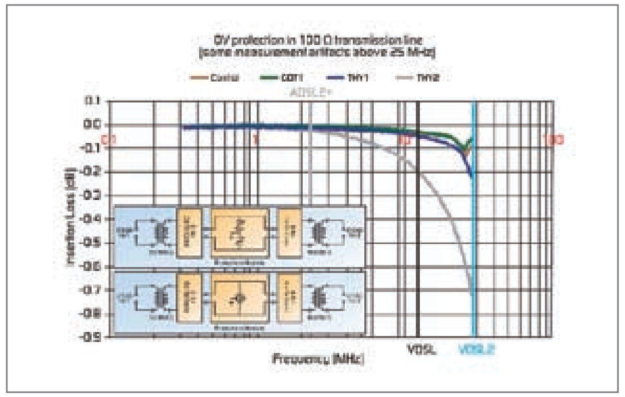

Figure 1: Test data shows the capacitance effects of various overvoltage protection configurations

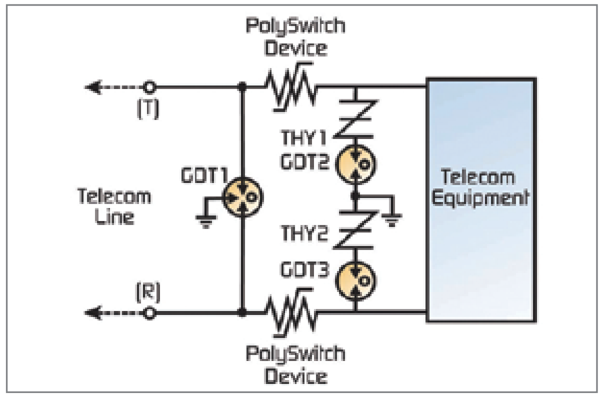

Figure 2: Coordinated circuit protection scheme helps reduce energy let-through

The capabilities of VDSL are dependent on the distance between the operator and end-customer equipment, as well as the condition of the existing copper plant and copper infrastructure outside the plant. Depending on loop conditions, VDSL is able to support varying bit rates and high bandwidth services, such as a channel of HDTV programming, over telephone copper pairs.

Since VDSL equipment connects to the copper infrastructure of the Public Switched Telephone Network (PSTN), the equipment may be exposed to overcurrent and overvoltage hazards from AC power cross, power induction, and lightning surges.

Resettable PPTC (polymeric positive temperature coefficient) overcurrent protection devices can be used in a coordinated protection scheme with overvoltage devices – such as gas discharge tubes (GDTs) and thyristor surge suppression devices – to help reduce equipment failures and warranty costs.

Reducing insertion and return loss

Because signal spectrum is increasing from 10 MHz to 30 MHz, VDSL system designers are faced with a number of new challenges. The most important issue is reducing insertion and return loss and the effect on reach and rates in high-speed applications.

The capacitance of overvoltage protection devices becomes a concern in the upper range of the VDSL frequency spectrum, as the devices used to protect the system may cause increased system insertion loss. Testing by Tyco Electronics has shown that low-capacitance thyristors and GDTs are suitable for high data rate circuits, including VDSL applications.

Figure 1 illustrates the capacitance effects on insertion loss of several overvoltage protection configurations. It shows that low capacitance GDTs (1pF) have the lowest insertion loss, with the standard 50A thyristors (15pF at 50V DC bias) and 100A microcapacitance devices (20pF at 50V DC bias) having slightly greater insertion loss.

The inset modules shown in this test diagram consist of either a 230V 3-Pole GDT or two 270V in-series thyristors, attached to two 0.3m pieces of Cat 5e twisted pair. An Agilent 8753ES Vector Network Analyzer with two North Hills' 0301BB 50:100 Ohm wide band transformers were used to make the insertion loss measurements.

The transformers were used to measure the insertion loss of the modules under 100 Ohm impedance conditions, which is

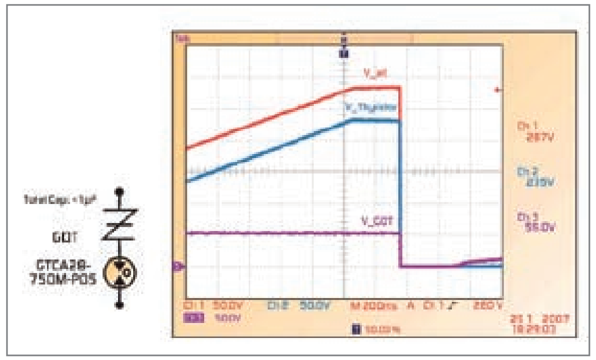

Figure 3: Test results of GDT and thyristor in series at 100V/s

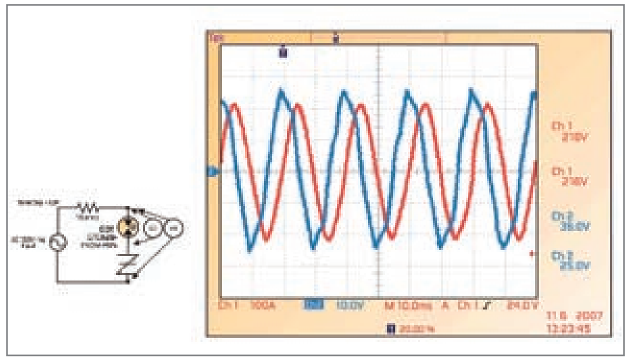

Figure 4: Test results of GDT and thyristor at 150Vrms

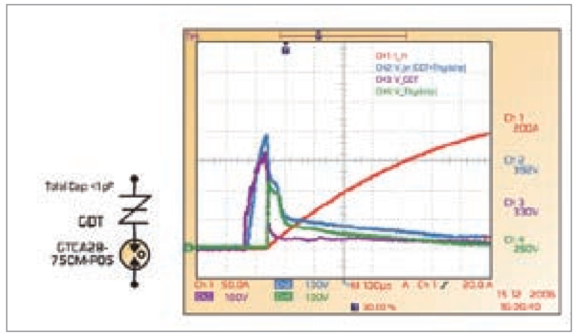

Figure 5: Test results of GDT and thyristor at 4kV level

equal to the line impedance over the VDSL frequency spectrum. Capacitance at 1MHz with no bias was measured using an HP 4195 Low Frequency Impedance Analyzer.

Implementing a low-capacitance solution for VDSL

The circuit diagram in Figure 2 shows a VDSL solution that effectively reduces capacitance and energy let-through, and optimizes the circuit protection scheme. As shown in this circuit diagram, GDT1 provides primary protection (at 350V to 1000V). The GDT2 and GDT3 devices are connected in series with the thyristors. In this scenario, the thyristor helps lower the breakdown voltage of the GDT and reduces the let-through energy in the case of a surge. The PolySwitch™ PPTC devices help coordinate the primary and secondary protection.

Figures 3, 4 and 5 show test results for this protection method and demonstrate that the GDT and thyristor combination does not break down under ringing voltage and does not clip the ringing voltage. In the oscilloscope screen shot in Figure 3, the input voltage rate is at 100V/s. The DC breakdown voltage at 287V is achieved, which is higher than the ringing voltage of 200V.

Figure 4 shows the data from a test performed with an AC voltage input at 150Vrms. Results show no clipping, indicating that the GDT and thyristor combination does not break down under the ringing voltage and clip the ringing voltage. Here, the thyristor determines the static breakdown.

In Figure 5, the same test was performed per the ITU K.20 10/700μS at 4kV level. Oscilloscope observations show the breakdown voltage of the GDT and thyristor combination at 392V. Voltages also noted are the GDT breakdown voltage of 330V, and the thyristor breakdown voltage of 250V. Here, the dynamic breakdown voltage is determined by the GDT.

Summary

GDTs are commonly used to help protect sensitive telecom equipment from damage caused by transient surge voltages that may result from lightning strikes and equipment switching operations. GDTs are placed in front of, and in parallel with, the sensitive equipment acting as a high impedance component while not influencing the signal in normal operation. Due to their low capacitance, GDTs exhibit lower insertion loss than many other overvoltage protection technologies.

Due to their fast and accurate break-over voltage, GDTs are suitable for applications such as MDF (Main Distribution Frame) modules, high data-rate telecom applications (e.g., VDSL and xDSL), and surge protection on power lines. When used in a coordinated protection scheme with PPTC devices and thyristors, they can help equipment manufacturers meet the most stringent regulatory standards.

As with any type of protection scheme, the effectiveness of a solution will depend on the individual layout, board type, specific components, and unique design considerations. Most circuit protection device manufacturers will work with OEM customers to help identify and implement the best approach.

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COMMUNICATIONS FIELD CALLS ON ANALOG DESIGNERS AND POWER SPECIALISTS

By David Morrison

As communications systems and products evolve toward higher performance and complexity, the power supplies developed to support them must grow along the same lines. Naturally, this means that power supply designers and other engineers with power electronics expertise are continually needed to tackle the latest challenging in powering communications products across a range of diverse applications.

These include wireline and optical communications equipment, networking equipment, and wireless infrastructure and handheld communications devices, just to name a few prominent areas.

These types of applications do create opportunities for engineers with power supply design expertise. Some of these opportunities are within the communications field at the equipment manufacturing companies, while others are in the power supply and semiconductor companies that develop modules and power ICs to support communications. These various types of companies have different requirements for power supply designers—different in terms of skill sets but also in terms of their levels of demand.

In the communications field, some of the larger companies have dedicated power supply design groups. However, many companies in this industry have jettisoned their power supply design teams over the years and outsourced this work. These companies still need hardware designers who can address power supply issues, but their design responsibilities tend to be broader than just power.

Meanwhile, the de-emphasis of power supply design within the communications industry places more of the burden of power design responsibility on the shoulders of the power supply and IC vendors. If this outsourcing trend sounds all too familiar, perhaps it's because it's the same one that's been occurring in information technology and other industries. And it has some of the same implications, namely that greater opportunities for power electronics engineers may exist in power supply and power semiconductor companies than in the communications OEMs.

Opportunities in the Communications Industry

A recent search of job openings at companies in the networking and RF/wireless fields revealed openings for power supply designers and others with related experience at companies such as Cisco Systems, Harris Corp., and Motorola. (To view these job descriptions, see the online version of this article.)

These job postings provide a glimpse into what roles power supply designers play within the communications OEMs and what particular skills and experiences are sought for these positions. But since these listings only provide a brief snapshot in time, I turned to two seasoned professional recruiters to see the bigger picture and trends. Both of these recruiters specialize in the placement of power supply designers and others with power electronics expertise.

Rich Cardarella, president of the staffing firm Power Technology Associates, notes that within the communications industry, there is significant demand for engineers with power supply design experience. "If you were to search one of the general jobs boards and you put in 'communications' and 'power supply design', you're going to find quite a few positions available, but I think you're going to see that they're not just power supply design. They've broadened out," said Cardarella.

"The openings you see within that industry are for hardware design engineers or analog design engineers, and [dealing with the] power supply is part of it," said Cardarella. "They're looking for someone to design the protocols around the power supply, so it's not your straight power supply design engineer that you might pull out of a power supply house."

Cardarella doesn't see this situation changing anytime soon "because it is extremely easy for a communications company to just buy a power supply."

Experienced power supply designers can make the transition to working in communications equipment companies. Except in cases where the company has a dedicated power supply design group, this transition will mean the designer will work more broadly in hardware design, according to Cardarella.

On the other hand, for power electronics engineers who want to remain focused on power electronics, there are plenty of opportunities to do so outside the communications industry. "There's a ton of work out there for good power electronics engineers," said Cardarella who noted that his firm is being kept busy by demand for these engineers in the renewable energy field.

Strong Demand In The Semiconductor Industry

Bryan Rogers, founder of the search firm Elite Professional Solutions, focuses his recruiting work in the power semiconductor industry, mainly seeking candidates for such positions as IC designers, applications engineers, and technical marketers. According to Rogers, there is currently great demand for these engineers, describing the current employment situation as a "candidates' market." With regard to positions requiring power electronics expertise in the semiconductor industry, "There are more positions out there than you can find good candidates for and it's right back to where it was three years or so ago before the downturn," explained Rogers.

The communications field is one of the industries fueling this demand. "If there's an IC design engineer with a good pedigree and knowledge of power management for handhelds like a cell phone or PDA or knowledge of networking applications, I constantly have at least three or four companies that are looking for those types of people," said Rogers who also notes these same companies have similarly strong requirements for applications engineers. Here, the IC makers are searching for candidates who have designed

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On the technology side, one of the factors driving this hiring surge is the push for higher integration. "This is especially true in the cell phone market, where they're continually going to higher and higher levels of integration on the ICs. They're combining a lot of the power management onto the baseband ICs, they're combining audio with power management, and just putting a lot more functionality onto single chips," said Rogers. The semiconductor vendors have to develop these ICs in very short development cycles "so they've got to put the resources into them and get them working very fast as the cell phone manufacturers go through their design iterations," said Rogers.

Rogers also noted how the larger economic and business trends play a key role in the current hiring demand. "I see the communications business as being very cyclical, very dependent on what the economic conditions are overall. The communications industry got hit hard like a lot of different areas during the down turn. But now things are on the upswing and they [semiconductor manufacturers] are back to the point where they don't have enough good power management people to fill the number of openings that they want to fill."

For more on communications-related opportunities for power supply designer, see "Big Power Challenges in Little Products Create Opportunities for Power Specialists," Power Systems Design, June 2010, pages 53-55, online at www.powersystemsdesign.com/career-development.

About the Author

David G. Morrison is the editor of How2Power.com, a site designed to speed your search for power supply design information. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Subscribe to the newsletter by visiting www.how2power.com/newsletters.

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CLEAN NETWORKING

By Cliff Keys

As an ever increasing number of people around the world become connected by fixed and mobile telecommunications networks, the challenges related to providing electricity to these expanding networks are becoming greater. Energy costs are among the largest expenses for network operators, and energy consumption from telecom networks is an increasing contributor to global greenhouse gas (GHG) emissions.

Faced with these economic and environmental realities, network operators and their equipment vendors have embarked on a series of new initiatives to improve the energy efficiency of telecom networks and reduce their associated carbon emissions. These efforts include dramatic reductions in the electricity required to power network elements, the integration of renewable energy sources such as solar and wind, more energy efficient practices for data center operations, and a greater focus on recycling and reuse of network equipment. A detailed analysis from Pike Research indicates that these initiatives are likely to result in a significant reduction in energy-related operating expenses in addition to a dramatic decrease in GHG emissions related to telecom network operations.

Solar Market

Despite extreme shifts in pricing, demand and governmental subsidies, the global photovoltaic market in 2011 will experience robust growth, with installations rising by 42.3% for the year, according to iSuppli. The company forecasts that worldwide solar installations will reach 20.2 Gigawatts (GW) next year, up from 14.2GW at the end of 2010. Germany, the world's leading Photovoltaic (PV) market, will continue to play a key role and account for half of the total installations, at 9.5GW. While an impressive growth total for the year, the expansion will be down significantly from the 97.9% increase in 2009.

The United States could see a solar boom that could provide 4.3% of the nation's electricity by 2020, according to a new report from Bloomberg New Energy Finance. The problem is that Investors need support the solar industry to the tune of $100 billion to keep the generation of solar electricity growing by 42% per year for the next decade to expand capacity from the current 1.4GW to 44GW.

Policy measures such as tax credits, capital expenditure grants, generation incentives and renewable electricity credits are predicted to remain a key driver of solar uptake in the US for at least the next three years, according to the report. The current drop seen in solar costs is taking place just as such policies are being implemented by the federal and various state governments, which is expected to lead to rapid growth in commercial, utility and residential solar power.

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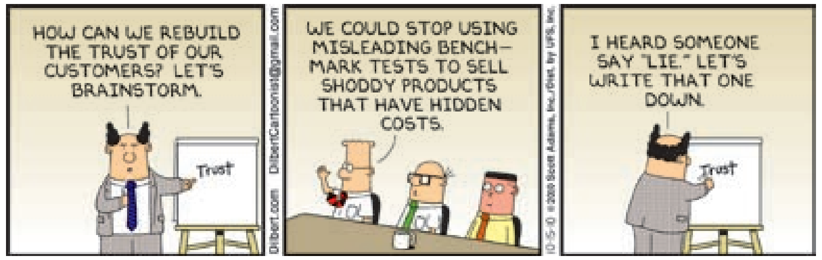
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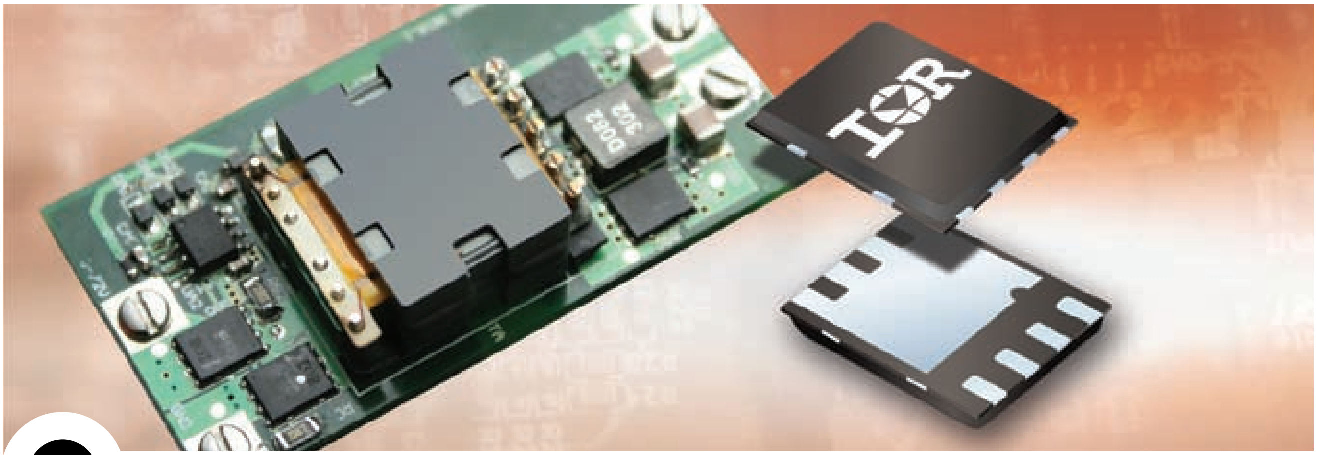

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IRFH5007TRPBF	PQFN 5x6mm	75 V	100A	5.9 mΩ	65 nC
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IRFH5020TRPBF	PQFN 5x6mm	200 V	41A	59 mΩ	36 nC
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