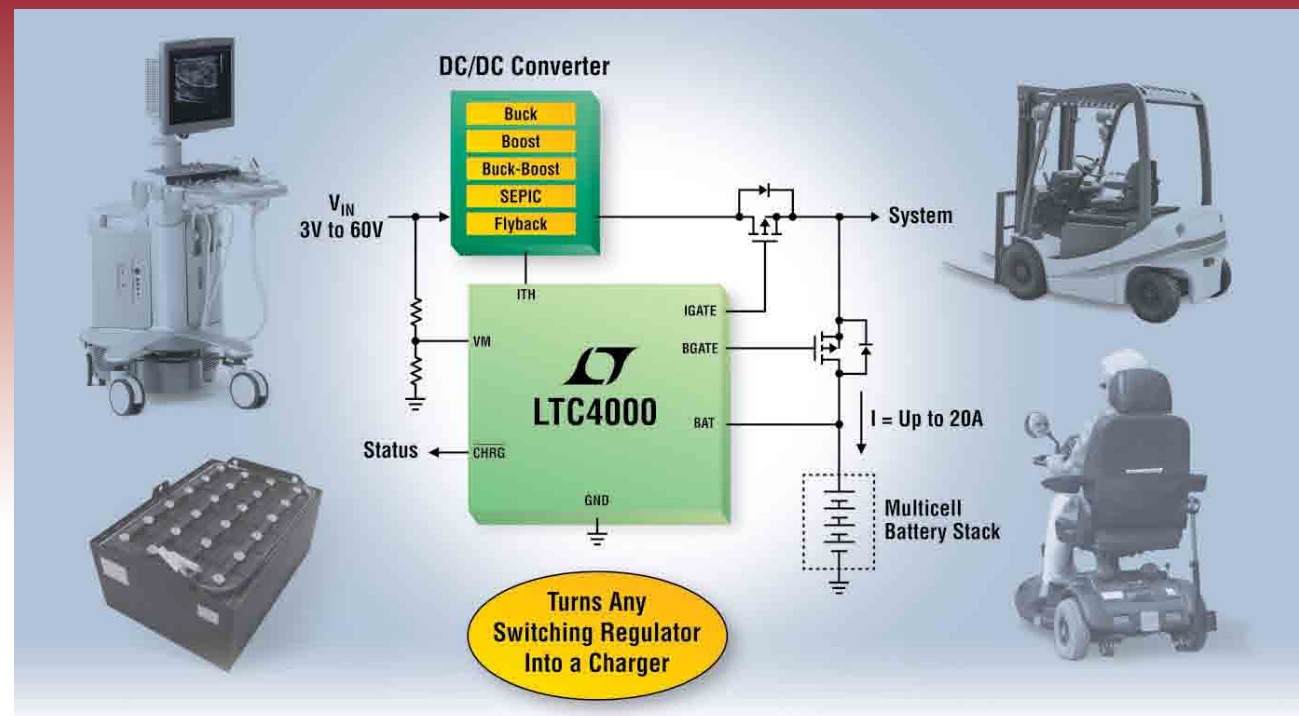




New Concept in BIG Battery Charging

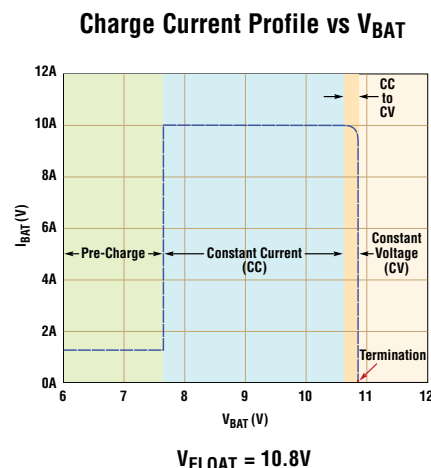


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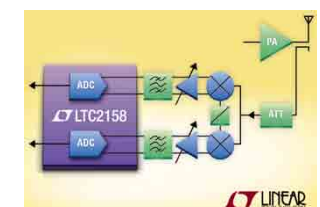
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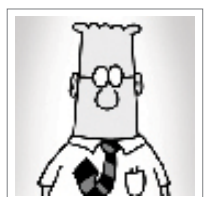
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Volume 3, Issue 6



THE COMMS EXPLOSION

Welcome to this issue of PSD where we are featuring the Communications sector. In North America, comms are pretty much well advanced, but even here there are many reports of call drops, especially in major cities such as New York where the overall need often exceeds the network capacity. Here, providers are struggling to increase capacity and bandwidth to maintain customer satisfaction, and this requires investment.

Therefore service providers and datacenters are required to become ever more powerful and have a driving need for better power efficiency which also is facilitated by our industry innovations to contain cost.

In this issue of PSD we are covering not only the issue of powering efficient communications systems, but also how companies are coping with this particular design conundrum. For instance our PowerPlayer features Alex Lidow of EPC, the innovative Gallium Arsenide (GaN) Company's CEO with his interesting perspective.

We are seeing our industry pioneer the powering and supporting of this burgeoning industry right from micropower management of portable devices to the heavy duty requirements of the cellular and datacenter installations. Good for our business in the power sector, but very challenging.

Also, with navigation features now becoming standard in smartphones like Apple Inc.'s iPhone as well as in tablets and gaming devices, the market for electronic compasses is set to close this year with sizable 73% growth, according to a new IHS iSuppli MEMS & Sensors special report on magnetic sensors from information and analysis provider HIS. Global revenue for electronic compasses is expected to reach \$419.1 million in 2011, up from last year's \$242.3 million. The hefty growth this year continues the explosive 186% surge seen by the market in 2010, with strong double-digit expansion assured for the next few years as well. By 2015, revenue is projected to amount to \$842.2 million, an increase of more than threefold from 2010.

All these aspects of comms remain a challenge for our industry.

There is much more in this issue. Please keep your valuable feedback and opinions coming in, and check out Dilbert at the back of the magazine.

All the best

Cliff

Editorial Director & Editor-in-Chief
Power Systems Design
Cliff.Keys@powersystemsdesign.com



Capacitors for Power Electronics



IGBT Snubbers
RF Mica Capacitors
DC Link Capacitors

-High Current, High Voltage Film
-High Capacitance Aluminum Electrolytic
AC Output Harmonic Filter Capacitors

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DEMANDING COMMS APPLICATIONS

Linear Technology products provide the essential bridge between our analog world and the digital electronics in communications and networking.

Digital predistortion is a closed-loop feedback system that samples the distortion bandwidth at the output of the base station transmitter and adjusts the input signal to cancel the power amplifier's intermodulation distortion products. This enables the transmitter to operate at its highest efficiency, 1dB compression point, where the power amplifier (PA) response is nonlinear.

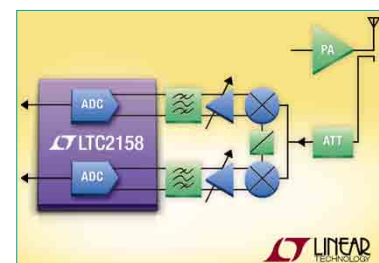
Linear Technology Corporation has introduced a family of dual (LTC2158-14) and single (LTC2153-14) high IF sampling 14-bit, 310Msps analog-to-digital converters (ADCs) designed specifically for wide bandwidth digital predistortion (DPD) linearization applications.

Due to prior limitations in the performance of available ADCs, transmit bandwidths were limited to 20-40MHz; depending on whether an IF sampling or I/Q sampling DPD architecture was implemented. To linearize a transmit bandwidth

of 20MHz, the feedback loop for the linearization algorithm must acquire fifth order intermodulation products out to 100MHz (five times the transmit bandwidth), requiring a 12-bit ADC with a minimum sample rate of 200Msps for IF sampling, or 100Msps for I/Q sampling.

Due to increasing data demands from mobile users, next-generation base stations are being architected to achieve much higher transmit bandwidths of up to 60MHz. To linearize a 60MHz transmit bandwidth requires an ADC with a minimum resolution of 14-bits and an I/Q sampling architecture with a minimum sample rate of 300Msps. In addition, the closed loop DPD algorithm requires short latency in the feedback path to achieve better efficiency in the PA.

The LTC2158-14 is the first dual, 310Msps ADC on the market to enable linearization of transmission bandwidths up to 60MHz using I/Q sampling, and offers a short pipeline latency of just 5



clock cycles for fast adaptation. The single version, LTC2153-14, is ideal for IF sampling architectures with transmit bandwidths of up to 30MHz.

Operating from a single 1.8V supply, the dual LTC2158-14 consumes 362mW/channel at 310Msps and offers signal to noise ratio (SNR) performance of 68.8dB and SFDR of 88dB at baseband with an easy-to-drive 1.32Vp-p input range. The LTC2158 and LTC2153 are part of a pin-compatible family of 170Msps to 310Msps dual and single ADCs, offered in 14-bit and 12-bit resolutions. Analog full power bandwidth of 1.25GHz and ultralow jitter of 0.15psRMS enables undersampling of IF frequencies with excellent noise performance.

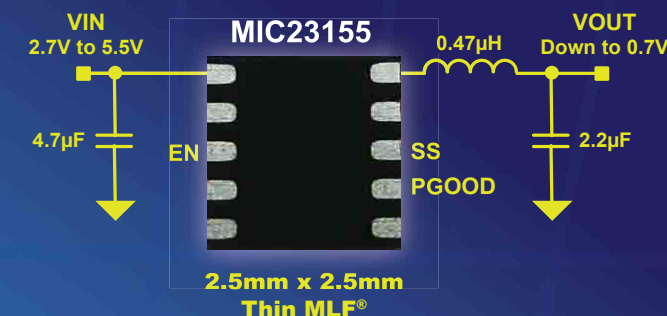
Available in commercial or industrial temperature grades, demonstration boards and samples are immediately available. The complete product family can be found at:

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WHY GaN POWER TRANSISTORS NOW?



By Alex Lidow, CEO, Efficient Power Conversion Corp.

Enhancement mode GaN power transistors such as EPC's eGaN® FETs are available to designers wanting to improve the efficiency and power density of their power conversion systems.

Ample evidence has been presented to show that, regardless of the topology, eGaN FETs perform better than the best power MOSFETs in applications needing 200 V or lower devices. Buck converters are being built with frequencies above 1 MHz and with efficiencies comparable to 250 kHz MOSFET-driven POLs. Eighth Brick isolated converters are being built with unprecedented output power capability. The same is true for half-brick converters used in PoE-PSE applications. These power conversion systems have been joined more recently by two new applications that emphasize even more the performance discrepancy between eGaN FETs and the aging power MOSFET.

RF envelope tracking has been around for a long time, but the performance of power MOSFETs or LDMOS FETs have not been able to simultaneously deliver

the power, voltage, and frequency capability required. In this application, the DC-DC converter that is used to bias an RF power amplifier can be replaced by a power supply that accurately tracks the modulated signal sitting on top of the RF carrier signal. By tracking this "envelope" the RF transistor does not dissipate as much power between the signal and the bias voltage. More power can be delivered by the same RF amplifier, or less energy is used for the same power delivered to the antenna. RF envelope tracking requires a combination of high power, high voltage, and high frequency. eGaN FETs perform well to these requirements.

In wireless power transmission it has been demonstrated that electrical energy can be efficiently and safely transmitted over distances as large as a half-meter. This recent development will, over the next few years, start to replace the

wall sockets and all the cables and extension cords we use to deliver power to our electrical appliances. We should start seeing these wireless power transmitters in late 2012. The first ones will be designed to power (or recharge) our smartphones. Next will be units to power laptops and displays, followed by power transmitters for all the appliances in our home and even our electric vehicles. eGaN FETs provide the combination of high frequency switching at high voltage and high power than make these wireless transmitters more economically viable.

As happened with the power MOSFET thirty years ago, gallium nitride transistors will reorganize the power management landscape such that new leaders and new applications will emerge, and market growth will accelerate independent of macroeconomic factors.

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POWER MARKET OUTLOOK REMAINS STRONG



By Ryan Sanderson

2011 has been an unsettled year for power semiconductor manufacturers. Revenues in the Q1 of 2011 grew by less than 1% over Q4, as end-equipment demand weakened and inventory levels remained high.

The Fukushima disaster in March introduced uncertainty over component supply to the market and led to additional orders for suppliers outside of Japan as customers sought to eliminate the risk of having to reduce their own production. This drove higher growth in the second quarter of 2011 with a sequential increase of almost 5%, however, a disappointing result in the third quarter for many, and a 'double-dip' recession looming, has left suppliers uncertain about what to expect for short and long-term market growth.

The outlook for power ICs is somewhat better over the next few quarters. This contrast in growth is driven by demand in end-applications which have high power IC content. The ongoing shift of consumers to smart phones continues to

drive revenue growth of power ICs such as DC-DC switching regulators, PMUs and battery management ICs. Smart phone adapters also favour an AC-DC regulator solution (with an integrated FET) rather than a solution using power discretes.

Infineon Technologies remained the largest supplier to the power semiconductor market in the first half of this year, growing share from 9.6% to 9.9% in the second quarter of 2011. The remaining top five suppliers are made up of STMicroelectronics, Texas Instruments, Renesas Electronics and International Rectifier.

Texas Instrument's recent acquisition of National Semiconductor should strengthen its position as the largest supplier of power ICs, moving it to second position overall. Texas Instruments held

an estimated 5.0% share of the overall power semiconductor market in 2010, whilst National Semiconductor held an estimated 2.7%. In comparison Infineon Technologies was the largest supplier with an estimated 9.4% market share and STMicroelectronics was the second largest with a 6.4% share.

All of these suppliers will be bracing themselves for a tough few quarters, but also preparing for the future growth ahead of the industry in the long-term.

By Ryan Sanderson
Senior Market Analyst
IMS Research

www.imsresearch.com

POWER SUPPLY DEVELOPMENT DIARY PART XVII



By Dr. Ray Ridley

In this article, the loop gain of the five-output forward converter is measured and compared to predictions. The final loop design is compensated with a combination of theoretical design and empirical measurements, resulting in a Type I compensator for optimal results.

Measuring the Loop of a Five-Output Forward

Figure 1 shows a five-output forward converter with coupled inductors. In the last article of this series, the control-to-output transfer function was measured, and found to have significant differences when compared to the predictions. The discrepancies were due to the coupled-output structure of the converter, and parasitics of the magnetics. This leads to measurement results that can be difficult to predict.

After measuring the control-to-output transfer function, the compensation was designed, and the control loop was measured as shown in Figure 1. The loop was closed and measured on the 12 V output of the power

supply. Normally, a Type II amplifier would be used for a current-mode control loop. However, the characteristics of the coupled-inductor design provide an area of increasing gain in the control-to-output transfer function with a corresponding phase lead. This allows us to use a simple integrator, or Type I compensation.

Figure 2 shows the results obtained for the loop gain

measurements. It can be seen that there are discrepancies in the measurement and prediction at all frequencies. This is a common result for multiple-output

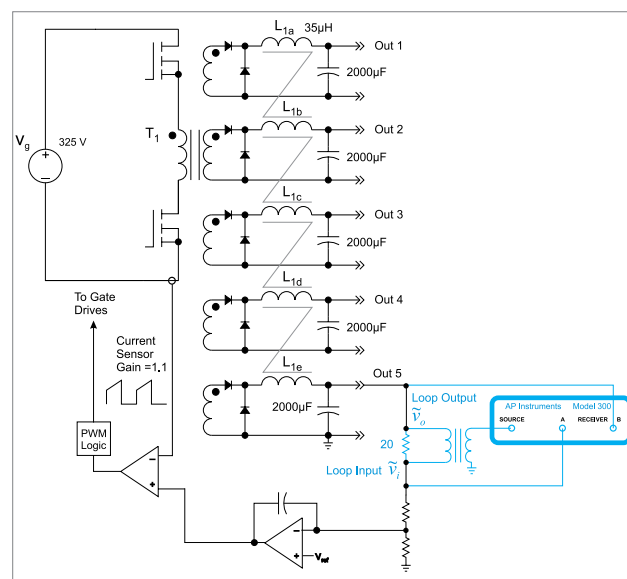


Figure 1: Forward Converter with Five Coupled-Inductor Outputs. Loop Gain Measured with the AP300 Analyzer on the 12 V Output.

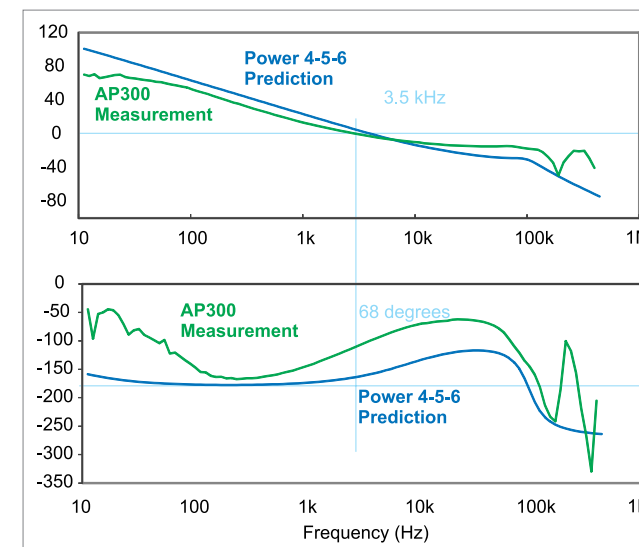


Figure 2: Initial Loop Gain Measurements versus Predicted Results

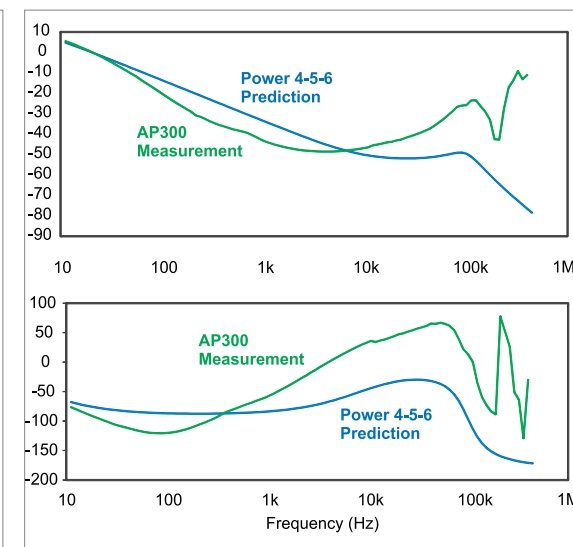


Figure 3: Variation in the Power Stage Predictions and Measurement

switching power supplies, which is one of the reasons that measurements are crucial for ensuring stability of hardware designs. Rarely are the models accurate enough for coupled-inductor power stages to properly predict stability of the system and ensure a reliable product.

It is important to understand which factors affect the discrepancies in the loop predictions and measurements. There are two blocks of the system that must be explored – the power stage and the compensation network. Both of these blocks can vary significantly from their theoretical predictions.

Predicted Loop Using Power Stage Measurements

In the last article of this series, the variation in measurements and predictions were discussed for the power stage gain. The

curves are repeated below in Figure 3.

Variations of the power stage model were due to inaccuracies when the coupled-inductor output is modeled as a single-output converter. Very little has been written on this topic since it is not easily amenable to analysis. To obtain a proper model, an approach similar to Vorpérian's work on the coupled-inductor Sepic converter would be needed. In order to proceed with the controller design, a decision is often made to work with the actual measured power stage rather than

the predicted results. The AP300 analyzer system, working with the design software POWER 4-5-6 [2-3], takes the measured results for the power stage, and cascades this with the predicted transfer function of the operational amplifier circuit.

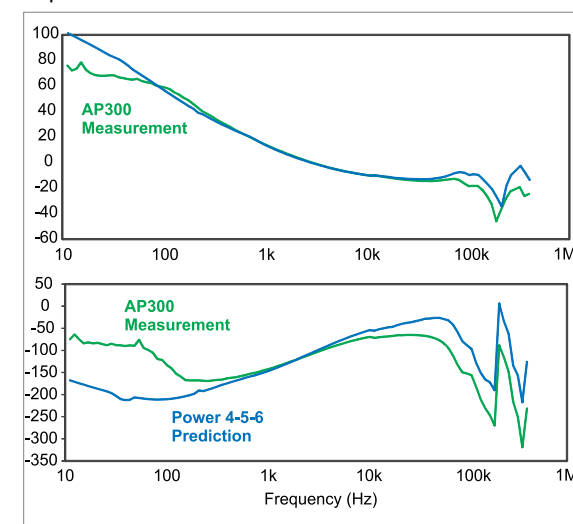


Figure 4: Predicted Loop Gain Using the Measured Power Stage, and Theoretical Compensator. This is Compared to the Measured Loop Gain

Figure 4 shows the measured loop gain versus the combination of the measured power stage and the predicted compensator. It can be seen that the prediction and measurement are now much closer to each other. Variations still persist in the very low-, and very high-frequency regions of the measurement. Since the predictions of this loop gain use the actual measurements of the power stage, these remaining discrepancies suggest that the operational amplifier does not perform according to the predicted model.

The crossover frequency of the loop is at approximately 3.5 kHz, and the measured phase margin was 68 degrees. This was achieved using a very simple Type I compensator.

Limitations of the Operational Amplifier

To measure the operational amplifier response, we can still inject a signal with the same circuit shown in Figure 1. The amplifier response is obtained

by connecting Channel A of the AP300 Analyzer to the output of the power supply, and Channel B to the output of the error amplifier. The measured and predicted responses are shown in Figure 5.

There are two areas of variation in Figure 5. One is at low frequencies, up to 100 Hz, and another is at high frequencies, from 100 kHz. At low frequencies, the open-loop gain limit of the operational amplifier is encountered. This is specified as a worst-case of 65 dB in the data-sheets, and measured at around 70 dB. Careful measurement is needed to extract this data, and a large injection signal is required to get clean results. At high frequencies, the gain-bandwidth limitation of the amplifier is encountered. This is often lower than expected due to the high-noise environment in which the amplifier must operate.

There are practical limitations to how much both of these regions can be improved. The gain limitation at low frequencies can be difficult to improve upon due to noise at the amplifier terminals. Although this noise is at a very high frequency, it still carries low-frequency modulated information. It is quite com-

mon to require bypass capacitors across all three terminals of the operational amplifier to improve the noise issue.

The gain-bandwidth problem is also hard to overcome. Working with a higher performance amplifier usually exacerbates the noise problems, and makes the converter impossible to control.

Summary

The control loop on the five-output converter was closed using a Type I compensator. This was possible since the complexities of the coupled-inductor power stage model introduce a zero in the measurements that makes a Type II compensator unnecessary.

Reliable design of the feedback loop is done using a combination of the measured power stage, and predicted feedback components. The final measured result is close to predictions, with discrepancies at low and high frequencies caused by the limitations of the error amplifier.

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www.ridleyengineering.com

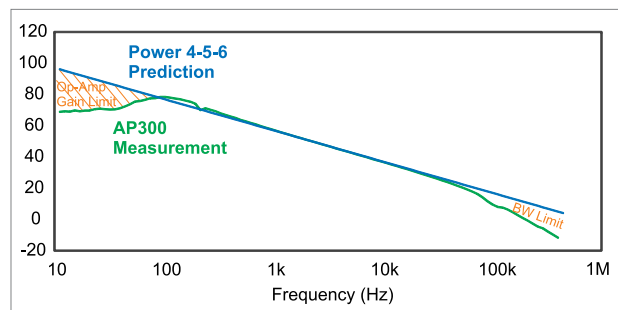


Figure 5: Measured and Predicted Error Amplifier Compensation

DATACENTER POWER ARCHITECTURE

System engineering and analysis on central-office datacenter power

By Maurizio Salato

Telecom Central Office Datacenters have seen rapid evolution in terms of the architecture of their power supply arrangements; a number of different approaches have been used in relatively quick succession and, indeed, more than one approach may be found within a single installation.

This article considers a number of embedded power supply architectures for Telecom Central Office Datacenters, looked at on a system perspective. Traditionally, power supplies were a simple service function; each major unit within a facility such as a datacenter had its specified requirements in terms of the number and level of its voltage rails, and the current that had to be provisioned in each case. If there were safety and protection requirements – voltage or current limits that, if exceeded, would be regarded as indicating a fault condition – then the response to those conditions would typically be a local trip or shut-down with, at most, a simple flag being set to indicate the existence of a problem.

The hardware that met those requirements changed only slowly over many years; the power supply in the form of the rectangular metal enclosure or “brick” was a familiar system component; self-contained, autonomous voltage-in, voltage-out devices. Whether custom-designed or sourced from a standard range, they invariably resided in any available space within – or even outside – the cabinet or rack, but had minimal mechanical and electrical integration with the host system.

Recent years have seen a rapid, and accelerating, pace of change in the design of such central-office systems in terms of their power – both computing or data throughput power, and the electrical power required to deliver it – and in levels of integration, and power density.

Power density, in fact, has been one of the fastest-moving parameters, irrespective of whether it is measured at circuit-board, rack, cabinet or total system level, and one of the key challenges in power supply provisioning has been to accommodate and to keep pace with its growth. Alongside, and intimately connected with, higher power, higher density, higher input voltages, and higher load currents sits the overall requirement to achieve higher efficiency. Reducing losses in the power supply subsystem lowers the heat dissipated within the system, with consequent reduction in the burden on cooling arrangements, boosts reliability by reducing component temperatures, assists with improving the environmental credentials of the installation and – far from insignificant at a time of escalat-

ing power tariffs – helps to contain rising power bills.

Many of the changes forced on power supply architectures can be traced to the evolution of microprocessors and other semiconductor devices. Successive generations operate at lower voltage levels while consuming higher currents; the processing power they deliver per Watt has grown rapidly but this has not, in general, led to any reduction in power dissipated in a given card or rack. Rather, throughput has risen dramatically while power density has at best grown at a more modest pace. High currents and low voltages force regulation closer and closer to the point of load; otherwise, currents of many tens of Amps, routed over any physically-feasible PCB or wiring structure, suffer voltage drops that are unacceptable as a proportion of a rail that may only be 1V or even less.

The disparity between such low voltage levels at the point of load, and the traditional telecom system-supply rails of (typically) 48V has stimulated an evolution in hierarchical power distribution architectures. For a majority of applications implemented today, the Intermediate Bus Architecture (IBA) has been the preferred power architecture. This power architecture has led to the development of the isolated, semi-regulated DC/DC converter known as the Intermediate Bus Converter (IBC).

Fixed ratio Bus Converters that employ a new power topology known as the Sine Amplitude Converter (SAC) offer dramatic improvements in power density, noise reduction, and efficiency over the existing IBC products. The power systems designer faces the challenge of providing small, cost effective and efficient solutions that keep pace with – or preferably, exceed – the trends in system voltage and current identified above. Traditional power architectures cannot, in the long run, provide the required performance. Vicor's Factorized Power Architecture (FPA), and the implementation of V•I Chips, provides a revolutionary new and optimal power conversion solution that addresses all of these challenges. The technology behind these power conversion engines used in the IBC and V•I Chips has a direct bearing on the designer's ability to respond to changing power supply demands.

System view

A systematic approach to partitioning shows that several functions need to be accomplished, while each architecture offers

different building blocks. System functions are summarized in Table I. These functions present some trade-offs, which need to be considered: for example

- DC step-down ratio vs. efficiency
- Load voltage vs. efficiency
- Battery cells (number and size) vs. backplane voltage range.
- Bus conductor section and current level vs. losses.
- The environment in which the typical datacenter operates is also changing, which adds an extra dimension to the matrix a recent trend is towards adoption of High Voltage DC infrastructure distribution instead of standard AC line.

IBA and FPA

The essential features of an Intermediate Bus Architecture (IBA) are that it distributes semiregulated 42-50V voltage (therefore taking advantage of reduced distribution losses); then, by means of an isolated, nonregulated Bus Converter, this voltage is approximately reduced by a factor of 4 (or 5), while the voltage reference is changed

Block	Functions
Power Entry Module	- AC/DC voltage conversion - Isolation
DC backup	- System availability through line faults - Interface with backplane distribution
Distribution	- Efficient power transmission
Point-of-Load	- Isolation from Backplane - Step-down DC/DC conversion - Load voltage regulation

Table 1. Major functional aspects of the power-supply system hierarch

from positive to negative (intermediate bus). This intermediate 9-12V bus enables non-isolated Point-Of-Load converters (niPOLs) to provide final step down and regulation function at the same time.

The Factorized Power Architecture (FPA) represents a further evolution onwards from IBA: the high efficiency, fixed ratio, isolated but not regulated converter is used as Point-Of-Load device, providing isolation and current multiplication directly from 48V; upstream, a non isolated device provides voltage regulation by dynamically adjusting the 48V "Factorized Bus" slightly above or slightly below 48V. This avoids the need for the intermediate bus altogether, therefore further increases distribution efficiency.

A state-of-the-art configuration for an IBA for a 48V telecom system is shown in Figure 1. Each stage accomplishes two main functions,

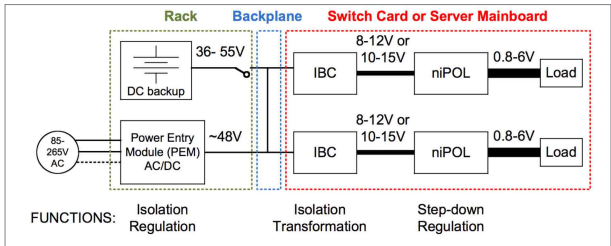


Figure 1. Intermediate Bus Architecture block diagram

as listed in the diagram. An aspect to note about this structure is that the first stage (AC/DC Power Entry Module, PEM) is a high power, highly optimized commodity device, which takes care of power factor correction (often from single or three phase lines) on a univer-

sal input voltage line, and provides an isolated output. Similarly, the niPOL comprises a standard, off-the shelf single or multiphase Synchronous Buck converter, which can deal with a relatively wide input range while providing accurate Load regulation. The bus converter is a fixed ratio electronic transformer device that interfaces the 48V backplane with the 9.6V or 12V (nominal) intermediate bus. In terms of total life-cycle cost, all three stages have achieved extremely high performances, with commodity level acquisition costs, and peak efficiencies well in excess of 90%. In order to minimize intermediate bus losses, the IBC is placed as close as possible to the niPOL it supplies.

The dotted lines in Figure 1 also show where the various blocks are located: DC backup and AC/DC PEM are normally stand-alone systems, sized to supply an entire rack through the distribution

- to be achieved.
- IBCs are available as open-frame, through-hole devices with power ratings ranging from few hundred Watts to one kilowatt; as such, they can effectively be placed close to one or a few niPOL regulators.
- niPOL regulators are standard synchronous buck converters that are tailored to each specific load.
- The major drawback of this configuration is that blocks at rack level are generally oversized, which implies an added initial cost and higher energy cost because they do not operate at their peak efficiency.

A possible FPA for a typical system is shown in Figure 2. It still consists of three stages of power conversion; while the Adaptive Cell PFM first stage is functionally equivalent to the AC/DC PEM block in the IBA, the load regulation function is now accomplished

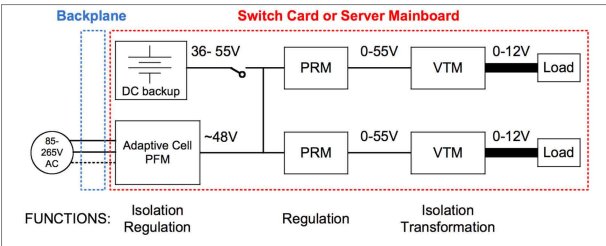


Figure 2. Factorized Power Architecture block diagram

backplane. IBCs and niPOLs are either discrete or modular devices that are soldered on each unit Mainboard. Further points to note include;

- Having larger, stand-alone AC/DC converters allows lower cost and higher peak efficiency

by a non-isolated converter, the PRM. This converter works with an input line range of 36V to 55V, and outputs a "factorized bus" that can range from 0V up to 55V.

The VTM stage is enabled by the same topology used in the

IBC (in effect, an electronic “DC transformer”), and provides both effective current multiplication (by a fixed factor), and isolation. Compared to IBC, FPA offers significant system advantages:

- The factorized bus is normally maintained above 40V, reducing losses and conductor cross-section requirements on the Mainboard.
- The Load voltage that can be regulated has a wider range, given the factorized bus range and the availability of various VTM transformer ratios.
- Just like IBCs, PRMs and VTMs are power components that can be directly soldered on the Mainboard PCB
- The PFM is also a power component that can be mounted on PCB.
- In this case also, the dotted lines show where the various components are ideally located. It is clear that FPA offers the possibility of integrating the entire power supply within each unit, potentially avoiding any 48V distribution at rack level.
- Given the ever increasing power density of DC backup systems, it is conceivable to integrate that block at Unit level as well, rather than at Rack level. This approach offers a number of advantages; Each Switch or Server unit is fully autonomous and does not depend on infrastructure, even just at rack level
- The entire supply system, being more granular, can be

tailored more closely to actual power levels of use, therefore maximizing conversion efficiency and minimizing acquisition costs

- Low voltage levels are generated within, and confined to, close proximity of the Load, minimizing distribution requirements and losses.

FPA flexibility is also evident when a high voltage DC supply is available: in this case, by simply substituting the Adaptive Cell PFM block with a High Voltage Bus Converter module (BCM), the same system can be efficiently powered, as shown in Figure 3.

Converter topologies

Three converter topologies contribute to enabling efficient, PCB-mountable power components for both IBC and FPA; these are the Sine Amplitude Converter (SAC);

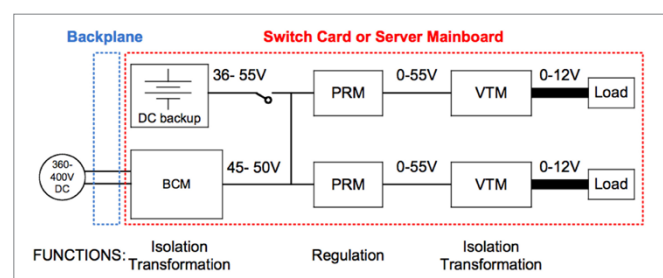


Figure 3: FPA with High Voltage DC infrastructure block diagram

Zero-Voltage-Switching Buck-Boost Converter (ZVS-BB); and Adaptive Cells, Double Clamp Zero Voltage Switching Converter (DC-ZVS).

The Sine Amplitude Converter is a transformer-based series-resonant topology that operates at a fixed

frequency, equal to the resonant frequency of the primary side tank circuit, as shown in Figure 4. The entire powertrain (primary and

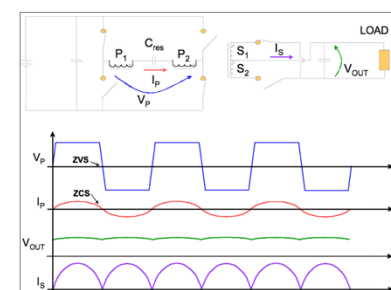


Figure 4: Sine Amplitude Converter topology and waveforms

secondary) is locked to the natural resonant frequency of the tank and is switching at primary current zero-crossing points both at turn-on and turn-off, eliminating switching losses in the transistors and reducing the generation of high order noise harmonics. The current in the primary resonant tank is a pure sinusoid rather than a square

wave or a partially sinusoidal waveform; because it does not rely on closed loop operations, but on voltage

imbalance across its resonant tank, its dynamic performance is effectively broadband, up to 2/3 of the switching frequency.

In response to a load step on the secondary, the Sine Amplitude Converter reacts by increasing the

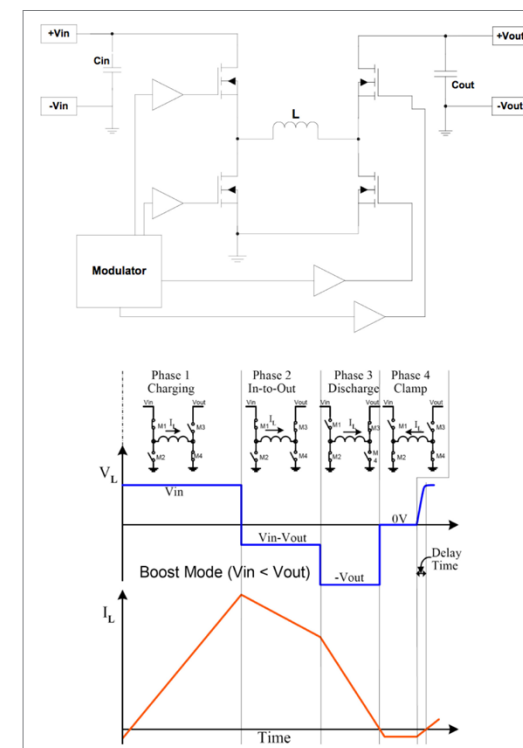


Figure 5: Zero Voltage Switching Buck-Boost Converter topology and waveforms

amplitude of the sinusoidal current on the primary resonant tank. The dynamic behaviour associated with this transient is only limited by resistive elements in the conduction path and the time constant associated with filter capacitors' energy depletion, being the primary current driven by voltage imbalance across the tank.

The Zero Voltage Switching Buck-Boost Converter is a conventional buck boost topology with a non-conventional modulation scheme (Figure 5). It is operated in discontinuous mode, with the majority of the power processed with the powertrain inductor directly connected between the input and the output (Phase 2 in Figure 5). Proper switch timing ensures that all

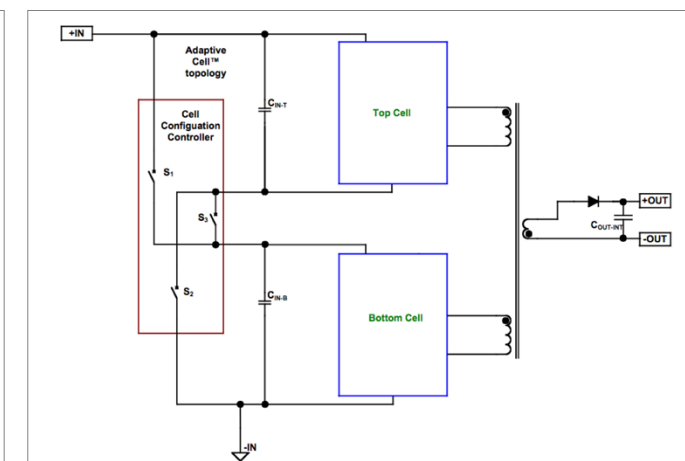


Figure 6: Adaptive Cells, Double Clamp Zero Voltage Switching Converter topology

the transitions happen at zero voltage, thus eliminating switching losses. The converter can therefore operate at few MHz and easily exceed 97% efficiency.

ed converter with unconventional modulation and storage elements, which ensure all the switches are turned on either at zero voltage or zero current. This enables switching frequencies in the MHz range with efficiency above 95%. The Adaptive Cell feature allows the converter to operate at the same efficiency over universal input range.

A unique feature of this topology is the complete symmetry with respect to the input and output line. This device acts as system regulator, taking care at the same time of both input variation, and load regulation. However, in nominal conditions, it is called upon to compensate only for minimal variations, therefore further maximizing efficiency.

The Double Clamp Zero Voltage Switching Converter (DC-ZVS) consists of two cells with the same topology – DC-ZVS – configured dynamically (that is, automatically switched as required) either in series or in parallel, in order to efficiently interface a wide variation of its input voltage. The Double Clamp consist of a standard isolat-

Conclusions

Advances in power conversion technology enable power supply systems to be effectively built and integrated on board as power components. This paradigm shift requires a revision of current system architectures, in order to take fully advantage of power density and efficiency, and reduce total cost of ownership.

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MANAGING THE POWER

Simplifying total energy management

By: Alan Elbanhawy

Energy management techniques have emerged as competitive and differentiating features of electronic equipment. Traditional DC-DC Integrated Circuit (IC) point solutions have focused on optimizing single power parameters via fine tuning of components. That is no longer sufficient or practical for managing system energy consumption under real-time and multi-variable operating conditions.

This article describes a novel new approach to energy management in electronic devices through use of DC-DC converters with the ability to monitor and control several aspects of their sub-power delivery system on the fly. Using digital interfaces on new multi-rail power management units, system designers can now go far beyond just high-efficiency static designs. In this article, a description of this approach and the key parameters required for a Total Energy Management (TEM) implementation will be analyzed.

What is Total Energy Management?

Traditionally power system designers have focused heavily on efficiency of power conversion as an end objective of the design. This is because limited interaction or data exchange has been

possible between the power subsystems and rest of the designs. Power subsystems are manually optimized at the time of design and are not part of a dynamic and adaptive loop based on real-time operating state of the equipment. Total Energy Management is an approach that not only provides high-efficiency power conversion ICs, it also focuses on total system efficiency. The objective is to dynamically control the power by monitoring the environment resulting in truly efficient system designs – not just of power sub-conversion.

Another important aspect of a power subsystem design is the amount of radiative or conductive noise energy that it creates. Most modern power supplies are based on switching mode operation where large amount of currents



Figure 1: The Total Energy Management approach to design

are being switched on clock edges. That can lead to both conductive and radiative emissions. Managing these emissions can be a challenging and costly affair, both in terms of bill-of-material costs and engineering time. Minimizing these emissions systematically at the source is part of the TEM approach of power system design. Implementation of Total Energy

Management requires features such as (see Figure 1):

- Real-time energy monitoring – like input power measurements, power system health monitoring on a continuous basis
- High efficiency conversion – including light load management, ultra-low standby power and sleep-mode power
- Fast system dynamic response and sequencing control – including the ability to rapidly change operating mode of the device from continuous to discontinuous modes, rapidly go in and out of standby and sleep modes ; flexible sequencing control to optimize multiple-rail output power start-up
- Digital power control – like voltage margining to manage power consumption under differing performance requirements, managing standby and sleep requirements
- High-efficiency EMI control and mitigation – minimizing radiative and conductive emission noise from the power supplies.

An energy management IC solution implementing such a feature set will exceed the traditional boundaries of power management ICs that are single block components optimizing one or two specific system parameters. Moreover

implementation of such a feature set requires digital interface and intelligence in the power subsystem that can be utilized across multiple-rails in a Power System-on-Chip (SoC) setup. The right approach is to integrate these essential energy management features into multi-rail power management device in a SoC like fashion.

An example of the TEM approach is Akros Silicon's new EnergySense AS19xx family of high efficiency DC-DC converters. Each digital power management unit (DPMU) integrates multiple features into each device (Figure 2). The product family comprises 10 products with five different power manager topologies. All are pin and PCB compatible and come in either hardware or software (I2C interface) versions. Each has three or two outputs as a combination of two fully integrated synchronous DC-DC converters and one versatile

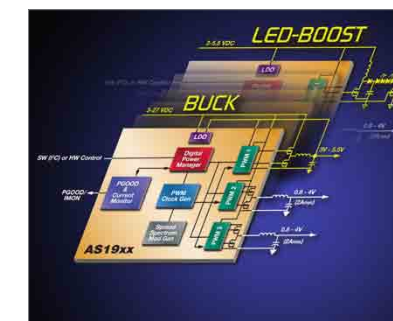


Figure 2: Pin and software (I2C) compatible DC/DC converters in the AS19xx family offer real-time energy management.

controller configurable as buck, boost or LED drive.

Total Energy Management is applicable to a wide range of applications, including 4G LTE residential gateways and femtocells to tablets and large display-oriented consumer devices, ultra-books, e-books, digital photo frames, NAS and media hubs, Internet-TV and IPTV set-top boxes, automotive infotainment systems, solid-state lighting, and communication equipment with cluster-power or intermediate bus architectures, as well as many other applications.

Here are a few examples of how this integrated approach facilitates the design and improves operational performance and efficiency:

Dynamic Power Amplifier Control

4G LTE Gateways/Cells using TD-LTE require the power amplifier (PA) to be operational only during the transmit mode. Typical PA efficiency even at the highest transmit power levels is below 40% due to linearity requirements. By employing dynamic, high-speed control, the PA power can be disabled during the listening mode (Figure 3), thus eliminating energy waste. The AS19xx devices can enable/disable each rail in 100µs – fast enough to permit this function without external control.

Dynamic LED Backlight Control

A Tablet PC's LED backlight screen consumes >50% of its power and is the biggest factor in battery life of the device. LED

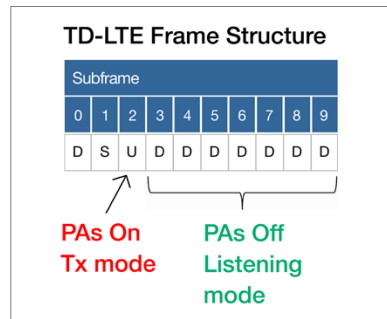


Figure 3: 4G data link transfers only require PA on during transmit period.

backlight management is not new. Traditional DC-DC converters support either Analog or PWM based dimming. The AS19xx devices support that but go a step further in supporting a fully integrated internal I2C-based 32-step (5-bit) logarithmic PWM dimming. This not only reduces external components but enables system designers to use a fully software-based approach to dimming by simply writing a “dimming word” to the device. Now software can dim the screen based on content, such as when watching a movie as opposed to reading content, bringing next

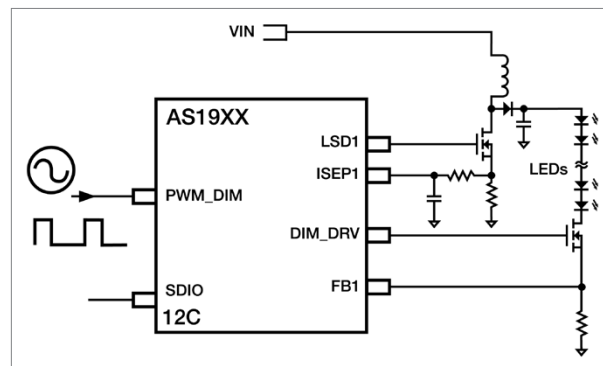


Figure 4: The AS19xx enables multiple-load LED dimming options, including fully internal PWM Dimming capability.

level of battery performance optimization without adding cost and components to the design (Figure 4)

Real-time Input Power Measurements

During the development phase of an electronic system, changes in the software can have dramatic effects on power consumption. TEM devices, like the AS19xx, are capable of providing feedback on power usage on each rail in real time. This can speed development and result in more efficient product designs.

EMI Management

Switch-mode power supplies require EMI filtering to minimize the injection of power supply noise onto the power line to prevent radiative and conductive emissions. This leads to extra bill-of-material cost and design efforts. The AS19xx devices use integrated spread-spectrum clocking to mitigate EMI. This leads to less design cost, higher system efficiency, and faster time to market.

Conclusion

The insatiable appetite for power and multiple rails in modern electronics is only matched by the need for high performance and advanced operational and

control features that confront power system designers. Their major challenge is to achieve all the design requirements with an implementation that has the highest efficiency ($\geq 95\%$), occupies the smallest possible PCB real estate, and at a cost sometimes bordering on the impossible. In other words, IC designers have to become system designers who use the available data to make energy management choices for their applications.

The most critical question designers must consider is this: which IC(s) will do the job? A Total Energy Management approach embodied in Akros' AS19xx DC/DC converter family offers a simple, elegant answer. The solution meets the designer's energy management needs without adding complication, space and cost — all while providing real-time power monitoring and adding energy management features that increase efficiency. The idea behind this 10 IC product family is to offer designers a choice of selectable ICs that can be used in a wide range of applications and across a multitude of platforms.

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AVOIDING COEXISTENCE PROBLEMS

Simplifying designs with integrated RF modules

By Allen Chien PhD

Applications for portable wireless data communications have been booming in the last few years. For designers, these applications pose the challenge of designing multiple high-efficiency, low-noise RF channels in as small a space as possible. One approach to meet this challenge is to leverage integrated RF modules that can provide superior coexistence faster and more efficiently than use of discrete components.

Applications for portable wireless data communications have been booming in the last few years. For designers, these applications pose the challenge of designing multiple high-efficiency, low-noise RF channels in as small a space as possible. One approach to meet this challenge is to leverage integrated RF modules that can provide superior coexistence faster and more efficiently than use of discrete components.

Wireless is becoming the preferred method for consumer and commercial data communications of all kinds. WiFi networks abound

in the home, supporting such devices as PCs, tablets, smartphones, gaming systems, and even televisions. Public WiFi “hotspots” are also plentiful, used for web surfing, messaging, and creating femtocells for the off-load of cellular network IP traffic.

There are also many other wireless data links in use beyond WiFi, including Bluetooth for remote headsets, ZigBee for home automation networks, WiMAX and LTE for wireless broadband, and cellular telephony. In addition, transportation and utility industries are working to employ many of these same network

technologies for applications such as the smart power grid and traffic management. Similarly, other industries seek to employ wireless networks for machine-to-machine communications to automate various elements in production and commerce.

This growing dependence on wireless data communications places a two-fold burden on equipment developers. First, their designs must provide extremely high quality transmit and receive channels. Transmit channels must meet strict power, spectral, and linearity standards, providing sharp bandwidth filtering while avoiding amplifier distortions and the reflections caused by

impedance mismatches. Receive channels must be efficient to avoid signal loss and must eliminate as much noise as possible in order to maximize data rates while dealing with very low received signal strengths.

While addressing these RF design challenges developers must also deal with the burden of channel coexistence. Many systems need not one but two or more wireless links, each corresponding to different standards. A laptop computer, for instance, might incorporate both WiFi and WiMAX connectivity in its design. A smartphone will include WiFi with Bluetooth as well as GSM, 3G, and LTE. Such portable systems also require the RF designs for the various channels to be as compact as possible and the different channels are typically interwoven on the circuit board.

This physical and spectral proximity places stringent demands on receive filters. For example, a WiFi design may need to operate over a 2.4 - 2.5 GHz band while rejecting signals from a nearby 3G transmitter at 2.1 GHz. Such tight

frequency spacing requires filters with extremely steep roll-offs.

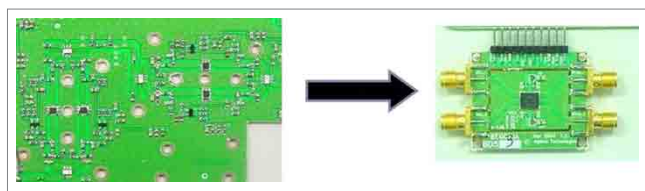


Figure 1: An example of the simplification of an RF design using an integrated front-end module

Integrated front-end modules (FEM) for RF coexistence can provide independent transmit and receive paths with in-line filters and amplifiers along with signal switches for sharing antenna connections. Utilizing an integrated module rather than pursuing a discrete-component design allows developers to significantly reduce their design effort and costs while creating highly precise and efficient RF subsystems. The modules save board space, as well, compared to discrete designs (Figure 1). Integrated FEMs achieve these

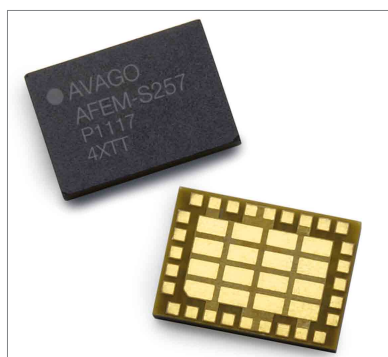


Figure 2: Amplifiers, switches, and filters are all encapsulated in a single package for simple layout

benefits through a number of key design features. First, the modules provide developers with a fully-designed and optimized configuration of layout and components. As an example,

Avago Technologies carefully designs modules with matched 50Ω impedances and

uniform phase delays on all signal paths. All active and discrete components in the modules are carefully matched and the design tuned to provide optimum operating characteristics along the entire RF path.

Another key feature of integrated FEMs is that they bundle everything into a compact form factor (Figure 2). All of the critical design and layout tasks are already done, with no tuning or tweaking necessary. Designers only need to deal with a few connections to a single component when laying out the front end of their RF subsystem, greatly reducing design time.

The integrated FEMs not only help eliminate the front-end RF design task, they help speed other development stages. Because the modules are fully assembled, optimized, and tested, for example, they eliminate the need for front-end design validation. Later in the development effort, these same characteristics

reduce time and effort needed for regulatory and standards compliance testing of the finished design. All this reduction in development time equates directly to quicker time-to-market as well as lower development costs.

The integrated FEMs also help lower production costs. The single FEM replaces numerous discrete components in the production bill of materials (BOM), reducing the cost of BOM management and inventory handling. Because the FEM is pre-tested, the design's RF section will also have a better production yield than products using discrete component designs.

The advantages that integrated FEMs bring to designs needing wireless coexistence can best be understood by examining a module's capabilities in detail. The Avago AFEM-S257 WiMAX coexistence FEM supports reception and transmission of 16 quadrature amplitude modulation (QAM) WiMAX in the presence of WiFi and other nearby RF channels, and offers dual receive channels to allow reception of two simultaneous signals or support RX diversity reception. It leverages Avago's proprietary film bulk acoustic resonance (FBAR) filters to achieve steep roll-off characteristics to provide high out-of-band rejection. The low insertion loss of FBAR filters

ensures maximum receive signal strength and minimal waste of transmit power, helping maximize battery life in portable devices.

The S257 module integrates a linear power transmit amplifier, low-noise receive amplifiers with pre-selector FBAR filters, band-pass filters, and RF switches with 50Ω impedance on all RF ports (Figure 3). The design is optimized for operation in the 2.5

0 dBm to the antenna output while the module typically draws 95 mA from a 3.6V supply. The amplifier has a 23 dB gain step, so in high power mode the amplifier produces 24 dBm while the module typically draws 420 mA. The transmit amplifier's total gain is 34 dB in high-power mode.

Typical gain flatness for the transmit amplifier is 1 dB over any 10 MHz band, with a gain variation of no more than 1 dB over the full supply voltage range. This allows the transmit channel to fully meet WiMAX QAM mask specifications with a typical error vector magnitude (EVM) of -34 dB (2.5%) in

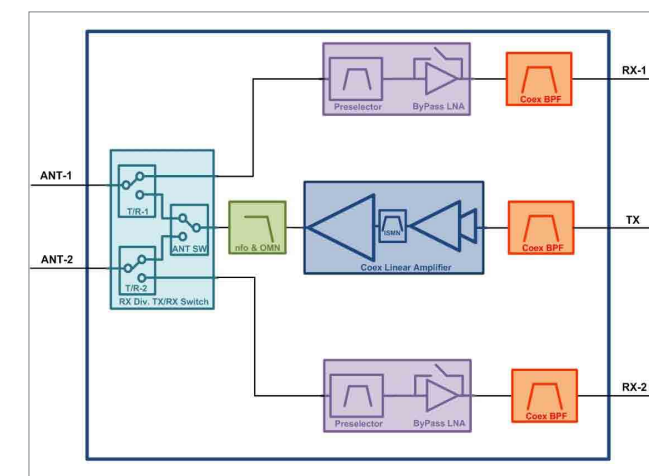
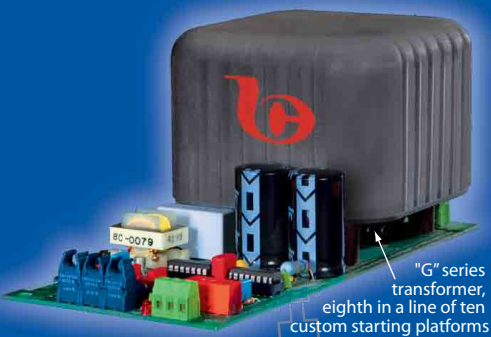


Figure 3: The AFEM-S257 is a complete WiMAX coexistence front-end module with dual receive channels in the 2.5 - 2.7 GHz band

to 2.7 GHz band of WiMAX with a supply voltage of 3 to 5VDC. All the amplifiers in the S257 module have exceptional tolerance to supply voltage and temperature variations because of the GaAs pHEMT process technology. The module's transmit amplifier has a selectable gain, allowing operation in low power mode to reduce the module's demand on a battery supply. In low power mode the amplifier delivers

high power mode. The low-noise amplifiers in the module's receive pathways provide a gain of 15 dB, typically producing 10 dB of overall gain from antenna input to receive path output. In the presence of strong input signals the receive amplifier can be bypassed, reducing current draw from 10 mA to 0.25 A per receiver. Even with the amplifier engaged, the module



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Frequency Band	Transmit Path Out-of-Band Rejection (dBc)	Receive Path Out-of-Band Rejection (dBc)
698 – 720 MHz	80	70
800 – 915 MHz	70	70
1574-1576 MHz	50	35
1805 -1880 MHz	40	30
1930 – 1990 MHz	30	30
2110 – 2170 MHz	10	35
2400 – 2468 MHz	35	30
2451 – 2473 MHz	25	30
3300 – 3800 MHz	30	30
5000 – 5380 MHz	60	-
>7200 MHz	60	-

Table 1: The sharp roll-off characteristics of FBAR filters permits strong out-of-band rejection of neighboring transmitters

exhibits a maximum 3.5 dB noise figure between an antenna input and its receive channel's output. In support of multi-channel coexistence the switches and filters provide substantial isolation between the various signal pathways and operating frequency bands. Isolation between the two receive channels as well as either receive channel and the transmit channel is 25 dB to prevent cross coupling of signal pathways. The FBAR band-pass filters provide substantial out-of-band rejection on both transmit and receive pathways (Table 1), with at least 35dB of rejection relative to carrier at the WiFi ISM band for the receive channel.

This entire RF front end is packed into a space-saving 5x7x1 mm sealed package, representing at least a 25% savings in board space relative to a discrete component design. Transmit and receive ports are arranged on one

side of the module with antenna connections on the opposite side for convenient signal routing, with ground pads between signal lines for isolation. Creating an effective front-end for designs requiring coexistence of multiple RF channels at nearby frequencies represents a significant challenge, even for the most experienced RF design engineers. For developers creating today's multi-radio mobile devices, integrated FEMs such as the Avago AFEM-S257 are an opportunity to side-step those design challenges. By utilizing an integrated FEM, developers can bring their devices to market quicker at less expense while obtaining a highly compact design with state of the art performance.

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UPS SIZING

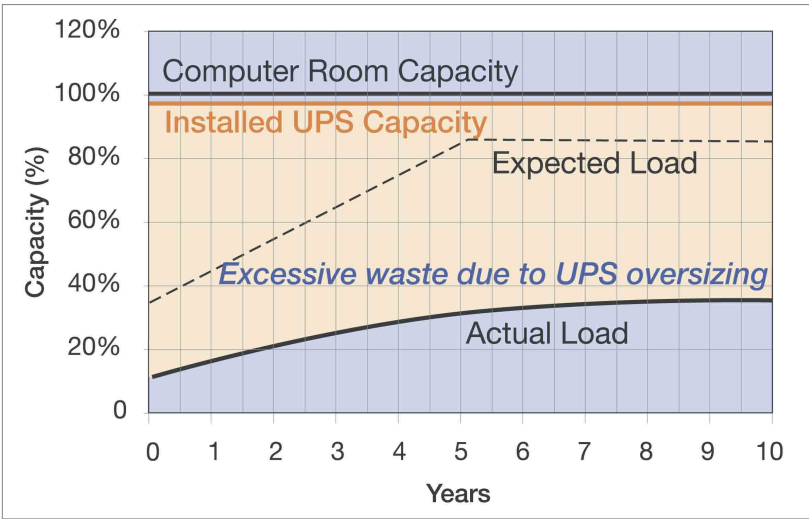
Practical and theoretical considerations

By Matt Henley

Choosing a UPS of the right capacity for a commercial or industrial application may appear as a simple task.

In reality however, making the correct choice depends on knowledge and understanding of a site's load and its characteristics. This article looks at the practical and more theoretical considerations contributing to the process of defining the UPS sizing required.

Although typically associated with data centres, Uninterruptible Power Supply (UPS) systems are finding their way into an ever-widening, diverse range of environments. This is due to the increasing number of telecoms, medical, industrial processing, retail and other applications that now rely critically on electrical equipment and power availability. This diversity imposes widely varying loads on any UPS chosen. Additionally, different applications generate different views on just how critical their load is, and the degree of protection that must be provided. Therefore, this article starts with some practical considerations for site load sizing, before addressing at how to provide for



this load with a level of security appropriate to the application. Clearly the load at any given site will be unique, depending on the mix of equipment in its make-up. However the load will also be time-variant in several ways. There will be daily and weekly variations as office occupancy and equipment use drops overnight or during weekends and holidays, and seasonal variations as the weather, and demand on air-conditioning or heating, changes. Longer term changes arising from operational expansion and addition of

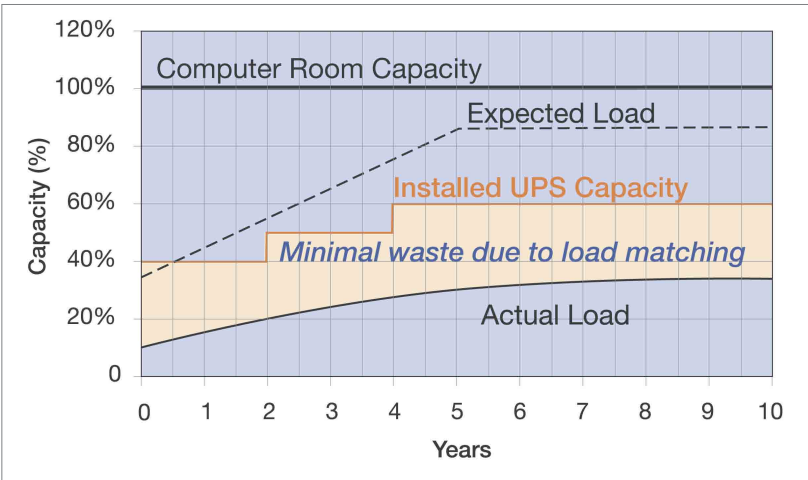
new equipment are also likely. Investigation of the critical load's on site components, including measurement of the load's performance over a meaningful time, is a necessary part of the UPS sizing exercise. Within the UK, the UPS is usually fed from the National Grid electrical mains, and feeds the site's critical load. During a mains failure, the UPS batteries maintain supply. To start sizing the UPS, the load should be scoped in terms of its required supply voltage, frequency,

number of phases, load current, power factor and power consumption.

UPS manufacturers express their products' power capability in VA or kVA. Meanwhile, equipment power consumption may be expressed in Watts. If so, its contribution to the load in VA can be found by multiplying its load current by its supply voltage. Alternatively its power consumption in Watts can be divided by its stated Power Factor to reveal its VA load. Manufacturers frequently overstate their equipment consumption by 20% or so to ensure the installer provides an adequate supply; however this over-rating cannot be relied on, and if in doubt the load should be measured.

This measurement activity can form part of the overall site survey. This should include installing portable measuring and monitoring equipment to record information about the load over a period of time. The period depends on the site situation; for example it would be misleading to monitor an office network over a weekend when very few staff have their PCs on.

The nature as well as the size of the load should be considered. Although UPSs are generally resilient, certain load types do present challenges which must be allowed for. These include blade servers, fluorescent gas



discharge lighting, motors and compressors, air conditioning equipment and laser printers. These can all draw high currents during normal operation, and even higher inrush currents during start-up. This may overload the UPS, causing a transfer to bypass.

Blade servers also impact UPSs in another way. Unlike much equipment with a lagging power factor, blade servers present a leading power factor. As these servers are powerful and increasingly popular within computer installations, the critical load's overall power factor may become leading. This presents a major problem with legacy transformer based UPS systems. For example a 300 kVA UPS requires derating by 24% for a 0.9 leading power factor. By contrast, a modern transformerless 300 kVA does not derate at 0.9 leading power factor.

If a three-phase UPS is supplying

a load with single-phase components, these components should be distributed as evenly as possible between the phases to allow the capacity of the UPS to be optimally utilized. A balanced load is also presented to the mains or, if installed, the generator if the UPS is bypassed. Although modern UPS systems can cope with phase imbalance, the load on any single phase must never exceed 33% of the total UPS loading..

When all the load information has been collected, measured and collated, the required UPS capacity will become apparent. It is normal practice to add contingency capacity of typically 20% to this value. Additionally it is essential to carefully consider the site's future expansion plans and allow for these in the UPS configuration accordingly. Most UPS manufacturers offer modular rackmounting UPS systems to allow scalability; A modular system's total output is the sum of all its component

UPS Details	Traditional (2 x 120kVA) 120kVA N+1	Modular (4 x 40kVA) 120kVA N+1
UPS Load (%)	50	75
UPS Efficiency (%)	91	96
Critical Load (kW)	96	96
Total UPS Input Power (kW)	105.5	100.0
Total UPS Heat Loss (kW)	9.5	4.0
UPS Losses – Cost per Year*	£6,521	£2,747
Cooling Cost per Year*	£2,152	£907
Total Cost per Year*	£8,673	£3,654
5 Year Saving	-	£25,095
CO ² Reduction over 5 Years	-	137.6 Tonnes (212 Trees**)

modules'. For such systems, the only initial requirement is to allow sufficient racking space, as more rackmounting UPS modules can easily be added when site expansion demands extra capacity.

As mentioned at the start of this article, the load's criticality will also influence the final decisions on the UPS's size and configuration. A small minority of users will prefer the initial capital savings of a capacity system – that is, a system with enough capacity to fully support its load as long as none of its constituent components or modules fail. If a failure does occur, the only solution is to immediately transfer the load to bypass, where it will be fed from the raw mains supply. Consider, for example a load of 270 kVA supplied by three 100 kVA units configured in parallel. Under normal circumstances, each unit will be supplying about 90 kVA, but if one module fails the other two will be called upon to

supply up to 135 kVA each. This will substantially overload them, invoking a switch to bypass.

In practice, most applications today demand a degree of resilience to failure from their UPS system. This means that the UPS should continue to fully support the load even if one or possibly more modules should fail. This redundant arrangement is more precisely known as an N+1 redundant system. 'N' represents the number of modules required to fully support the load, and '1' is for the single redundant module. If the application warrants it, more than one redundant module can be supplied to create an N+n redundant configuration. 'n' is the coefficient of redundancy. These guidelines allow users or design consultants to specify a UPS capacity which allows for the conditions prevailing on the user's site together with considerations of the resilience to failure required. This decision can then be added to other selection

criteria including the UPS's efficiency and running costs, its topology, its upgradeability, its size and weight, its flexibility of battery configuration and battery autonomy and its serviceability.

Further issues such as cost, the reputation of the UPS supplier and the availability of references for existing installations are important as well. Any reputable UPS supplier will be able to help with site surveys, discuss the criticality of the load and other factors, and advise on UPS configuration and sizing accordingly.

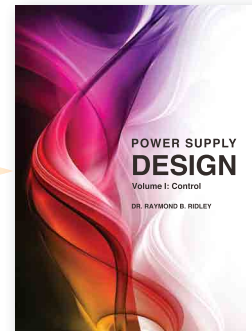
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An excerpt from the introduction . . .

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The harsh reality of power supply development is that they rarely behave in an expected manner, or in the manner that simulators dictate. Therefore, you must build hardware, then test and measure as quickly as possible to uncover problems. This book is intended to help you get there faster by providing key information, and showing where the issues lie.

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SPECIAL REPORT: POWERING COMMUNICATIONS

PSD NORTH AMERICA
Power Systems Design: Empowering Global Innovation



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PMBus COMMUNICATIONS

Promotes programmable power-conversion systems

By Patrick Le Fèvre

Digitally controlled power converters that embody power management subsystems and PMBus communications in telecoms applications makes it easy to assemble sophisticated hardware that suits a variety of distributed power applications.

The ability to monitor the status of a power domain and fine-tune its configuration in real time lays the foundation for energy-saving schemes that will be especially attractive in systems that experience large load swings, such as datacom and telecom centers. A PC-compatible package, with its graphical user interface, extends ease-of-use to the software development realm, freeing users to experiment with alternative power-converter configurations.

With its low-cost SMBus physical hardware layer and a standard command set that specifically addresses the power-conversion environment, PMBus™ provides system architects with a simple, robust and highly flexible platform that seamlessly communicates with any compatible power-system component – from AC-DC front-ends to variable-speed

cooling fans. While many legacy components can only report rudimentary status information, fully exploiting the opportunities made available by the PMBus requires the intermediate-bus and point-of-load converters, which deliver load currents in a typical intermediate-bus-architecture (IBA), to include comprehensively capable measurement and control subsystems.

Mostly built using mixed-signal silicon processes, today's digitally controlled power converters embody these additional hardware elements alongside the core PWM controller at negligible additional cost. As a result, system architects can construct sophisticated hardware schemes with unprecedented ease – the major challenge now being to develop supervisory and control software that maximizes system reliability and energy

efficiency. Such schemes require the ability to reconfigure the power converters 'on-the-fly', but crucially for more modest applications, PMBus mandates a 'set-&-forget' mode where the converter behaves much like any other programmable component. This allows, for instance, one programming step to write its non-volatile memory with user-defined parameters, such as output voltage and current-limit values, in addition to any power-rail sequencing delays required by multi-rail logic components.

Clearly, practicality and simplicity are key factors in the PMBus' success. Mirroring V2 of the SMBus specification, the bus comprises the clock and data lines SMBCLK and SMBDAT, which facilitate bidirectional communications between a bus master that initiates data transfer and the slave that responds when it recognizes its unique 7-bit address. PMBus

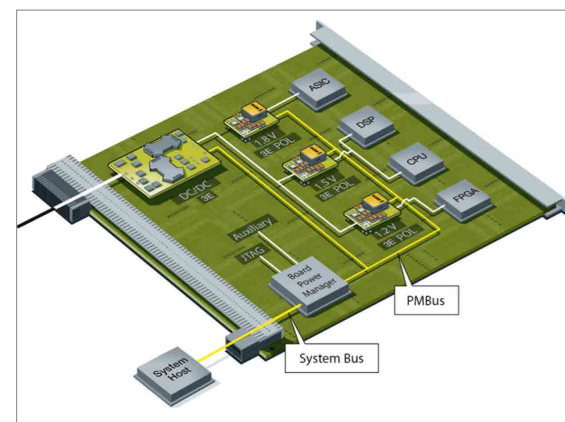


Figure 1: In a typical rack, the system host provides overall control for each board's power system via a Board Power Manager.

adds two signal lines whose use is optional: SMBALERT#, an interrupt line to inform the system host that a device requires service; and CONTROL, which turns devices on and off in conjunction with PMBus commands.

Electrically similar to I2C, a PMBus link is almost always confined to a single board. It may optionally communicate with other boards using the backplane-level system bus that uses the system designer's choice of network technology. Figure 1 shows the structure of a rack-mount board in a typical IBA environment, where local board power-manager logic most often forms a physical bridge between the onboard PMBus link and the backplane's system bus.

The system host, which handles overall power control and management tasks, is the primary node on the system

bus. The host could be an embedded system and/or external intelligence, such as a PC that might usefully link into the local enterprise network. Depending upon the degree of autonomy that the designer considers appropriate for

individual boards, the board power manager might range from a simple bridge built using some leftover gates in an FPGA to a microcontroller with on-chip protocol conversion.

Standard command language eases programming

Experience with long-standing communications protocols such as the test-&-measurement industry's IEEE-488.2 and SCPI (standard commands for programmable instrumentation) demonstrates that a well-developed standard command language is hugely influential in winning over designers wishing to simplify, secure and future-proof their projects. Again, the key is simplicity without compromising flexibility.

The full list of standard commands appears in Part Two – Command Language – of the PMBus Power System Management Protocol

Specification. With the exception of the last two codes, 0xFE and 0xFF, which form the first byte of a pair of two-byte extended-functionality commands, PMBus commands are single-byte entities. Accordingly, the format allows for 256 commands, each of which falls broadly into one of these categories: control, output, fault-limit, fault-response and time-setting commands; read-only status, monitor and identification commands; group and supervisory commands; and device- and manufacturer-specific commands.

The great majority of the underlying functions within these groups are self-explanatory and generally applicable, such as setting power on/off delays and ramp times to implement power-rail sequencing without requiring any external hardware. But among the normal device-specific functions such as trimming calibration data, the last of these groups makes it possible to program aspects of the target hardware that are unique to a particular device. Such abilities may include altering the PID (proportional, integral and derivative) filter constants that control a digital converter's dynamic responses, or varying the dead-time period between the control and sync FETs switching in a buck converter to minimize losses with changing line-&-load conditions. Given suitable hardware, these capabilities are

almost invariably new and offer the possibility of dynamically fine-tuning a converter's responses to suit its current set of operating conditions.

At a higher level of control, established techniques such as dynamic bus voltage control that require extensive support circuitry in analog power converters become easy to implement when using PMBus-compatible digital converters. This energy-saving scheme involves intelligently reducing the intermediate-bus voltage when load currents are relatively small, which minimizes down-conversion losses in the multiple point-of-load converters that regulate the load voltages. As the load current level rises, supervisory software commands the intermediate-bus converter to increase its output voltage to ensure sufficient headroom for the point-of-load converters. This approach particularly suits systems that experience large swings in load current levels, such as those systems that handle networks and typically are highly dependent on traffic demand. These types of systems will often shutdown entire circuit blocks to save energy, when demand is low. PMBus greatly simplifies implementing the power control aspect of these systems.

Evaluation kits ease hardware and software design

The message-exchange

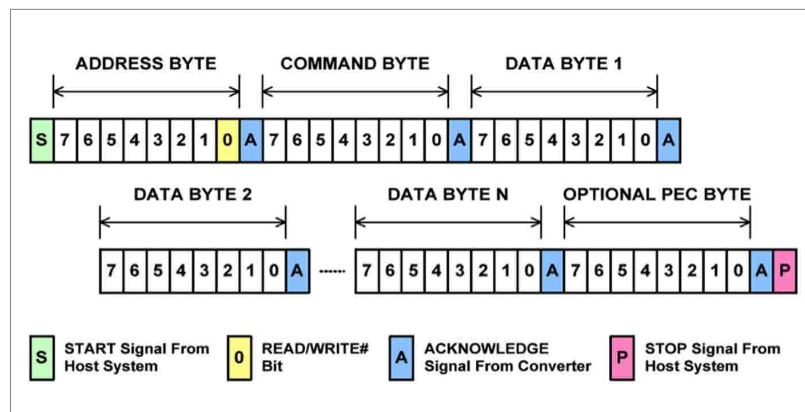


Figure 2: PMBus uses a simple and robust message-exchange mechanism

mechanism that PMBus uses generally consists of a 'start—target device address—command—data—stop' sequence. The number of data bytes that follow any command depends on the nature of

the current exchange, with receiving devices asserting an acknowledge signal for every transferred byte.

The sequence can optionally terminate with a PEC (packet error checking) byte as Figure 2 shows.

In the end system, dedicated hardware assumes responsibility for these exchanges, leaving developers to find a way of communicating with prototype

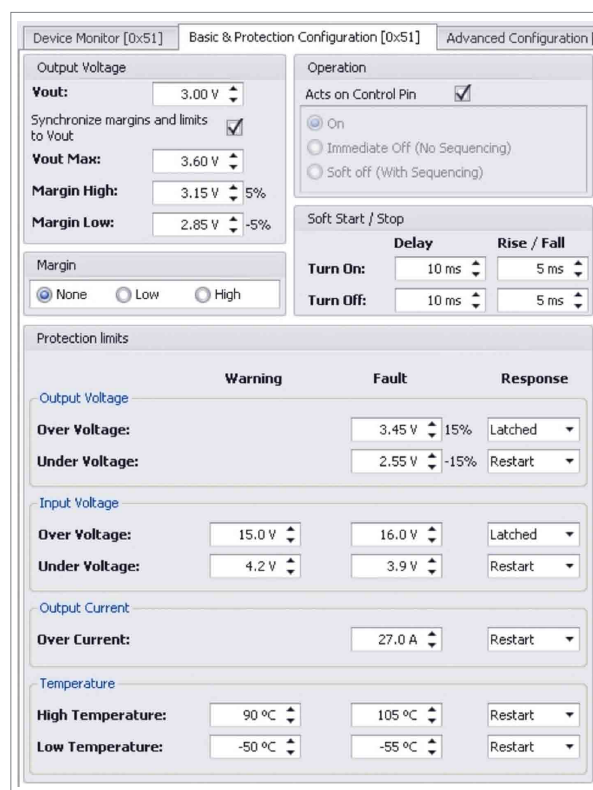


Figure 3: A GUI simplifies PMBus-device set-up tasks.



Figure 4: 3E-design-kit

hardware and evaluating alternative power-converter configurations. One approach that is proving popular uses a Windows PC to host a graphical development environment that communicates with an evaluation board via a USB-to-PMBus adapter. The evaluation board accommodates a selection of PMBus-compatible intermediate-bus converters and point-of-load regulators that designers can choose to closely replicate their target environment, while the graphical development environment vastly simplifies device set-up as the example panel in Figure 3 shows.

This example environment from 3E GUI Gold Edition specifically suits Ericsson's 3E family of digital intermediate-bus converters and point-of-load regulators, but unusually, it is also capable of communicating with any PMBus-compatible device. Furthermore, its facilities include a PMBus transaction log that records and analyzes message exchanges to speed troubleshooting.

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LTPoE++ EXTENDS PoE

90W with reliable and easy-to-use standard

By Heath Stewart

Power over Ethernet, or PoE, is an increasingly popular way to deliver both power and data over existing Ethernet cable, thus freeing applications from the constraint of AC-power proximity.

As the number PoE solutions has grown, so has the applications' appetite for power. A new proprietary standard, LTPoE++™, satisfies this hunger by extending the PoE and PoE+ specifications to 90W of PD delivered power. LTPoE++ also dramatically reduces engineering complexity in power sourcing equipment (PSEs) and powered devices (PDs) when compared to other power-expansion solutions. Plug-and-play simplicity and safe, robust power delivery are hallmarks of LTPoE++. The capabilities of this standard expand the field of Ethernet-powered applications by several orders of magnitude, enabling entirely new classes of PDs, such as power-hungry picocells, base stations or heaters for pan-tilt-zoom cameras.

The IEEE standard defines PoE terminology, as shown in Figure 1. A device that provides

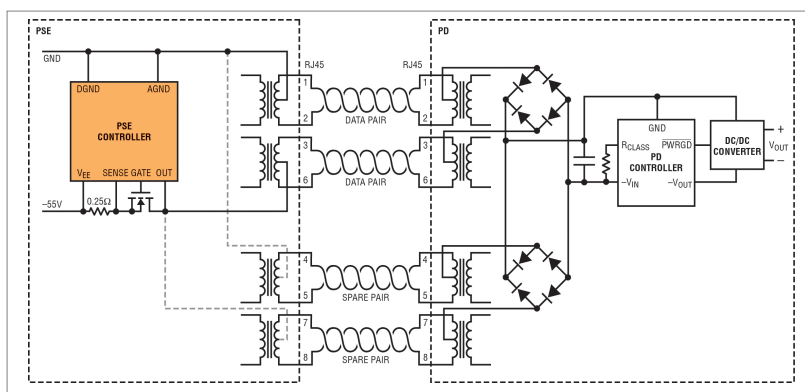


Figure 1: Typical PoE system

power to the network is known as a PSE, or power sourcing equipment, while a device that draws power from the network is known as a PD, or powered device. PSEs come in two types: endpoints (typically network switches or routers), which send both data and power, and midspans, which inject power but pass data through. Midspans are typically used to add PoE capability to existing non-PoE networks. Typical PD applications are IP phones, wireless access points, security cameras, cellular femtocells, picocells and base stations.

The IEEE PoE+ specification specifies backward compatibility with 802.3af PSEs and PDs. The PoE+ specification defines Type 1 PSEs and PDs to include PSEs and PDs delivering up to 13W. Type 2 PSEs and PDs deliver up to 25.5W.

LTPoE++ Evolution

The IEEE PoE+ 25.5W specification had not yet been finalized when it became clear that there was a significant and increasing need for more than 25.5W of delivered power. In response to this need, the LTPoE++ specification reliably

allocates up to 90W of delivered power to an LTPoE++ PD.

The LTPoE++ specification provides reliable detection and classification extensions to existing IEEE PoE protocols. LTPoE++ is backward compatible and interoperable with existing Type 1 and Type 2 PDs. Unlike other proprietary power-extending solutions, Linear's LTPoE++ provides mutual identification between the PSE and PD. LTPoE++ PSEs can differentiate between an LTPoE++ PD and all other types of IEEE compliant PDs, allowing LTPoE++ PSEs to remain compliant and interoperable with existing equipment.

LTPoE++ PSEs and PDs seamlessly interoperate with IEEE 802.3at Type 1 and Type 2 devices. Type 1 PSEs generally encompass 802.3af functionality at and below 13W. Type 2 PSEs extend traditional PoE to 25.5W.

- Type 1 PSEs will power all Type 1, Type 2 and LTPoE++ PDs with up to 13W.
- Type 2 PSEs will power Type 1 PDs with up to 13W and provide 25.5W to Type 2 and LTPoE++ PDs.
- LTPoE++ PDs can power up with limited functionality even when attached to traditional Type 1 and 2 PSEs.
- LTPoE++ PSEs interoperate with Type 1 and Type 2 PDs. LTPoE++ PDs are powered to the designed limit of the

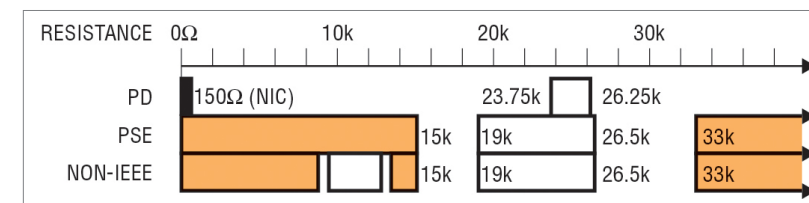


Figure 2: IEEE 802.3at signature resistance ranges

LTPoE++ PSE. When an LTPoE++ PD is identified, the PD will be powered up if the PSE power rating meets or exceeds the requested PD power. For example, a 45W LTPoE++ PSE can power both 35W and 45W PDs.

and destroying non-PoE Ethernet devices.

The following rules define any detection methodology for the highest levels of safety and interoperability.

- Priority 1: Don't turn on things you shouldn't turn on.
- Priority 2: Do turn on things you should.

Linear Technology PSEs provide extremely robust detection schemes utilizing four-point detection. False positive detections are minimized by checking for signature resistance with both forced-current and forced voltage measurements.

IEEE-Compliant PD Detection
LTPoE++ physical detection and classification is a simple, backward-compatible extension of existing schemes. Other power extension protocols violate the IEEE specification, as shown in Figure 2, and risk powering up known noncompliant NICs. Any high power allocation scheme violating the IEEE-mandated detection resistance specifications risks damaging

LTPoE++ Advantages

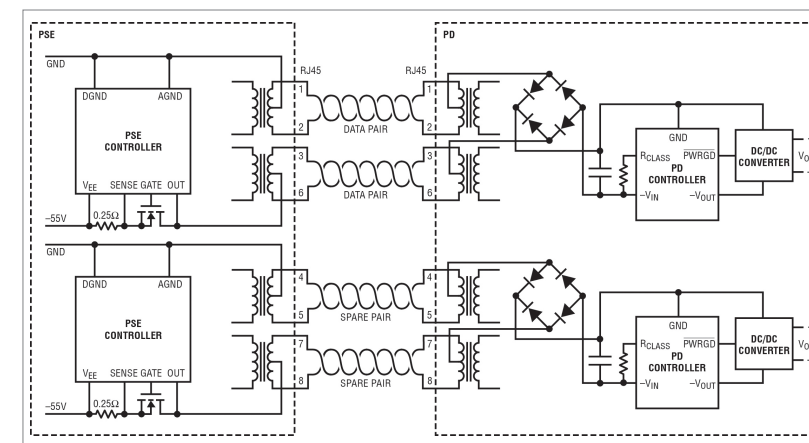


Figure 3: The expensive way to extend PoE+ power. Dual Type 2 PD provides more power than standard PoE+ PD, but it also doubles the cost and component count.

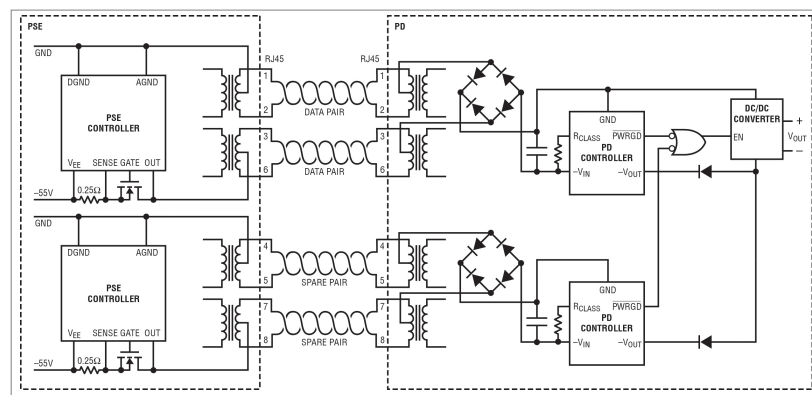


Figure 4: Less expensive, but flawed, alternative for extending PoE+ power. This scheme is similar to the dual Type 2 set-up shown in Figure 3, but a diode ORed power sharing architecture reduces some of the cost by eliminating one DC/DC converter in the PD. However, due to intrinsic reductions in surge protection tolerance, these solutions rarely meet PD design goals.

Standard PoE PSEs use two of the four available Ethernet cable pairs for power. Some power-extending topologies use two PSEs and two PDs over one cable to deliver $2 \times 25.5\text{W}$. This “dual Type 2” topology is shown in Figure 3. The main problem with this strategy is that it doubles the number of components, thus doubling PSE and PD costs. Additionally, robust design considerations require two DC/DC converters at the PD, one for each component PD, where each DC/DC converter is a relatively complex flyback or forward isolated supply.

One of the DC/DC converters in a dual Type 2 set-up can be eliminated by ORing the PD's output power as shown in Figure 4. This approach still requires two PSEs and two PDs, with the associated cost and space disadvantages. The voltage drop incurred by the power ORing

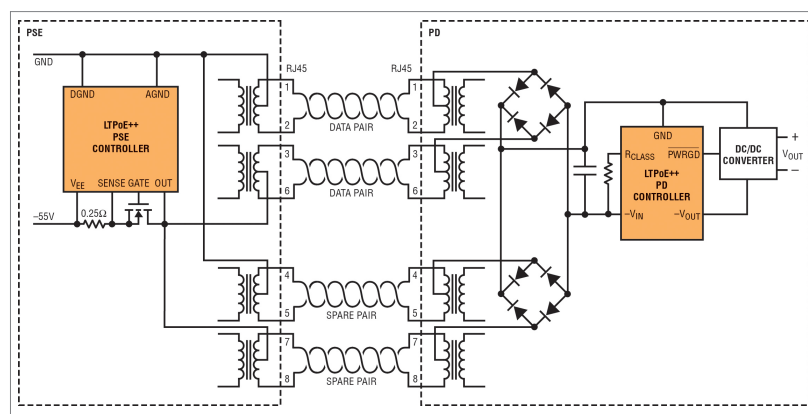


Figure 5: The LTPoE++ architecture is the only PoE power-extending solution that provides 90W at the PD while keeping complexity and costs in check.

diodes might be considered a fair trade-off for the savings gained by using a single DC/DC converter. In most cases diode ORed power sharing architectures remain attractive until surge protection testing begins. Due to intrinsic reductions in surge protection tolerance, these solutions rarely meet PD design goals.

In contrast, LTPoE++ solutions, as shown in Figure 5, require only a single PSE, PD and DC/

DC converter, resulting in significant board space, cost and development time advantages.

LLDP Interoperability and Options

During selection and architecture of a PoE system, many PD designers are surprised to discover the hidden costs of Link Layer Discovery Protocol (LLDP) implementations. LLDP is the IEEE-mandated PD software-level power negotiation. LLDP requires extensions to standard Ethernet stacks and can represent a

significant software development effort. Unfortunately the open-source community effort to provide LLDP support is still in its infancy.

While Type 2 PSEs may optionally implement LLDP, fully IEEE-compliant Type 2 PDs must implement both physical classification and LLDP power negotiation capabilities. First, this places the burden of LLDP software development on all Type

2 PDs. In addition, designs are complicated by the dual power requirements inferred by the LLDP requirement. Specifically, the PD-side processor must be fully functional at the 13W power level and then have the ability to negotiate, via LLDP, for the delivery of additional power. Clearly this requirement can increase development and system costs and complexity.

LTPoE++ offers LLDP implementation options. LTPoE++ PSEs and PDs autonomously negotiate power level requirements and capabilities at the hardware level while remaining fully compatible with LLDP-based solutions. In short, LTPoE++ gives system designers the choice to implement or not implement LLDP. Proprietary end-to-end systems may choose to forgo LLDP support. This creates time-to-market advantages while further reducing BOM costs, board size and complexity.

Power Claims Demystified

PoE power paths can be divided into three main components: the power produced by the PSE, the power delivered to the PD and the power delivered to the application. Claims of PSE and PD power delivery capabilities must be carefully examined before useful comparisons can be made. One vendor may describe the power as delivered by the PSE, another the power delivered to the PD, while the PD designer

typically cares about power consumed by the application.

Although the PSE power metric is the least useful of the three, it is the one most often cited in marketing materials. PSE power is generally defined as the power delivered at the PSE end of the Ethernet cable. Power capability is sometimes further distorted when vendors specify power at the maximum rated voltage, which is rarely achieved.

PD power or “delivered power” is the power delivered to the PD end of the Ethernet cable, prior to the diode bridge. Quoted PD power is a more useful metric than PSE power, since it must account for significant losses over 100 meters of CAT-5e cable. PD power claims make no assumptions about the application's DC/DC converter and diode bridge efficiencies, which are unknown to PSE and PD silicon vendors.

A PD designer is most interested in the power delivered to the application when all system effects are considered, including the resistance of the Ethernet magnetics, diode bridge voltage drops and DC/DC converter efficiency.

This metric, although the most telling, is the most difficult to accurately specify.

PSE Availability

Linear Technology is committed to LTPoE++ technology and provides an entire family of PSE and PD solutions. A full family of PSEs, spanning 1- to 12-port solutions is now available.

Conclusion

LTPoE++ offers a robust, end-to-end high power PoE solution with up-front cost savings. Combined with Linear Technology's excellent application support, proven delivery record and reputation for reliability, LTPoE++ is the most comprehensive high power solution on the market. LTPoE++ systems simplify power delivery and allow system designers to concentrate their design efforts on their high value applications.

Author: Heath Stewart
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www.linear.com

LOW-POWER NETWORKED SOLUTION

At home with the wireless internet

By Colin Faulkner

All households and businesses are under pressure to fulfil the twin ideals of reduced energy consumption and reduced costs.

There have been many advances in building technology such as double glazing, and roof and wall insulation, which improve the loss of energy, but to date, very little has been done to minimise consumption at the source. Conventional heating and lighting systems are not much more sophisticated than piling more wood on the fire if it's cold! Conventional thermostats and lighting systems often operate at a whole house level and provide uneven distribution of comfort around the building.

This is true for both residential and commercial buildings. One reason for this condition is "installation costs". It is possible to wire up control signals to individual lamps or to place thermostats in every room, but in practice, the cost of installation is prohibitive. Even for a new build, cabling is expensive to install, making it uneconomic to specify improved control. However, the

"Internet of Things", particularly when connected with wireless technologies, is set to change the situation by offering a means to install many sensors and actuators at very low cost.

IPv4 (Internet Protocol version 4) as the transport mechanism of choice for data on the internet has served the world well for many years, but has been restricted from dramatic expansion by the limited number of IP addresses. This has recently been addressed by the introduction of IPv6 which now offers around 5×10^{28} addresses for every person on the planet. This is plenty for any currently conceivable control systems and in principle, any device around the world could be given a unique IP address. If this can be applied to lighting and climate control within buildings, we have a mechanism to realise complex control systems. The issue, of course, is how to communicate with the devices in a cost-

effective fashion and this is where a wireless network comes into play. What is required is a low-power networked solution specially designed for building automation solutions.

The IEEE802.15.4 standard provides a radio and Media Access Control (MAC) platform designed for low-power wireless networks, including systems where devices are connected together in a tree or mesh arrangement. These techniques allow messages to bounce from node to node, making their way across the network. If a building has these nodes installed, in every light fixture, for example, then it ensures that all devices are within range of one of the radios.

One of the most common standards using IEEE802.15.4 is ZigBee, which defines both the networking to connect devices together and "profiles" for interoperability, allowing devices

from different manufacturers to work together. As an alternative to ZigBee and to provide IP connectivity to all nodes, the Internet Engineering Task Force (IETF) has developed a standard named 6LoWPAN. This is designed to allow IPv6 communications over wireless networks with low bandwidth, such as IEEE802.15.4. 6LoWPAN describes two main techniques; i) fragmentation of large IP packets so that they can be transmitted within the 128 byte payload of IEEE802.15.4 and ii) compression of the IP headers within the wireless network, again in order to provide as much payload space as possible. 6LoWPAN therefore is the key enabler in achieving our dream of IP connectivity to all devices in the home.

However, there are other parts of this picture – we still require methods to network devices together and to provide a common way of operating so that some kind of interoperability is possible. NXP has solved this problem with the creation of JenNet-IP, which provides the optimum combination of standards-based and proprietary solutions to provide ready-to-use networked wireless solutions. The structure of JenNet-IP is shown in Figure 1.

JenNet-IP uses NXP's proven JenNet networking layer to provide the connectivity between devices. This is a tree-based networking layer, with the capability to create networks of up to 500 nodes. It has one of the key features of a so-called Mesh network, in that it allows

robustness and reliability which is essential to successful deployments. It also includes techniques for applying a high level of data security using the 128-bit AES encryption built into IEEE802.15.4. This ensures that networks cannot be hacked maliciously and that they remain unique to their owner and do not overlap with adjacent ones. In addition to providing true IP connectivity from the internet to devices in the home, JenNet-IP also implements a gatewayless mode of operation. This allows the system to carry on working even if the internet gateway fails. It also allows the sale of starter kits comprising just a few devices and a remote control in order to allow consumers to try out and become familiar with the technology before investing in a full internet connected system.

self-healing. If one of the established routes fails – for example, due to a faulty router – the network will detect this and will automatically try to re-establish alternative routing through a nearby node, providing a high degree of

One of the other important features is the provision for interoperability and device control. This is implemented in a simple application layer named SNAP (Simple Network Application Protocol). This uses the concepts of the common SNMP protocol but has been architected to provide a solution appropriate for low-cost embedded devices. Put simply, it provides a small database of device characteristics, such as name, group membership, and capabilities (On, Off, Dim, Up/Down, etc/).

This can then be interrogated

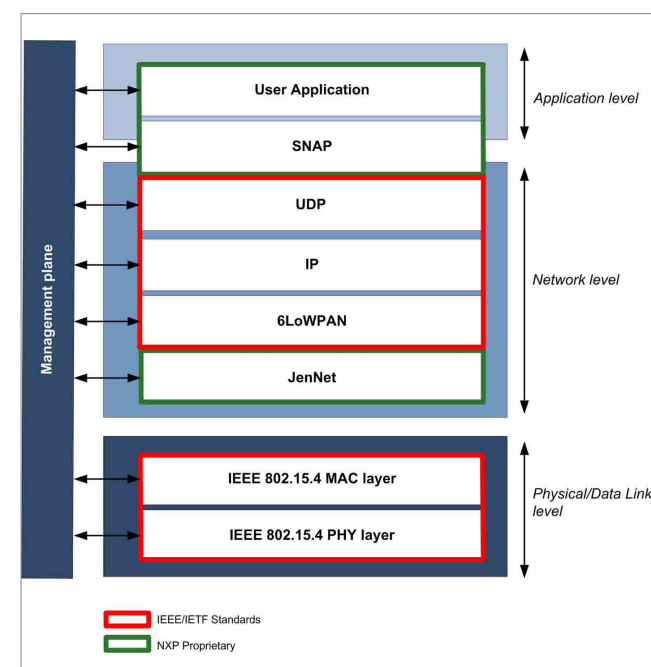


Figure 1: JenNet-IP Stack build-up

and manipulated by external devices. So a SNAP application will run on a bulb and this can then be controlled by another SNAP application running on either a remote control device, or on a device such as a tablet PC connected to the internet. In this way, individual bulbs can be controlled and put into groups, enabling the provision of lighting “scenes” – for example with just one lamp illuminated for reading or dimming the lamps close to the TV for watching a film. With wireless connectivity enabling implementation of complex control systems with minimal installation costs, seamless integration with the internet, and a powerful and flexible means of providing interoperability, JenNet-IP goes a long way to facilitating the systems needed to maximise energy efficiency within all sorts of buildings.

Installation costs are minimised as the only wiring required is power which is already required for most devices. Switches and remote controls can be easily battery-powered or even use energy harvesting. The use of IP to all nodes ensures that the wireless system can interface directly with existing or new building management systems which can interact with the data generated to accurately control light levels, temperature and humidity to ensure user comfort with a minimum of energy usage. For example, in an office system, if each lamp

can be individually controlled, it becomes straightforward to dim lamps where the exterior ambient light level means that little or no additional light is required. Likewise, at home, with groups and scenes, there is no need to have unused lamps on, again minimising energy usage.

In summary, JenNet-IP is a low power wireless networking system that provides IPv6 connectivity to any device within buildings, providing flexible individual control and monitoring of lights and heating, without the huge expense of cabling installation, hence making an important contribution to the efficient use of energy.

The Wireless capability is fully integrated into the bulbs themselves, using NXP's GreenChip solution which combines the JN5148 wireless microcontroller with the TEA1721 power supply devices and SSL2108 (for LED lamps) or UBA2028 (for compact fluorescents) into the body of the bulb itself. The lamps

can be set up and controlled individually or in groups, and scenes comprising different light levels on each lamp can be set, for example for reading or for watching TV. The remote control is a full member of the network and can control devices within it, but the beauty of the IP provision is that external devices can easily control the system. This is demonstrated by the use of an Android application running SNAP and communicating into the network via the Wi-Fi router and also by the provision of a web interface, again manipulating the SNAP databases. The smart plug devices allow both on-off control of equipment such as a TV or monitor, but also monitoring of energy usage. This allows users to see exactly where their energy usage is going and to take steps to minimise consumption.

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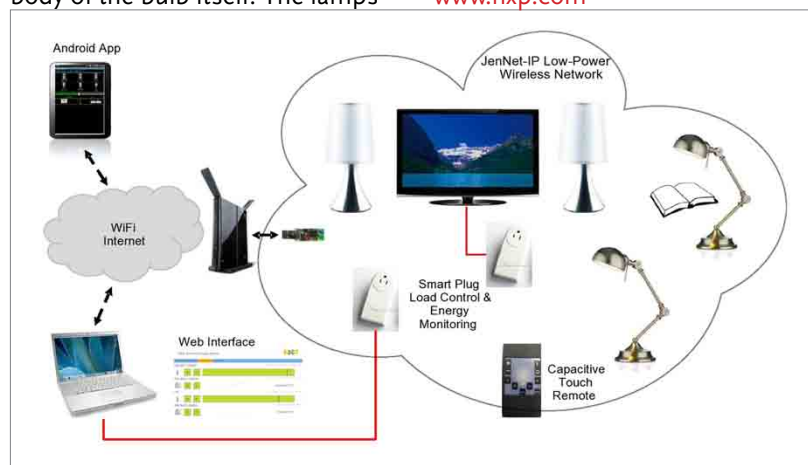


Figure 2: JenNet-IP demonstrator configuration

COMMUNICATED ADAPTIVE DIGITAL CONTROL

Efficiency, reliability, & time-to-market benefits

By David New

Real-Time Auto-Compensation Technique Enables More Versatile and More Efficient Power Systems while Reducing Design Overhead

Experienced power supply design engineers know that specific power requirement of their power supplies are often not finalized until late in the design cycle, when the end product is close to completion. Or that the power supply's use may vary in the field depending on its user; this is especially true if a common platform is to be used with multiple end configurations. Additionally, today's power supplies are subjected to increasing efficiency requirements and aggressive cost targets. Each of these cases present challenges to design engineers; fortunately there is a technology that is able to help.

This article discusses a new approach to power supply design that is based on a real-time self-adaptive loop compensation technique developed by Powervation; this

unique technology is called Auto-Control®. Using an adaptive compensation technique that operates in real-time allows the power supply controller to optimize the trade-off between dynamic performance and system stability on a cycle-by-cycle basis, and enables the use of efficiency improvement techniques that otherwise would require additional cost & complexity to implement. The self-compensating, adaptive approach relieves power supply designers of the burden of compensation, plant characterization, and reduces total design iterations. Additionally, Auto-Control provides a key advantage for designs that drive imprecise or variable loads, and addresses the challenges associated with power supply component parameter drift that occurs over temperature and time.

Power supply designers often develop power supplies that

are for general use, without knowing exactly how the design will be used in operation, and for platforms that will be used with multiple end configurations. In these cases, a design is developed to operate over a wide range of conditions, and both cost and performance are part of the overall compromise. Alternatively, for designs that are dedicated specifically for a single platform, cost optimization may be more obtainable. However, the process that engineers undertake to achieve this is time intensive, and iterative. Even with an experienced power supply design engineer, both cases can require a large amount of design effort and time spent to balance the various design trade-offs and to optimize key metrics where possible. Finding ways to shorten this development time allows a reduction in development costs, and minimizes lost opportunity

costs by bringing products to market quicker.

One approach that is able to shorten development time by eliminating and shortening some design steps, while improving system reliability, is to implement a real-time self-adaptive compensation technique. By constantly monitoring the output of the converter, Powervation's Auto-Control self-compensating controllers adjust the PID coefficients of the loop (Figure 1), on a cycle-by-cycle basis to optimize the converter's performance for that condition, and continues to do so, even as conditions change. Auto-Control allows the controller to continuously modulate the bandwidth of the loop to optimize performance, and eliminates the need for power supply engineers to build in the additional design margin needed for fixed compensation-based designs.

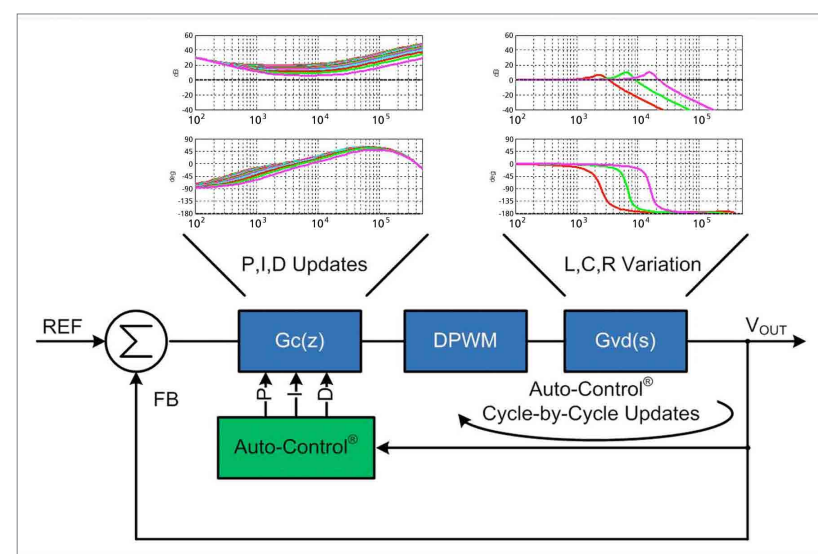


Figure 1: Auto-Control Adapts to Power Stage Variations

The self-adaptive compensation technique: removes the need for the designer to invest large amounts of time attempting to anticipate worst-case conditions, allows designers to reduce some engineered design margin – and the cost associated with the design margin, eliminates the iterative manual tuning of the design's compensation loop, and provides a solution that is optimized over a wide range of operating conditions.

Auto-Control Manages Changes in Power Stage

There are several elements that can change in a power supply that Auto-Control's real-time adaptive compensation is able to manage. Some of these include:

- Changes in output impedance (e.g., when using phase add/drop)
- Component tolerances (i.e., output inductor and capacitors)

-Component aging
-Temperature
-Variations in load (e.g., manufacturer and capacity size of memory DIMMs)
-Unknown load (e.g., power modules designed for the general market, where the load may vary greatly over users).

Auto-Control provides benefits when dealing with variations such as component tolerances and for designs that may need to power a wide range of loads. Other variations occur over time when the system is in use. Some of these, such as component aging and changes over temperature occur somewhat slowly; while others, such as phase add/drop, can occur very rapidly. Auto-Control's real-time adaptive compensation is able to manage all of these variances by modulating the bandwidth according to the supply's current mode-of-operation and eliminates the need to over-design the hardware for the worst-case mode-of-operation. All of this is done internal to the controller without input or intervention from the user.

In Figure 2 we see Powervation's PV3012 control IC use automatic phase add/drop; in this two-phase converter, PV3012 transitions the converter from single-phase mode to dual-phase mode as it crosses the 15 A threshold (solid black line). This is done to maximize efficiency. Without the ability to

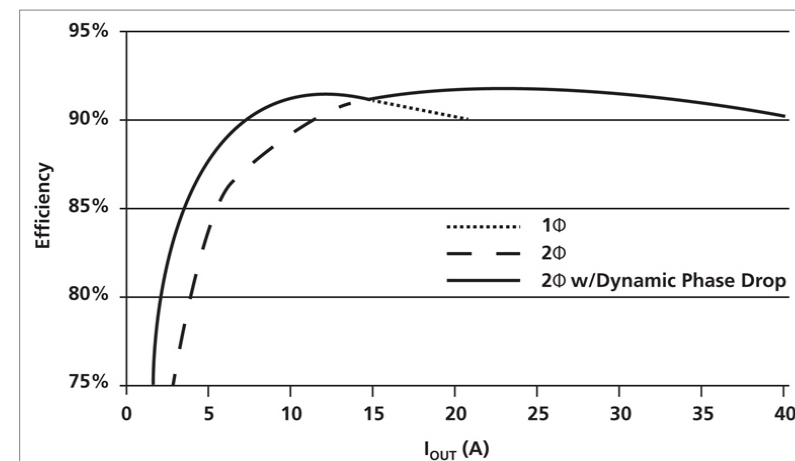


Figure 2: Efficiency Improvement Using PV3012's Automatic Phase Add/Drop

dynamically perform phase add/drop, controllers follow the two-phase curve (dashed line) from 0 to 15 A, thus running at a lower efficiency in that range.

While the advantages of using phase add/drop to improve efficiency are clear, the technique is not without challenges; adding and dropping a phase changes the output impedance of the multi-phase converter, and thus can affect the converter's transient response and require a modification of the converter's

output filter (e.g., an increase in output capacitance to ensure sufficient bandwidth under all modes of operation).

Figure 3 shows a comparison of the transient responses of a fixed compensation converter (left) and a converter using Auto-Control (right); both using phase add/drop.

In the fixed compensation case, the loop and number of output capacitors has been optimized for two-phase operation (upper left). However, when a phase

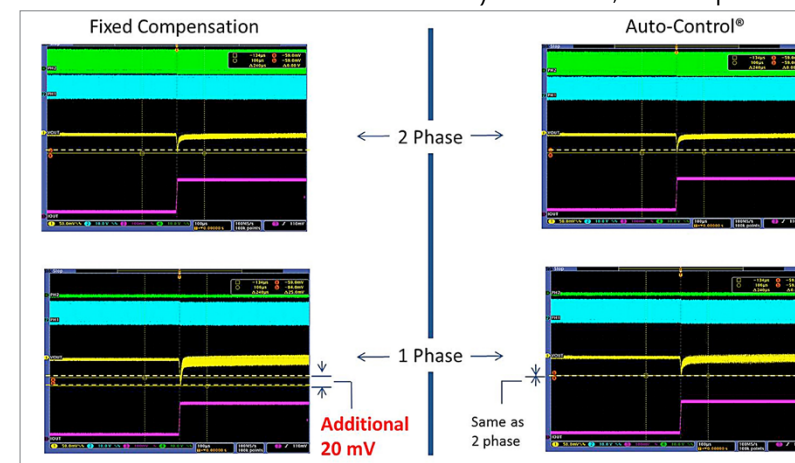


Figure 3: Transient Response Comparison

is dropped (lower left), we see a degradation in transient performance; in this case, an additional 20 mV of undershoot was found.

With the converter using Auto-Control, two-phase operation (upper right) provides a similar transient response as the fixed compensation converter while using the same output filter. However, when the converter transitions to single-phase mode, Auto-Control has re-tuned the system, and the transient performance is maintained; there is no additional undershoot. Figure 4 illustrates the gain-frequency curves for the examples shown in Figure 3. In dual-phase mode, both designs follow the green line. In the fixed compensation case (red line), the bandwidth falls back to a lower value in single-phase mode; this is a result of the change in the converter's output impedance, and the inability of the fixed compensation system to react. For the converter using Auto-Control (blue line), the bandwidth has also been reduced (a result of shedding a phase), but Auto-Control's adaptive compensation has increased the bandwidth beyond that seen in the fixed compensation case (red line), thus maintaining the converter's transient response without modifying the output filter.

Real-time adaptive control brings a new versatility to designs, and enables designers several

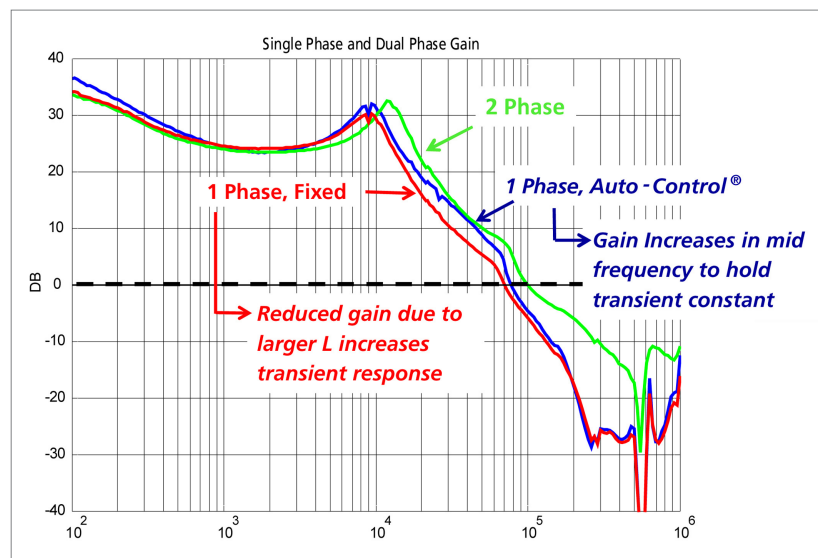


Figure 4: Auto-Control Adjust Gain to Maintain Transient Performance

advantages related to efficiency, reliability, and time-to-market.

Power supplies that incorporate Auto-Control’s real-time adaptive

compensation are able to maintain stability over a wide range of operating conditions (e.g., varying or unknown loads) and modes of operation (e.g., phase add/drop) without relying on modifications to the output filter that would result in higher solution costs or lower performance. Furthermore, reliability is improved as Auto-Control optimizes its behaviour to adapt to changes and variables such as component tolerances, degradation and aging, and variance over temperature.

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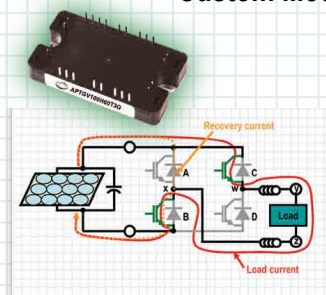
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POWER DESIGN REMAINS CORE COMPETENCE IN SATELLITE INDUSTRY



By David G. Morrison, Editor, How2Power.com

In the communications equipment industry, many companies that previously designed power systems in-house, have outsourced this engineering work to other vendors. But in one segment of this industry power system design is still considered a core competency, and too vital to the success of the end product to delegate to others. The companies inhabiting this corner of the communication field are the satellite manufacturers.

Their equipment must operate in the hostile environment of space for well over a decade without faults or failures that would result in satellite downtime. A satellite's power system must be optimized for highest efficiency and lowest power losses, in large part to minimize the system's size and mass. Naturally, power electronics engineers play a critical role in the development of these power systems, but so too do the mechanical engineers who package them and address the associated thermal issues. Also, essential to the design are the component and process engineers, who qualify all the parts

and assembly techniques used to build the power system. Therefore, power electronics engineers in the satellite equipment industry are working in a very collaborative environment.

In this design environment, new power components and design techniques are adopted very methodically, and only as needed to enable the needs of new satellite programs or deal with component obsolescence. The development of a new power system can be a multi-year effort that ideally must anticipate the needs of the next satellite program. Despite the high-rel nature of this work and the long list of application requirements,

power system designers in this field must still manage costs in their designs.

One engineer who has a bird's eye view of all these design challenges is Robert Lyon, a systems engineering manager at Space Systems/Loral, a leading manufacturer of commercial satellites based in Palo Alto, California. Lyon was previously the systems architect for SS/L's Super Power Subsystem (SPS), which tripled the amount of power that the company's satellites could generate to satisfy the needs of newer applications. Lyon's descriptions of the issues that drive power system design

for satellites illustrate why there continue to be opportunities for power electronics engineers in this field. (For some examples of recent job postings, see the online version of this article.)

Long Life, Lack of Serviceability Are Design Drivers

Space Systems/Loral specializes in large geostationary satellites which orbit in a fixed position approximately 22,000 miles above the equator. In addition to radio and TV broadcasting, these satellites are used in VSAT (very small aperture terminal) applications. These include business-to-business applications such as a retail gas station using the VSAT equipment to transmit point-of-sale data.

According to Lyon, the discussion about power system design requirements for commercial, geostationary satellites begins with the issue of operating life.

"When we start talking about satellite anything, particularly the power systems, we have to recognize that these things are expected to last for at least 15 years on orbit and there is no ability to send the warranty truck out there to do a repair," says Lyon. "So the long life, high fault tolerance/high reliability requirement is tantamount to what we do."

As a result, Lyon says the number one design driver for the satellite power system is that it have greater than 15-year survivability.

This encompasses every part of the power system from the solar panels that generate the electricity to the batteries that store it to the power electronics circuitry that processes and regulates power for the on-board electronics (see the Figure 1 diagram in the online version of this article.)

But if long life is the first priority, mass and thermal considerations are a close second. "For these applications rockets can only lift a certain amount of weight, so every kilogram is very expensive. Consequently, there's a need to make sure that everything is very efficient from both a mass perspective and also a thermal efficiency perspective," says Lyon.

He adds that from the customers' perspective, the power system is simply overhead needed to run the equipment—what they're buying are the components that deliver content. In other words, they want to maximize the amount of communications hardware in the satellites, which means minimizing the mass of the power system.

The thermal issue is multifaceted. Power system components need to operate efficiently, with low power dissipation, so that they run cool, which leads to greater reliability and longer life. This applies particularly to the semiconductors in terms of keeping their junction temperatures low. However, the power dissipation of all the power system components is a concern

because of the difficulties of heat removal.

For example, because the equipment operates in a vacuum, convection cooling is not an option and all the heat generated within the electronics must be conducted out of the enclosure. In the end, the mechanical design becomes as important to the performance of the power system as the electrical design.

"Sometimes people forget that every electrical design has a mechanical design. The mechanical engineers are equally as critical as the electrical engineers—and in some cases you could argue more so—to the successful development of an electronics unit," comments Lyon. While the electronics designers are working to make power components operate as efficiently as possible, the mechanical designers are figuring out how to get rid of the heat generated by these components. Lyon also notes that, on a system level, the amount of heat that a satellite can reject is one of the key factors limiting overall system performance. (Another is the amount of power that can be generated.)

With regard to heat removal Lyon explains that "they [the mechanical engineers] have to do this by using very lightweight structures because we need low mass and we need to make sure things are as compact as possible. But at the

same time we need to make sure all the tolerance stack ups don't cause any interferences in the packaging," says Lyon who also points to shock and vibration as another consideration. "We have dynamic environments. When the box is sitting on the satellite riding up in the rocket, it's not exactly riding in a Cadillac."

Impact of Radiation

While the mechanical design is critical to the power system, the space environment still poses significant electrical design challenges including those not typically faced in the design of earthbound power systems. According to Lyon, the biggest difference is radiation. The impact of radiation on electronic components makes it challenging to meet the 15-year life requirement.

Radiation accelerates aging and drift processes. So components, particularly the active semiconductor devices that have tight initial tolerances on specifications coming off the assembly line, will experience much wider variations in those specifications over the operating lifetime of the satellite, according to Lyon. These wide tolerances must be accounted for in the electrical design in order to meet the satellite's long-life objective.

Naturally, that means designers must perform extensive worst-case analysis on the electronics. And that's despite the fact that the electronics (including the power

electronics) are designed using radiation hardened (rad hard) components.

The need for rad hard components is noteworthy for a couple reasons. One, it illustrates one of the key environmental challenges in the design of satellite power systems. But it also helps to explain the design environment in which these power systems are developed. Power system designers can only select components that have gone through a qualification process, which points to the role that component and process engineers play in these designs. Lyon describes the way components are approved at his company.

"We have an infrastructure in place for buying parts and procuring them and making sure they're qualified. We don't rely on just the design engineers to find space-qualified parts, we have a very long list of qualified parts that we've used before and are currently using. So the power system designers have that material available to them when they do a design," says Lyon. In terms of personnel, the infrastructure is extensive and rather specialized. "We have many engineers. We'll have a resistor expert, a capacitor expert, an IC expert "all of whom work with the vendors to make sure the parts are qualified and requalified as needed. If the desired power components are commercial parts (not space qualified) these engineers will subject the parts to an upscreening process

to certify them for space flight.

In addition to the component engineers, which are referred to as parts engineers at Space Systems/Loral, the company employs process engineers whose work also impacts the power system design. For example, process engineers develop techniques for applying thermal compounds and encapsulating pc boards.

Beyond the components and processes, once the power system assemblies are designed and built, they too are subjected to a rigorous development and qualification process. All of this helps to explain why the satellite power system is designed and (with the exception of some low levels of assembly) built in-house.

To read more about power system design in satellites, see the online version of this article.

About the Author

David G. Morrison is the editor of How2Power.com, a free portal providing information on all aspects of power conversion. Morrison is also the editor of How2Power Today, a free monthly newsletter presenting design techniques for power conversion, new power components, and career opportunities in power electronics. Subscribe to the newsletter by visiting www.how2power.com/newsletters

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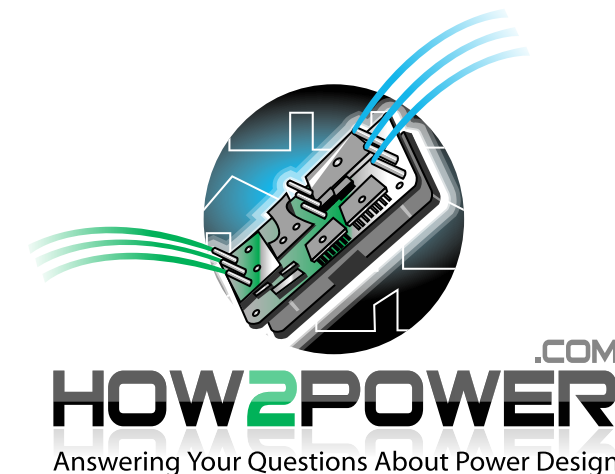
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THE GREEN REALITY



By Cliff Keys, Editorial Director & Editor-in-Chief, Power Systems Design

The US communications sector could never be classed as truly green, with demand accelerating on portable devices and the huge power consumption by the telecom industry for processing and cooling.

But it is improving. With more emphasis on power management and new technologies such as SiC and GaN emerging as real products, there is now the hope that even this industry can become greener. Not only this, but the availability and transmission of power for the heavy users is a problem where the administration is trying to encourage the development of the smart grid where solar and wind power can add to the power reservoir. Although these alternative or natural sources are growing, with the current US financial climate investment is not as forthcoming as it could be in a thriving world economic climate. Hopefully this improves

by Solyndra LLC in the United States, Also, Solyndra's subsidiary, Solyndra International AG in Baar, Switzerland and its subsidiary Solyndra GmbH in Holzkirchen, Germany, no longer have access to funding. As a result, Solyndra International AG and Solyndra GmbH have similarly ceased operations and are expected to file for insolvency under the laws of their respective jurisdictions in the coming days.

Despite strong growth in the first half of 2011 and traction in North America and EMEA with a number of orders for very large commercial rooftops, Solyndra could not achieve full-scale operations rapidly enough to compete in the near term with

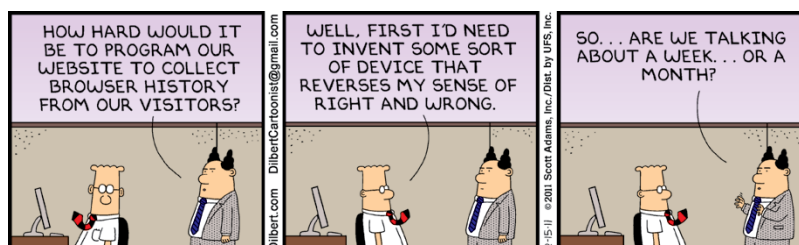
the resources of larger foreign manufacturers.

This competitive challenge has been exacerbated by a global oversupply of solar panels and a severe compression of prices that in part resulted from uncertainty in governmental incentive programs in Europe and the decline in credit markets that finance solar systems.

It's not all good news is it? Hopefully the US economy picks up to allow investment.

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We have also seen the sad demise of Solyndra, the American manufacturer of innovative cylindrical solar systems for commercial rooftops. With the discontinuation of operations and ceasing of business



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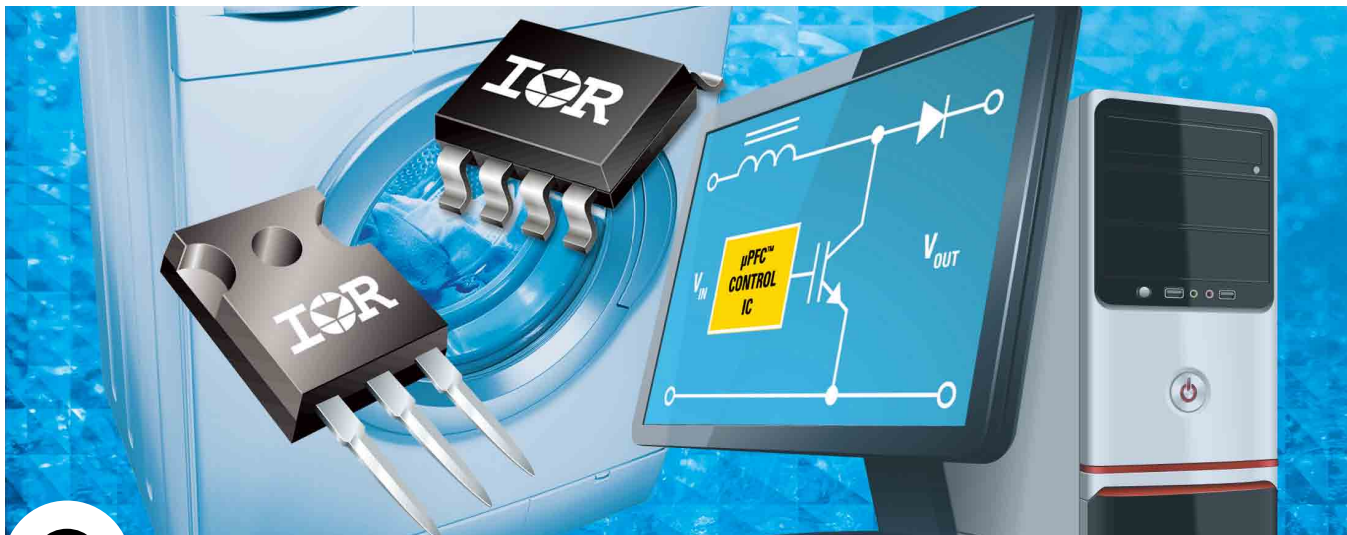
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