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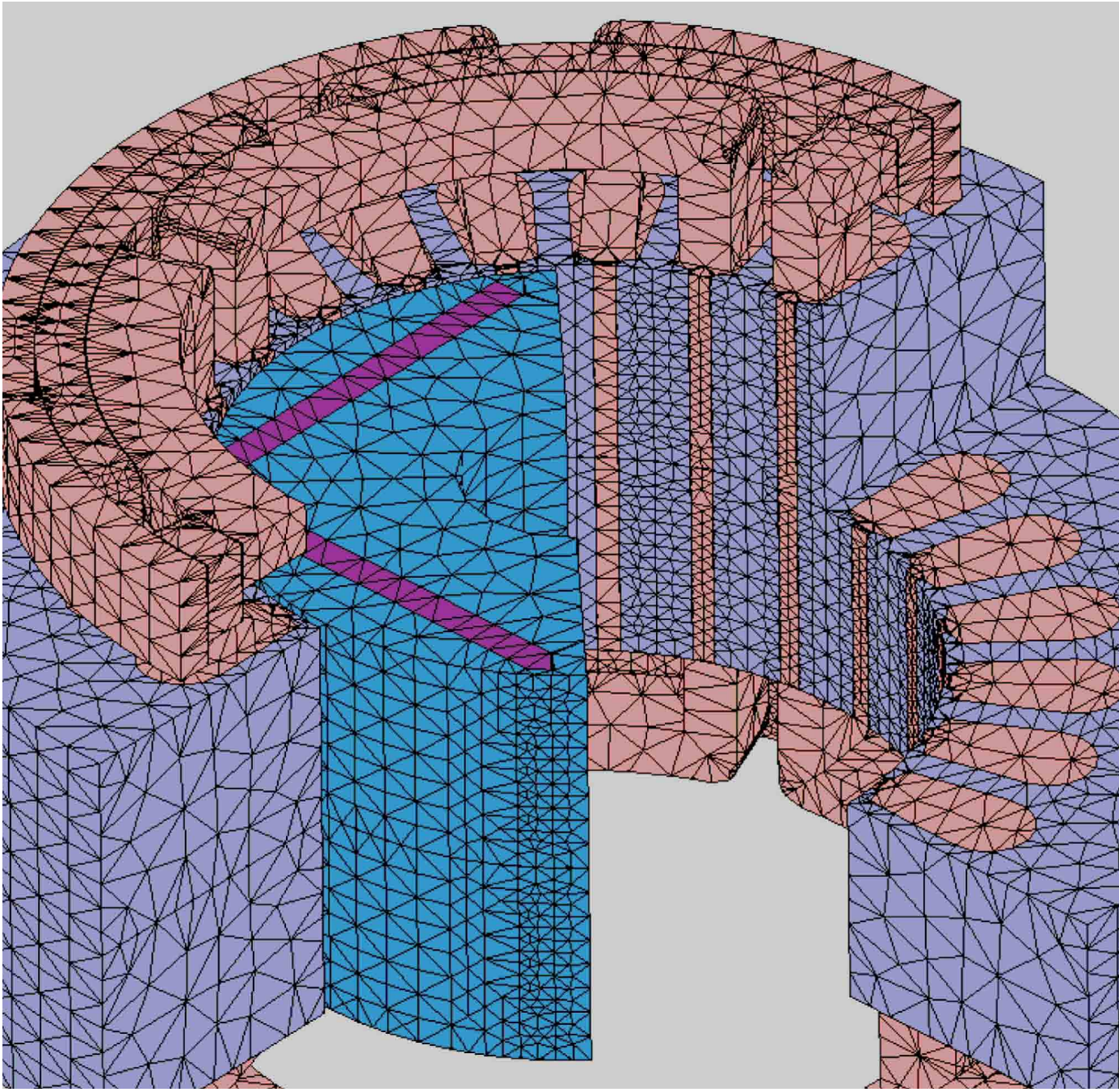

SPECIAL REPORT: AUTOMOTIVE (PG31)

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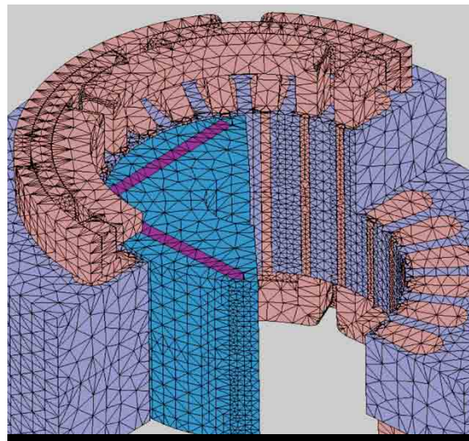
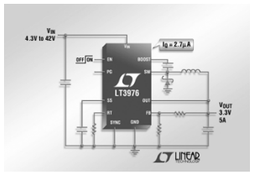


COVER STORY
Improving Electric-Montor Testing Techniques (pg 14)



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TIDE AND WAVE DATA NEEDED BY POWER SYSTEMS

While all renewable-energy manufactured devices inevitably have some adverse environmental impact, solar systems have struggled most with material efficiency being significantly less festooned with the environmental imponderables that beset wind, wave, and tidal power.

Wind farms urged to develop offshore mega-projects to improve supply chains, cut costs, and compete with other large-scale power generator, raise the protest that large turbine offshore wind farms significantly affect wind speeds, changing ocean up and down welling velocities, pushing nutrient-rich deep water to the surface, changing temperatures, and ultimately impacting existing ecosystems.

It makes current UK work into wave and tidal renewable power all the more intriguing. Several consortia of companies and universities are at work on scenarios that include FLOWBEC (Flow and Benthic Ecology) as well as Project ReDAPT (Reliable Data Acquisition Platform for Tidal) assessing three offshore wind turbine technologies, while a fourth observes a new commercial-scale tidal turbine.

The sonar systems in play here adapted from traditional down-facing ship mounted systems to up-facing seabed based units, collect an acoustic data curtain along the tidal flow around turbines and tidal device. Its yield will be essential data for the best in sea energy system designs.

And quietly coming to the aid of the data gathering party is news that two projects and some £720,000 in funding will involve the UK's National Oceanography Centre, the BGS (British Geological Survey) and the SAMS (Scottish Association for Marine Science) variously, first looking at AUVs (Autonymous Underwater Vehicles) drifters and gliders to demonstrate how data collected by these robots can not only support marine coastline and floorbed mapping requirements, but also perhaps help to reduced the cost of statutory marine monitoring obligations.

In the course of this work it seems likely that the deep-sea wind farm entrepreneurs might well lean towards use of robotics for data to prove their care of the ocean ecosystems too!

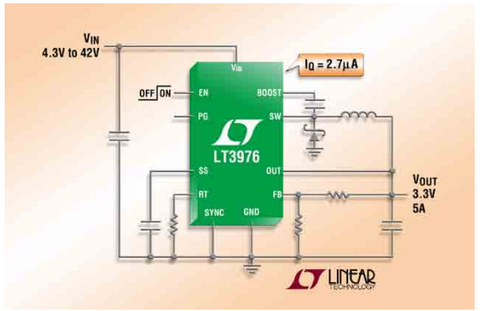
Best Regards,

Gail Purvis

Europe Editor
Power Systems Design
Gail.Purvis@powersystemsdesign.com

2 MHZ STEP-DOWN CONVERTERS NEED ONLY 2.7-µA IQ

The LT3975 42 V step-down switching regulator from Linear Technology delivers 2.5 A of continuous output current and requires only 2.7µA of quiescent current.



Similarly, the LT3976 can operate from a 40 V input, delivers 5 A, and requires only 3.3µA of quiescent current. Both devices offer a 4.2V to a nominal 40V input voltage range, making them ideal for automotive and industrial applications. Their internal high 75 mΩ switches deliver efficiencies as high as 90%.

The LT3975's and LT3976's burst mode operation offers ultralow quiescent current, a feature that is also well suited for automotive and industrial systems applications that demand always-on operation and optimum battery life. The devices' design maintains a minimum dropout voltage of only 500mV when the output voltage drops below the programmed output voltage, a functional necessity in applications subject to automotive cold-crank conditions.

Switching frequency is user-programmable from 200 kHz to 2 MHz, and synchronizable from 250 kHz to 2 MHz, enabling the designer to optimize efficiency while avoiding critical noise-sensitive frequency bands. The combination of their 16-lead thermally enhanced MSOP package and high switching frequency keeps external inductors and capacitors small, providing a compact, thermally efficient footprint.

The LT3975 and LT3976 use a high-efficiency 75 mΩ switch, with the boost diode, oscillator, control, and logic circuitry integrated onto a single die. Low-ripple burst mode operation maintains high efficiency at low output currents while keeping output ripple below 15 mV pk-pk.

Special design techniques and a new high voltage process deliver high efficiency over a wide input voltage range, and their current-mode topology enables fast transient response and excellent loop stability. Other features include a power good flag, soft-start capability and thermal protection.

The LT3975EMSE and the LT3976EMSE are available in a thermally enhanced MSOP-16, priced starting at $3.10 (1000) and $3.75 (1000), respectively. The LT3975IMSE and LT3976IMSE are tested and guaranteed to operate from a -40 to +125 °C operating junction temperature and are priced at $3.41 (1000) and $4.13 (1000), respectively. The LT3975HMSE and LT3976HMSE are tested and guaranteed to operate from a -40 to +150 °C operating junction temperature and are priced at $3.66 (1000) and $4.38 (1000). All versions are available from stock.

www.linear.com

THE VARIED USES FOR POWER DEVICE MODELLING

By: Dr. Phillip Mawby, Professor, University of Warwick

Power devices are used to process electrical power as efficiently as possible.

In the design process, therefore, there are many aspects for which device simulation is used. There are several levels of complexity needed depending on what the engineer is trying to quantify. At the device level, usually full scale numerical models that solve the drift-diffusion equations and heat equation are needed to understand the nuances of device design.

These models are used by device designers who need a detailed picture of a device's internal operation to improve its performance. This modelling technique is detailed so the time needed to characterise a single switching event can be long, which is problematic when a designer wants to look at anything more complex.

To look at the operation of a circuit, circuit simulators such as SPICE or SABER are used. Here the device is treated as a set of equations that characterise the physical operation of the device in a simple manner and are often referred to as compact models because they boil down the essence of the device operation without the need to solve a set of partial differential equations.

For bipolar power devices, these models can be very complex in their handling of stored charge, which determines the switching characteristics of the device. This is difficult to model because the diffusion equation that characterises bipolar devices has moving boundary conditions.

Many methods have been tried to successfully model the bipolar switching behaviour, but if this model is too simple, it will fail to capture the device's underlying physical behaviour. This type of model is often used to capture the switching losses of the device switching in a complex circuit environment.

The next level of abstraction that simulators such as PLECS use is to have an ideal model for the switching device. This level of model helps investigate the circuit operation, the control mechanism used in its drive, and its thermal behaviour. The main reason this is required is that there is a fundamental difference between the time constants involved with the electrical switching (ns or µs) and the time constants involved in the thermal operation (ms to s).

These are essentially incompatible in terms of the computing time needed, and so the two are decoupled by the use of a look-up table. This dramatically speeds up the thermal modelling while not losing any accuracy. To get accurate thermal information, it is necessary to have a detail thermal model of the associated cooling system. The most effective method is to use a full 3D compact model, which can be represented as a Fourier series.

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POWER ICS DRIVING FORWARD IN AUTOMOTIVE ELECTRONICS

By: Ben Scott

Power-management and IC-driver products are becoming increasingly important as electronic content per vehicle rises.

Moreover, the power-IC market is a lucrative one with a value of $1 billion in 2011, growing to $1.4 billion by 2018, says IMS Research. This opens up many opportunities for the suppliers in this market like Infineon, Maxim Integrated Products and Fairchild Semiconductor.

A large proportion of this value comes from powertrain applications. Power ICs are essential for engine-management systems in petrol, diesel, hybrid, and electric vehicle applications. The market for power ICs in the hybrid and electric space will reach over $50 million this year, but the largest market will be for power discretes and modules. The vehicle's inverter requires power electronics to drive the motor/generator. Alternators and fuel pumps make significant use of power ICs. Automatic transmission control units also make use of power ICs to drive the large number of MOSFETs found in this application. Steering systems use either a brushed or brushless DC motor and there are a number of MOSFETs here which require a power IC.

Stepper motors will become more prevalent in auto-leveling headlight control where a stepper-driver IC will be used. HVAC systems have historically used unipolar stepper motors, but there is a trend towards bipolar stepper motors because of increased efficiency and better torque. Bipolar steppers are more expensive, but are approaching parity with unipolar steppers. Bipolar steppers will use similar driver ICs to those found in headlight leveling.

The high growth expected in this market is also driven from regional legislation on ESC (Electronic Stability Control). In the USA there is legislation that all 2012 model passenger vehicles will have ESC fitted as standard. There is similar legislation in the UK, Canada, and Australia. Clearly, mandatory fitment of this system will drive the power-IC market value upwards. However, in these regions the market for this system will be saturated and the market will stagnate as power IC prices come down.

There is a trend in passenger vehicles for the use of LEDs for front and rear lights, ambient cabin lightning, and backlighting for infotainment and instrument clusters. These are all growth areas for the power-IC market as the LEDs need a driver. The number of LEDs per system will decrease as LEDs become brighter, but the number of power ICs to drive these LEDs will remain roughly the same.

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AUDIOSUSCEPTIBILITY MEASUREMENTS AND LOOP GAINS

By: Dr. Ray Ridley

In this series of articles, Dr. Ridley discusses the four important frequency-response measurements to be made during full characterization of a switching power supply. The important relationships between loop gain and audiosusceptibility measurements are highlighted in this second article. As with output-impedance measurements, it is possible to extract a calculated loop gain from the audiosusceptibility measurements, but direct loop gain is recommended to guarantee rugged stability.

Power Supply Transfer Function Measurements
There are four fundamental transfer functions that characterize the small-signal performance of a switching power supply. They are as follows:

1. Loop gain and phase – determines the stability of your design, and available margin to accommodate variations in components.
2. Output impedance – determines the output regulation, dynamic load response, and susceptibility to complex loading.
3. Audiosusceptibility – determines the transmission of noise from input to output.
4. Input impedance – determines the sensitivity of the power system to input filter or input power system components.

The first two parameters, loop gain and output impedance, were discussed in the first article of this series. It is highly recommended that both of these measurements are made on every switching power supply that you design and build. The loop measurement is essential to guarantee stability over the lifetime of the power supply, and the output impedance gives comprehensive information about the performance in the presence of load variations.

An audiosusceptibility measurement gives information about the transmission of noise from the input of the power supply through to the output. It is usually a requirement of the documentation package in the aerospace industry. This measurement is more difficult to make than output impedance since a perturbation must be injected on top of the high-power input rail. Most commercial designs

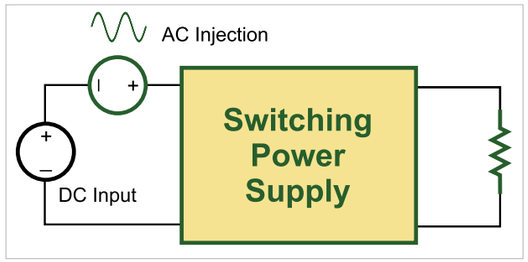

Fig. 1: Audiosusceptibility is measured by adding a voltage signal at the input terminals of a power supply.

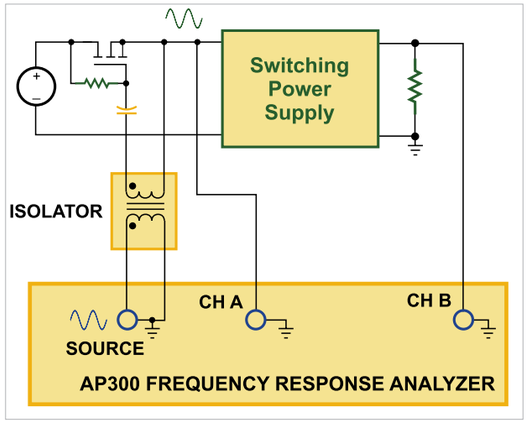

Fig. 2: Practical test setup for injecting voltage signal and measuring audiosusceptibility.

omit this measurement, although it can be very useful for getting maximum performance out of your power supply. With the injection techniques recommended in this article, it is not that hard to make the measurement and it is usually well worth the time.

Audiosusceptibility Measurements

Audiosusceptibility directly shows how well a converter rejects noise appearing on the input. In order to measure audiosusceptibility, a voltage source must be injected in series with the input of the power supply as shown in Figure 1.

Figure 2 shows how this is implemented practically using a frequency response analyzer and a few discrete devices. The output of the analyzer is connected to wide-bandwidth isolator which is then AC coupled to a FET hooked up as a voltage follower. The size and rating of the FET may vary according to the power level and voltage level of the converter that is being driven. This injection technique is much simpler and more cost effective than inserting a high-power amplifier in series with the input source, and will allow sufficient signal to be injected for most applications.

It is useful to plot both the open-loop and closed-loop audiosusceptibility to show how well your control design is implemented. These two measurements are shown in Figure 3 for a sample flyback converter operating with voltage-mode control.

The green curve of Fig. 3 shows the open-loop audiosusceptibility of the converter. At low frequencies, the dc value is determined by the dc gain of the converter and the transformer turns ratio. Above 1 kHz, beyond the resonant frequency, the

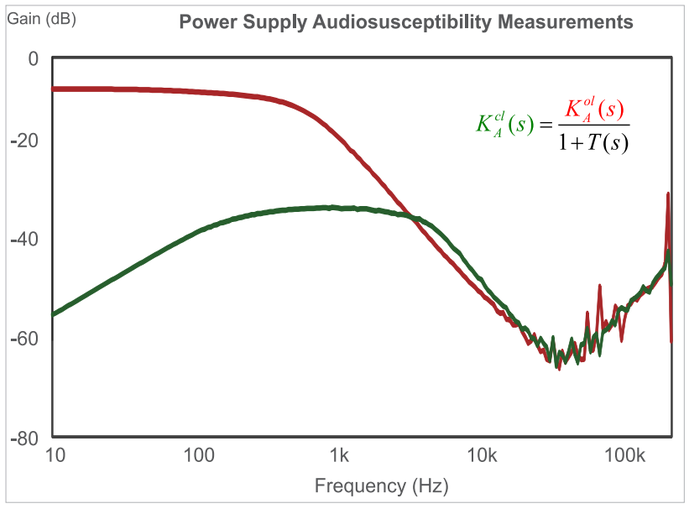

Fig. 3: Open-loop and closed-loop audiosusceptibility measurements of a flyback converter.

measured audiosuceptibility is attenuated according to the LC filter characteristics. It is often difficult to make measurements at higher frequencies due to noise pickup in the cables and the small size of the output signal, as indicated by the results of Fig.3.

The red curve of Fig. 3 shows the effect of closing the loop on the output impedance. At low frequencies, where the loop gain is high, the audiosusceptibility is greatly reduced. The two curves converge together at the crossover frequency of the loop. As is well known for a single-loop feedback system, the theoretical closed-loop audiosusceptibility is related to the open-loop audiosusceptibility by the equation:

$$K_A^{cl}(s) = \frac{K_A^{ol}(s)}{1+T(s)}$$

From this equation we can see that the higher the loop gain T(s), the more the audiosusceptibility is reduced by the feedback loop. When you are designing a power supply, there are two ways to reduce the audiosusceptibility. The first is by increasing the amount of capacitance on the output of the power supply to lower the open-loop audiosusceptibility. This, of course, requires more expense in terms of parts and space. Or, you can increase the gain of the loop. Changing loop components is usually a zero-cost option,

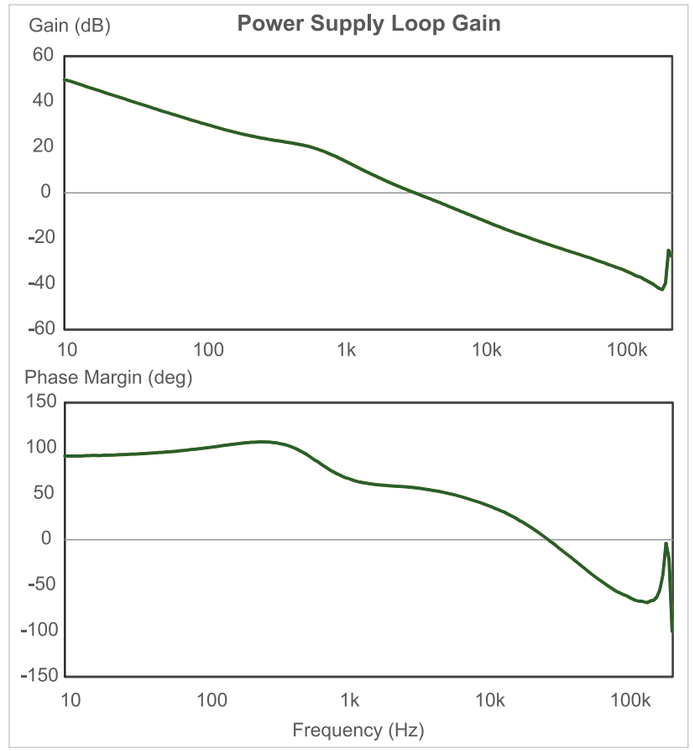

Fig. 4: Measurement technique for loop gain.

but you must be careful not to increase the loop gain too high or instability can result. Some modern converters have very low loop gains and crossover frequencies, resulting in non-optimal performance.

Loop Gain Measurements

You should always measure the loop gain of your converter to ensure you are maximizing the performance in terms of audiosusceptibility and output impedance, whilst retaining rugged stability. Fig. 4 shows the test setup for injecting into the feedback loop for accurate results. This setup requires the insertion of a test resistor into the feedback loop, but this is not a difficult process. Further details of using this test setup are covered in detail in [1, 2].

Fig. 5 shows the measured loop results for the flyback converter. The gain at 10 Hz is approximately 50 dB, and this corresponds to the difference in magnitude of the open- and closed-loop audiosusceptibility shown in Fig. 3.

The crossover frequency is at around 3 kHz, and the phase margin at crossover is 60 degrees. The open and

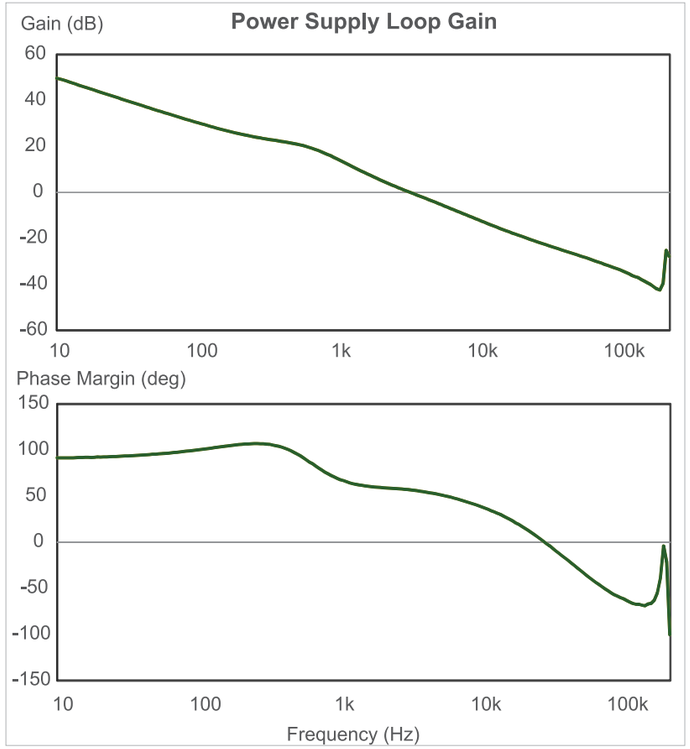

Fig. 5: Direct loop gain measurement of flyback converter.

closed-loop audiosusceptibility measurements are approximately equal at this point. It is interesting to see that beyond this frequency, the closed-loop audiosusceptibility is actually higher than the open-loop measurement. This is because the vector sum of 1+T(s) is less than one as the phase margin of the measured loop drops below 60 degrees. The same effect was observed for the output impedance measurement in the previous part of this series.

Synthesized Loop Gain Measurements

Three measurements have been made so far for this converter – open-loop audiosusceptibility, closed-loop audiosusceptibility, and loop gain. In theory, only two of these measurements should be necessary since the three quantities are related to each other by Eq. 1. In practice, however, we always measure all three quantities since direct measurement of each gives the most dependable results. If we rearrange Eq. 1, we can express the loop gain of the converter in terms of the audiosusceptibility measurements as follows:

$$T(s) = \frac{K_A^{ol}(s)}{K_o^{cl}(s)} - 1$$

From this, we can try to plot the loop gain from just the audiosusceptibility measurements. Note that it is crucial that both the magnitude and phase of the audiosusceptibility measured in order to perform this calculation, even though we commonly only present the magnitude as part of a power supply characterization. Fig. 6 shows the result of this equation plotted against the directly-measured loop. The green curve of Fig. 6 shows the directly-measured loop gain, and the blue curve shows the calculated loop gain, synthesized from the impedance measurements.

Fig. 6: Direct loop gain measurement compared with synthesized loop from audiosusceptibility measurements.

For this power supply example, the measured and calculated loop gains agree fairly well up to the region of the crossover frequency. At high frequencies there is very significant deviation of the directly-measured true loop gain and the gain synthesized from the audiosusceptibility measurements. This is due to the noise pickup in the audiosusceptibility measurements as the attenuation is large. The synthesized loop gain of Fig. 6 is not sufficient to guarantee lifetime stability since gain margin is not measurable, and the possibility of multiple crossings cannot be observed.

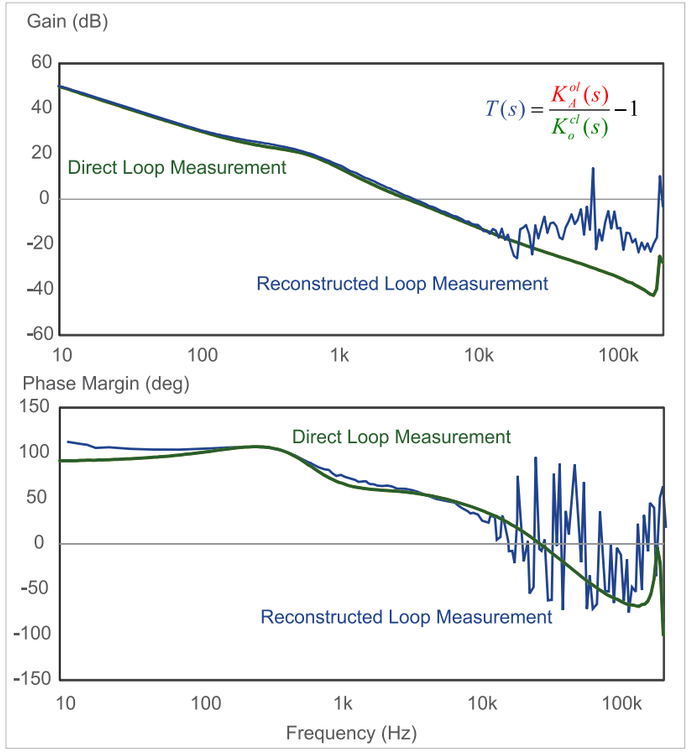

Fig. 6: Direct loop gain measurement compared with synthesized loop from audiosusceptibility measurements.

Summary

This article clearly shows the relationship between loop gain and audiosusceptibility measurements. Most aerospace designs require the audiosusceptibility measurement to be made, but it is also useful for other applications, and it is recommended that you record these measurements as part of a complete documentation package.

In the next article of this series, we will look at the input impedance measurement and its correlation to loop gain.

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Dr. Ray Ridley
President, Ridley Engineering

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IMPROVING ELECTRIC-MOTOR TESTING TECHNIQUES

By combining FEA with FPGA hardware, simulation models can include nonlinearties for accurate motor representation

By: Nick Keel and Frank Heidemann

The growing adoption of electric motors in the automotive industry creates new challenges for embedded-control-system developers and test engineers.

Control algorithms for electric-drive ECUs (electronic control units) must run much faster than power-train ECUs for internal-combustion engines. These higher speeds make the traditional approach to HIL (hardware-in-the-loop) testing inadequate for testing electric motor ECUs. Engineers must simulate electric motors with high fidelity, and HIL test systems must be able to execute simulation models at rates on the order of 1 µs to adequately represent the electric motor's operation (Figure 1).

Power electronics introduce another challenge when developing and testing electric-motor control systems. To test the power electronics, the test system must handle voltages that range from 20 to 600 V and current that could be in excess of 500 A.

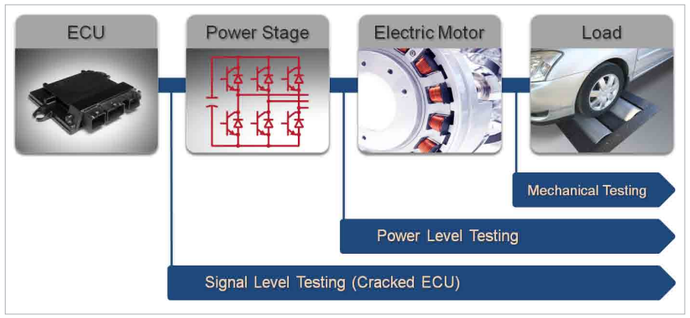

Figure 1: Each stage of embedded-software validation for electric-motor simulation introduces new challenges for test engineers such as high-speed processing and high-power signals.

These types of tests often implement on a dynamometer, but dynamometers are limited in the test coverage that they can provide. They often fail to represent accurately vehicle dynamics, which increases the number of field tests necessary to validate fully an electric vehicle power train. A test system capable of handling high-power signals while accurately simulating vehicle dynamics reduces the number of dynamometer and field tests, and reduces the overall time and cost to test.

Motor simulation using FEA

One of the greatest challenges engineers face when conducting real-time simulation of advanced motor drives is how to attain an adequate combination of model fidelity and simulation step time. While a simple constant parameter D-Q model may be sufficient to conduct some HIL tests, increased model fidelity is often necessary for the design of advanced motor drives.

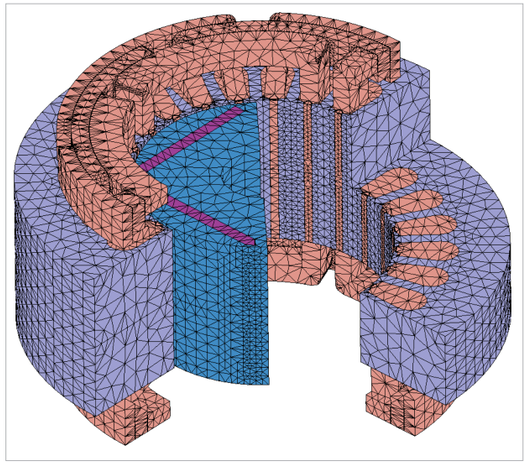

Figure 2: The high density mesh of the FEA (finite element analysis) produces a very high fidelity representation of this IPM (interior permanent-magnet) motor's characteristics.

High-fidelity simulation also applies to performance optimization of control systems in high-efficiency electric motor applications commonly found in the automotive industry. Using high-fidelity FEA (finite-element analysis) models, an engineer can simulate complex, non-ideal behavior such as cogging torque and design a controller to reduce torque ripple.

Similarly, a designer can simulate the variation in motor inductance at high currents, which greatly affects the torque produced by the motor, and test the controller accordingly. Lower-fidelity models do not adequately represent cogging torque, motor inductances at high currents, or other nonlinearities in the simulation. The absence of these characteristics reduces the effectiveness of HIL testing, which results in more field tests and increased development time to test adequately embedded-control software.

FEA is a simulation method that provides highly accurate motor models with enough fidelity to account for nonlinearities found in electric motors (Figure 2). However, historically, this high fidelity simulation has been limited to software-only implementation, because it can often take hours to simulate a few seconds worth of real-world operation.

To perform HIL testing on electric motor systems, simulation models must run in real-time. High-fidelity models need simplifying to run within the limits of processor-based systems, resulting in reduced effectiveness of HIL tests. A processor-independent, hardware-based simulation is necessary to achieve the closed-loop update rates required for electric-motor HIL testing.

FPGAs provide the high speed processing necessary for electric-motor simulation and high-speed update rates with low latency from input to output. However, because FPGAs are hardware, they have limited available resources.

Engineers must often simplify electric-motor models to operate within the limits of these resources, which reduces model fidelity. To obtain the performance and accuracy necessary for real-time high-fidelity electric-motor simulation, an FPGA must be large enough to contain the entire characterization of the electric motor.

Advancements in FPGA technology have made it possible for tools such as the JMAG add-on for NI VeriStand to perform real-time high-fidelity simulation of electric motors for HIL testing. Meanwhile graphical-programming tools such as LabVIEW FPGA provide an abstracted tool chain for FPGA development that reduces development time for creating high-fidelity electric-motor models.

High-power HIL testing

While signal-level testing provides much value for developing control algorithms and evaluating ECU performance, it is important

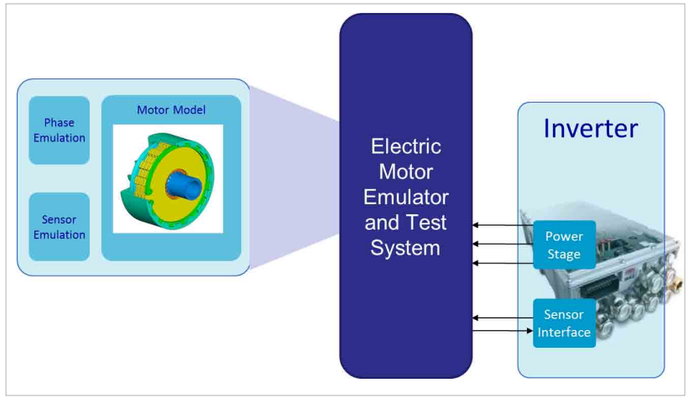

Figure 3: In an electric-motor emulator test system, the emulator inputs the high-power signals from the power stage and closely represents the dynamics of the system's missing components.

to also validate the power electronics associated with the system. Dynamometers are common for power-level testing, but they cannot accurately represent high-frequency dynamics needed to adequately validate system performance.

The lack of test coverage dynamometer testing achieves forces test engineers to perform extensive field tests, which results in reduced test coverage and higher overall test costs. An HIL test system capable of integrating power electronics and simulating vehicle dynamics provides test coverage not found in dynamometer testing.

In the case of an electric-drive dynamometer, the original electric motor in the drive train couples to another electric motor that the test system controls. This electric-motor-dynamometer configuration involves an electric drive tested together with a controller that includes high-voltage power electronics.

The problem with this procedure is that the rotating test system itself constitutes a drive train with drive shafts and load machine, but it has nothing in common with the vehicle into which the electric motor will eventually operate. This renders it almost impossible to model mechanical feedback and turning-speed dynamics from the vehicle with any level of accuracy.

This is a serious disadvantage since electric-motor speed does not always couple to vehicle speed, especially in hybrid drives. In many real-world scenarios, there are intermediate states with gears disengaged and no drive to the wheels, which leaves the electric motor to turn without any load.

The test system cannot reproduce the resulting turning speed dynamics in the rotating test system, because the inert masses involved are too different from those in the future vehicle. This forces engineers to test the ECU in a test vehicle on the road.

An inverter test system, or electric-motor emulator, bridges this gap between the HIL test system and vehicle field tests (Figure 3). This system can interact with high-power signals associated with inverters, and it allows engineers to reproduce load and ambient conditions in the lab exactly as they occur in a drive inverter under field conditions. System level testing that accurately simulates real-world conditions helps test engineers find faults earlier in the embedded software development process, which reduces costs and minimizes development cycles while yielding test data of higher quality.

In practice

Real-time high fidelity electric motor simulation makes it possible to test many types of transient and fault conditions that would be difficult or impractical to perform with the real systems. In the past, many of these conditions such as faults on motor terminals or faults between DC and AC busses have been impossible to implement during HIL testing with standard DQ electric-motor models.

By combining high-fidelity FEA with high performance FPGA hardware, simulation models can include complex non-linear behavior for accurate motor representation. The signals from the model running in FPGA can then connect to other hardware at the high I/O rates necessary for complete testing.

Electric-motor emulators are useful at very early stages in developing and testing hybrid drives and other drives with electric motors. Engineers can map any electric motor type using an integrated emulator, which will behave like the corresponding physical motor in dynamic turning-speed operation.

Emulators also allow developers to model phenomena not yet accounted for in controllers such as harmonic vibrations in electric motors and cancelling out acoustic effects in control engineering. The system runs like a physical motor, but without any moving parts. This means that engineers can run a wider range of tests and collect more accurate data, which reduces time spent with field tests and produces better embedded software.

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REDUCE STAND-BY POWER LOSS IN AC—DC SUPPLIES

New digital power controllers satisfy strict stand-by dissipation standards for consumer-electronics.

By: Scott Brown

Over the past decade, controller-IC manufacturers have worked to reduce so-called vampire or stand-by power consumption.

Organizations such as Energy Star in the US, Blue Angel in Germany, and CNIS (China National Institute of Standardization) have introduced strict stand-by power-consumption standards for consumer electronics. New topologies in the AC—DC power-supply market need implementation to achieve the approvals of these important standards agencies. Traditional flyback converters designed with legacy analog controllers can struggle to achieve the combination of low cost, high operating efficiency, and low stand-by power consumption that today's consumer electronics require. The market now demands new topologies that address all AC—DC feature and performance requirements at low BOM cost.

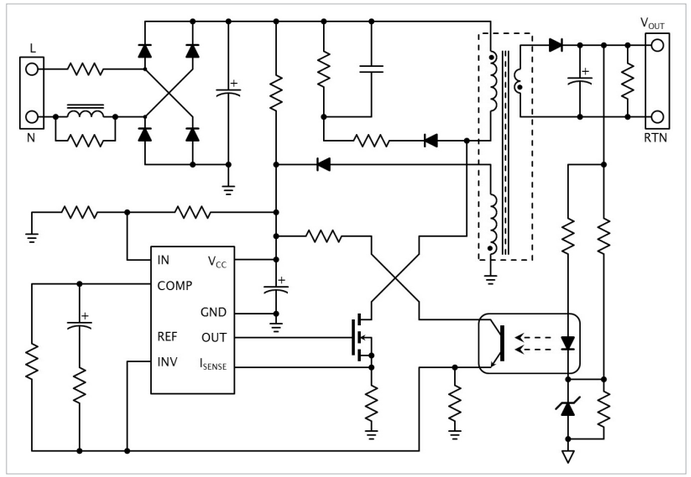

Figure 1: A simplified diagram of a typical 10—20 W flyback converter for isolated off-line applications.

With the typical number of small appliances and electronic devices in an average household rising to 24 over the past decade, the consumer electronics and home appliances market reached its zenith despite one of the largest global economic downturns in a century (Reference 1). With the number of powered devices in our homes increasing, the demand on the electrical power grid is expanding at an equivalent rate. Many governments, realizing the economic and environmental ramifications of the ever-increasing electrical load have implemented strict energy standards to limit the power consumption of these electronic devices while they're operating and, more importantly, while they're in stand-by mode.

The biggest problem area is the main power supply, whether for powering plugged-in electronics or the charger for portable electronics. Traditional approaches use power supply technologies that waste energy at low output power as a consequence of keeping costs down. The industry needs new techniques to reduce power consumption when the load is virtually zero without increasing system cost.

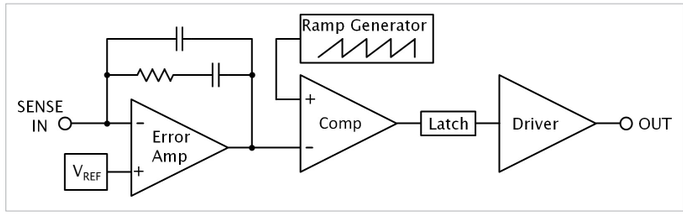

Figure 2a: An analog controller directly monitors the converter's output voltage.

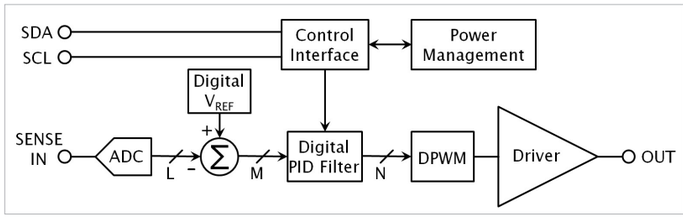

Figure 2b: A digital converter can switch operating modes without complex compensation schemes.

Traditional analog PWM ICs

The main off-line AC—DC power supply for consumer electronics traditionally uses a simple analog PWM (pulse-width modulation) controller IC and low-cost external components. To keep cost to a minimum, the designer generally uses a generic analog PWM controller, typically a controller that could apply to multiple configurations with a minimum of internal complexity. With these basic controllers, the main power-supply topologies are typically isolated flyback or forward converters, requiring a large number of external components and output feedback from a costly opto-isolator and several discrete components for external frequency compensation (Figure 1).

Most of these analog controllers are simple PWM controllers which operate in full PWM mode regardless of the load conditions. This works well at full output power, but efficiency, η, quickly degrades at medium and light loads, making it difficult for these legacy controllers to meet modern efficiency requirements, which use an average η calculation based on output power to set a minimum η requirement. At light load currents, the legacy controllers will have efficiencies well below 70% that pull down the average, making it difficult for these converters to meet the new standards. Designers can implement additional modes of operation, such as PFM (pulse-frequency modulation) or pulse-skipping to improve η, but this adds complexity and circuit cost that may be burdensome for the mainstream market.

Digital control technology for power supplies has been around for several years but it has now matured to the point where the cost—performance tradeoff can better that of analog alternatives. In the case of off-line power supplies, digital control blocks' benefits surpass those of analog-equivalent blocks.

Domain makes a difference

The analog block monitors

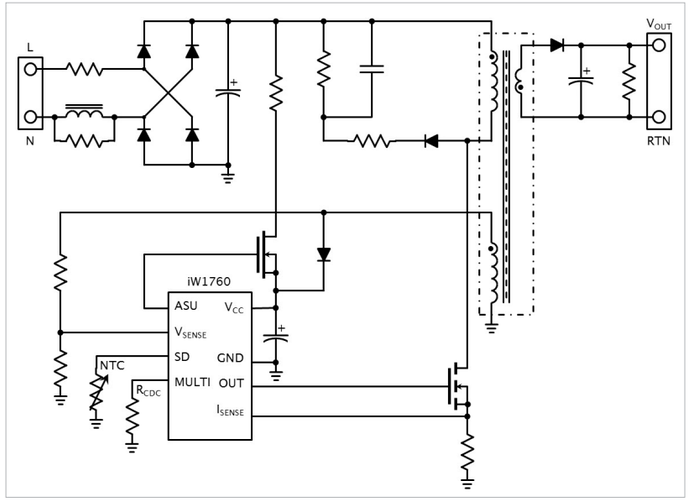

Figure 3: A flyback converter implemented with a multi-mode digital controller maintains high η over a large current range.

voltage directly and modulates the output based on that input (Figure 2a). In contrast, the digital block converts the traditional analog input into a digital signal, which it then filters and processes to determine the output conditions (Figure 2b). The digital converter, however, achieves a degree of freedom that the analog circuits cannot: The digital block can quickly modify the modulation scheme, matching the converter's operating mode to the system's needs, increasing η without sacrificing performance. Additionally, because digital algorithms manage the loop compensation, there is no concern about stability and, in some cases, no need for external compensation components. In the event of heavy loads, the controller can drive the output at its highest programmed

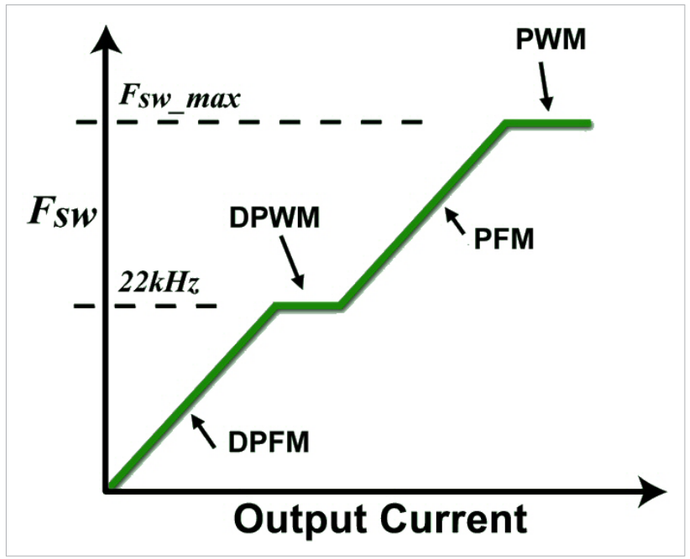

Figure 4: Multi-mode operation—switching frequency as a function of load current.

switching frequency to maximize η. When the load current falls to a level where the switching losses become an important efficiency factor, the digital controller can change the modulation from PWM to PFM, reducing the average switching frequency and saving power. Digital control makes it possible to implement this type of dynamic multi-mode approach cost-effectively.

Multi-mode increases η

For example, iWatt's iW1760 is a digital controller that integrates a multi-mode digital modulator to increase efficiency. The circuit example (Figure 3) and the typical operating curve of (Figure 4) illustrate the power of digital control technology: The device offers four distinct operating modes, PWM, PFM, DPWM (Deep PWM) and DPFM (Deep PFM) to maintain a high average η.

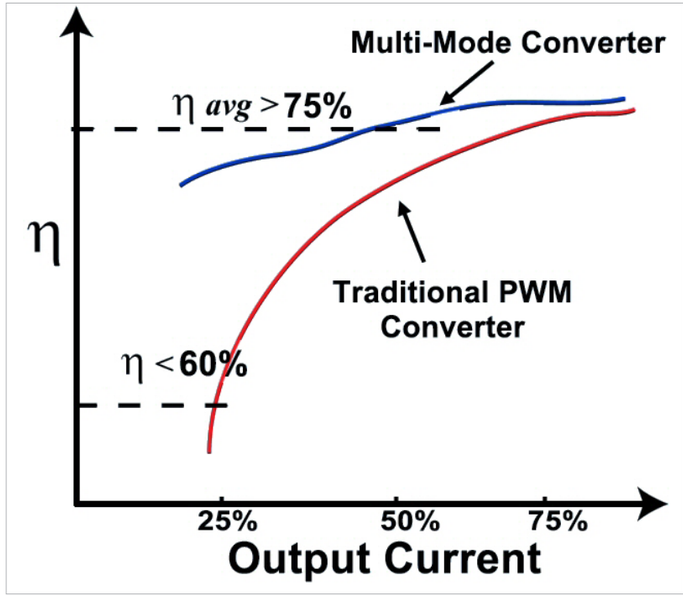

Figure 5: Efficiency comparison between a multi-mode converter and traditional PWM converter implementations.

The converter operates in full PWM mode with a constant frequency at high output currents. When the output current reaches a calculated minimum threshold, the converter switches to PFM mode, increasing the off time to save energy.

As the load current decreases to the point where the PFM switching frequency would possibly enter into the audible spectrum (no less than 22 kHz), the device automatically switches into DPWM mode, holding the switching frequency constant at 22 kHz. When the load current drops low enough, the digital block changes the converter into DPFM mode, where the switching frequency drops into the audible range, but at power levels so low that the converter does not emit audible noise.

An analog controller, operating in full PWM mode at very light loads will end up dissipating 0.5—1 W just in power lost in the external components and the operating current of the controller itself. This power consumption is beyond the levels that standards organizations such as Energy Star have established (Figure 5).

By using the digital control block, the user enjoys efficiency levels greater than 80% at full load and an average efficiency over a broad operating current range greater than 75%. Modern digital controllers, such as the iW1760, can achieve a no-load power consumption of only 50 mW. This is well below Energy Star's requirement that AC—DC external power supplies consume 300 mW or less in stand-by mode.

Fewer components

Besides the efficiency gains, digital control also allows designers to reduce the external component count. By managing compensation in the digital domain, designers can remove several passive components from the schematic.

The digital controller can also implement primary-side control without sacrificing regulation performance. This allows the circuit to provide an isolated output without an opto-isolator, a component that is costly and is one of the weak links in power supply reliability.

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ESTIMATING BOND WIRE CURRENT-CARRYING CAPACITY

Analysis provides insight into bond-wire performance in various configurations for power-management ICs.

By: Jitesh Shah

Semiconductor manufacturers use wire bonds extensively to connect a chip's I/O pads, including power, to its package's external pins.

Wire bonding processes typically use gold wire because of its oxidation resistance, high electrical conductivity, and the relative ease with which it bonds to the IC's pads and the package's pins. An approach involving replacing gold wire with copper is gaining strength due to copper's superior electrical and thermal properties, lower intermetallic growth, and increased mechanical stability.

Devices that pass high DC currents use multiple bond wires. The extra wires reduce the DC IR drop and its associated heating to reduce the risk of wire fusing. Unfortunately, there is no method or analysis in place to estimate the number and size of wires to use for a given application. Either the number of wires used is too pessimistic, increasing the die area and cost, or too optimistic, decreasing the device's reliability.

The theoretical estimate

The classical design equation for wire fusing was developed by W.H. Preece in 1884 and applies only to wires in free air. The Preece equation relates the fusing current in amperes to the diameter of the wire in inches:

WIRE DIAMETER	PREECE EQUATION	MODIFIED PREECE EQUATION (MIL-M-38510J)	
(Mils)		Conductor Length ≤ 0.040"	Conductor Length > 0.040"
2	0.92	2.68	1.83
1.3	0.48	1.41	0.96
1.2	0.43	1.25	0.85
1	0.32	0.95	0.65
0.9	0.28	0.81	0.55
0.8	0.23	0.68	0.46
0.7	0.19	0.56	0.38
0.6	0.15	0.44	0.30

Table 1: Current-carrying capability based on Preece equations

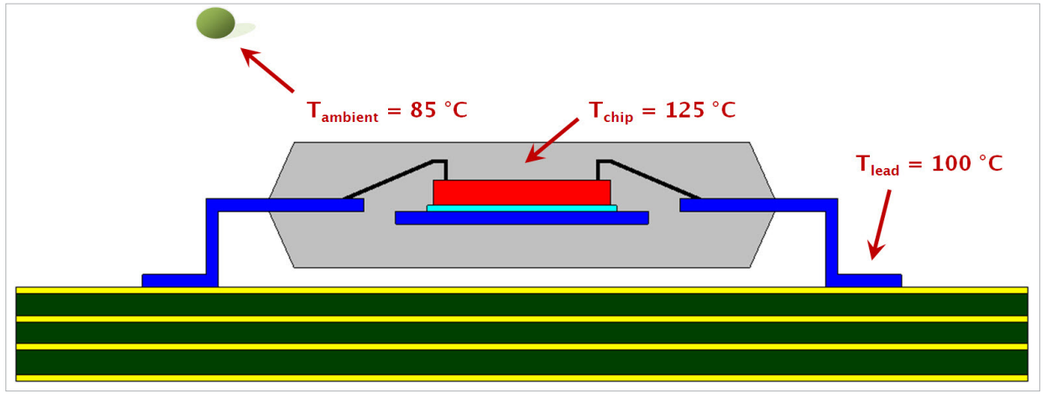

Figure 1: Package on a PCB with relevant temperature-monitor points

$$i = kD^{\frac{3}{2}}$$

where i is the DC or RMS current, k is a constant corresponding to wire composition, and D is the diameter of the wire in inches. For gold and copper, k = 10,244.

One of this equation's limitations is that it applies only to wires in free air. Additionally, it does not consider the fact that the current carrying capability of a wire varies inversely with its length.

Modified Preece equation

One way to address these limitations is to modify the Preece equation with a higher value of k to reflect typical packaging processes that encapsulate the bond wire with an epoxy-based molding compound. The constant k also reflects the effect of length on the wire's current-carrying capability. The value of k for conductor length ≤ 0.040" for both gold and copper is 30,000 and for conductor length > 0.040" is 20,500.

The equation Military specification MIL-M-38510J presents bases its current-carrying capability assessment on the modified Preece equation. Table 1 lists the calculated current-carrying capability in Amperes of both conductor types using the two versions of the Preece equation.

Two limitations remain with the modified Preece equation. It produces current-carrying-capability values that are material-independent. Copper has 20% higher thermal conductivity and 30% higher electrical conductivity than gold, which should result in copper being able to carry more current than gold for a given bond wire length and diameter.

The equation does not extrapolate the current carrying capacity with conductor length beyond 0.040" (about 1 mm). Most applications use wire lengths in the 2- to 3-mm range or longer. A wire's current-carrying capability varies dramatically as conductor length changes, which the equation fails to consider. Given these limitations, a new approach is necessary that accounts for known geometry and material properties and on limitations typical applications impose.

Joule heating in conductors

Current flowing through a non-ideal conductor—one with non-zero electrical resistance—converts electrical energy to thermal energy through a process called Joule heating or resistive heating. The magnitude of heat the processes generates is directly proportional the wire resistance and to the square of the current:

$$Q_{generated} = I^2R$$

For a conductor surrounded by still air, all heat generated dissipates through the conductor with negligible heat conducted

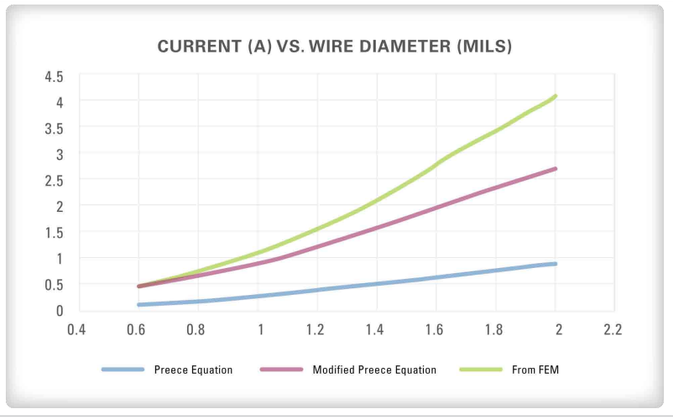

Figure 2: Current-carrying capability of 1-mm-long gold wire using FEM and the Preece equations

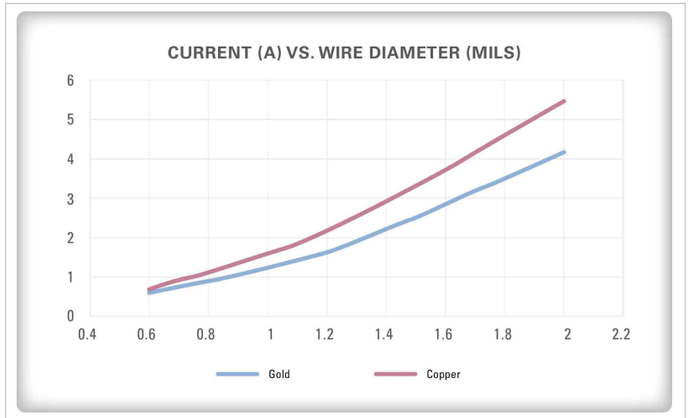

Figure 3: Current-carrying capability of 1-mm-long gold and copper wires using the FEM approach

away from the conductor surface. The system reaches steady state when:

$$Q_{generated} = Q_{dissipated}$$

The generated heat dissipates through the length of the wire using a simple conduction heat-transfer process:

$$Q_{dissipated} = kA\frac{dT}{dx}$$

where k is the wire's thermal conductivity (310 W/mK for gold and 390 W/mK for copper), A is the cross-sectional area of the wire, dT is the temperature differential at the two ends of the wire, and dx is the wire's length.

Rearranging and simplifying,

$$I = \frac{\pi}{4}\sqrt{\frac{k}{\rho}}\frac{D^2}{l}\sqrt{\Delta T}$$

where ρ is the wire's resistivity (2.44x10-8 Ω-m for gold and 1.68x10-8 Ω-m for copper), D is the wire diameter, l is the wire length, and ΔT is the temperature difference between the wire's two ends, which we assume to be a constant for a maximum current-capacity calculation. Simplifying even further,

$$I\alpha\sqrt{\frac{k}{\rho}}\frac{D^2}{l}$$

Based on the above relationship, assuming everything else remains the same, copper should be able to handle 25% more current than gold.

In most practical applications, heat does not just conduct away through the wire but also conducts away in the radial direction from the surface of the wire through the epoxy-molding compound. The combined phenomenon is complex and not subject to analysis with closed-form equations but yields using finite-element modeling software with a thermal-electric-coupled physics solver to examine the effects of different wire parameters.

Model setup

A typical wire-bond process connects the chip's I/O pads to the package's leads with wires, predominantly gold or copper (Figure 1). Manufacturers limit the IC's maximum-ambient operating temperature to 70 °C for commercial applications; 85 °C for industrial uses. Most devices specify a 125 °C maximum chip-junction temperature.

WIRE DIAMETER	GOLD			COPPER		
(Mils)	1mm long	2mm long	3mm long	1mm long	2mm long	3mm long
2	4.075	2.11	1.425	5.45	2.8	1.89
1.3	1.8	0.97	0.665	2.41	1.275	0.87
1.2	1.563	0.847	0.58	2.065	1.1	0.76
1	1.12	0.625	0.435	1.475	0.81	0.56
0.9	0.94	0.525	0.368	1.225	0.677	0.47
0.8	0.76	0.435	0.309	1	0.55	0.394
0.7	0.612	0.355	0.254	0.787	0.45	0.322
0.6	0.475	0.28	0.203	0.608	0.355	0.255

Table 2: Summary of current values in Amperes for different wire combinations

To estimate the bond wires' current-carrying capacity under worst-case conditions, the models assume the industrial ambient temperature with the maximum chip junction temperature. Natural convection boundary conditions apply to the package surface, with the package lead temperature at 100 °C.

A small amount of current through the wire does not change the temperature profile across the span of the wire with the two ends still at the original temperature. As the current increases, the hottest temperature is no longer at the chip junction, but is somewhere in the middle of the wire span.

The glass transition temperature, Tg, of the mold compound is the temperature at which the material transitions from a hard and relatively brittle state to a soft, rubber-like one. A typical Tg is about 150 °C. If the current causes the mold-compound temperature to exceed Tg, time and temperature will degrade the epoxy's chemical bonds at this interface. This not only causes an increase in the thermal resistance of the mold compound, but also results in an increase in the porosity of the material, exposing it to the ingression of moisture and ionic contaminants. A wire-mold-compound interface temperature of 150 °C is, therefore, the upper temperature limit to calculate bond wire current-carrying capability.

With this as the criterion, the effects of wire-material type, wire length, and wire diameter are calculable and a comparison is possible to the theoretical estimates. Figure 2 shows the current-carrying capability of 1-mm-long gold wire using the three approaches. The current value using FEM starts out at about the same level that the modified Preece equation gave but then diverges as the wire diameter increases. The FEM analysis shows the current-carrying capability of gold and copper wires modeling 1-mm-long bond wires (Figure 3) and wires of several lengths (Table 2).

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FLEXIBLE POWER MANAGEMENT FOR COMPLEX PCBS

Flexible algorithm development, accurate supply monitoring, and rapid fault logging enhance product reliability.

By: Shyam Chandra

The number of power supplies on a board depends on the VLSI chip complement, the communication speed between them, and the number of other devices that require unique supplies.

This is because each of the ASICs and SoCs require multiple supplies to operate normally, including core, I/O, PLL, SERDES-channel, and memory-interface supplies. As a result, it's common for PCBs to have 15 to 25 rails. Boards with multiple power supplies typically need to implement power management functions that include power sequencing, supply-fault monitoring, trimming, and margining. Some boards may require enhanced power management functions, such as voltage scaling, non-volatile fault logging, and background sequence updating.

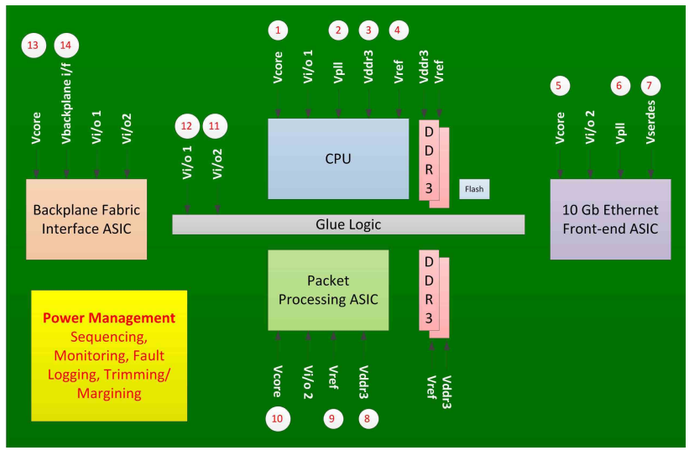

Figure 1: Communication line card primary ICs and powersupply requirements

PCB power management

For example, consider a line card with four main ICs and some glue logic (Figure 1). Each of the ICs requires multiple supplies and each imposes sequencing requirements. This board has 14 rails that need monitoring, sequencing, trimming, and margining. In addition, the board's design also requires logging supply faults in non-volatile memory.

When a board's designers initially create the power-management algorithm, they typically only consider device-dependent sequencing. This is because the designers will not know about the power-sequencing interdependencies among different rails. In general, to finalize the power sequencing during debug, the designers should consider seven types of changes to the original algorithm:

- Adjust the time delay between turning on each of the rails or rail groups.
- Rearrange the supply turn-on sequence.
- Set the supply turn-off sequence.

Minimize conditions where the board partially powers ICs that require multiple rails during a supply fault. For example, if supply 3 fails then the power manager may need to turn off supply 4 immediately and then supplies 1 and 2. If supply 1 fails, then the appropriate sequence may be different, say, supplies 2, 3, and 4 in sequence.

Generate power-good signals to various devices to get them to start operation. For example, CPUs require power-good signals not only for the core supply but also for DDR Memory, PLL, and I/O supplies.

Be able to monitor digital signals to complete sequencing. For example, wait for the packet-processing ASIC's PLL-lock signal before powering up DDR supplies.

Initiate power shut down on receipt of a digital control signal originating on the board or from elsewhere in the system.

After all of the supplies are on, the board starts to function normally and the power management section should begin monitoring the supplies for faults. When any supply fails, then—depending on the particular supply—the power manager should interrupt or reset the CPU to prevent Flash corruption. The monitoring section of the power-management algorithm should have the following four characteristics:

Identify faults of any local supply with an accuracy of 1% or better to minimize spurious supervisory fault indications and prevent missing power faults due to the supervisor's accuracy limit. This fault indication can generate an interrupt reset signal for the CPU.

Sense lower supply voltages—1.5 V or below—using differential signals to minimize errors due to ground-voltage differences between the power management circuit and the local supply.

Report faults within 100 µs to minimize the duration of faulty data or instructions due to a faulty supply.

Associate faults with the supervisory signals. For example, activate reset signal if supply 1, 2, 3 or 4 fails but if supply 12 fails, just interrupt the CPU to prevent faulty data transmission.

The fault logging function should log the primary reason for a board shutdown. In a PCB, an initial fault usually triggers secondary actions. For example, if supply 1 fails, the board shutdown function starts to shut off the remaining supplies as per a fault-response power-down sequence. If the fault logging circuitry reacts fast enough for the supply-1 failure, the log will show supply-1 fail and the remaining supplies healthy. If the response time for fault logging is slow, it will log supplies 2, 3, and 4 faulty as well. Such a fault log is not usable.

The fault logging circuit should measure supply faults accurately—within 1% error—to increase the reliability of the fault log. It should also initiate the fault logging process within 100 µs to minimize secondary effects of the original failure corrupting the fault log.

Implementation example

One common approach to implementing complex power management is to use power-good signals from DC-DC converters to monitor the supplies and use a CPLD to implement the sequencing algorithm to controlling DC-DC converter-enable signals. The CPLD also generates supervisory signals such as power-good, faulty-rail-interrupt, and reset signals (Figure 2).

This implementation brings six key advantages: It meets all

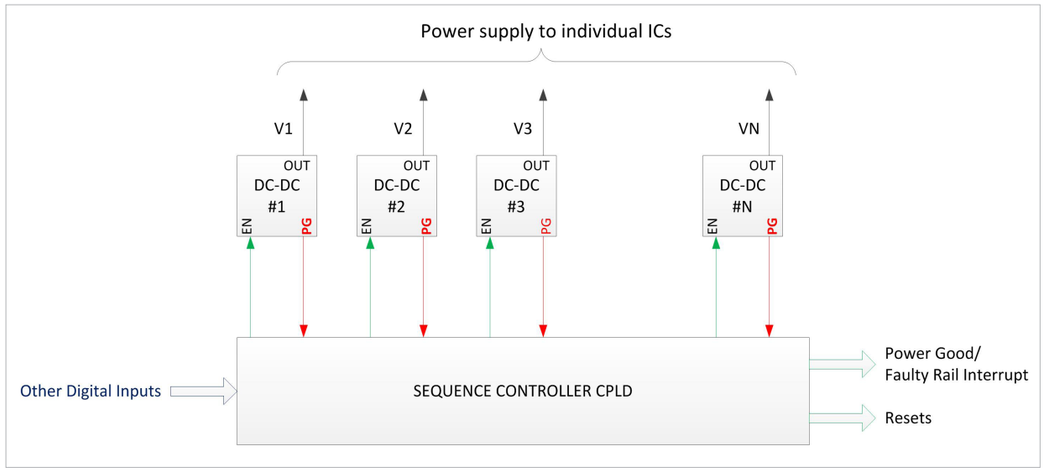

Figure 2: Power management using power-good signals vs. monitoring supply voltages

sequencing requirements. It's scalable with the number of supplies. There's no limitation on the power up or power down sequencing algorithm sizeor complexity. The sequencing algorithm can interleave supervisory signals such as power-good or faulty-voltage indications between supply sequencing. Any number of digital inputs can control the sequencing and monitoring algorithms. In-field upgrading procedures can update the sequencing algorithm without interrupting the board operation.

The implementation does, however, bring four disadvantages: An cctive power-good signal does not mean that the supply is within the client IC's supply tolerance. The power-good signals from most DC-DC converters have a monitoring error of 8 to 20% but most ICs' supply tolerances are between 3 to 5%. For example, the 1.2 V core-supply rail's voltage can be 10% below the rated value—1.08 V—but the DC-DC converter power-good signal can indicate that the supply is good and the CPLD may not activate its reset signal. Consequently, the CPU may hang and overwrite a section of the Flash memory. Systems should not use the power-good signal from a DC-DC converter as a supply rail fault indication to generate supervisory signals such as reset or low-voltage interrupt.

Often this type of supervisory system with enable some ICs before their supply voltages are within operating tolerances. As a result, sequencing algorithms wait for an additional time before enabling the ICs, and the board does not start-up reliably.

Increases software debug time – Due to the poor accuracy of the CPU and memory supplies' power-good signals Flash corruption can occur, increasing software-degug time. It is difficult to differentiate between a software bug and unexpected program behavior due to faulty supply. Because there is no way to determine the faulty supply in hardware, software engineers waste time blaming the software bug for Flash corruption before blaming the faulty board. This can cause a delay in product release.

Distributed sensing and centralized control

An alternative is to provide accurate remote sensing and centralized control (Figure 3). This architecture is similar to the previous circuit but, due to the integration of the comparators and ADC, it requires the least number of components. For example, a Lattice Platform Manager and two Lattice Power

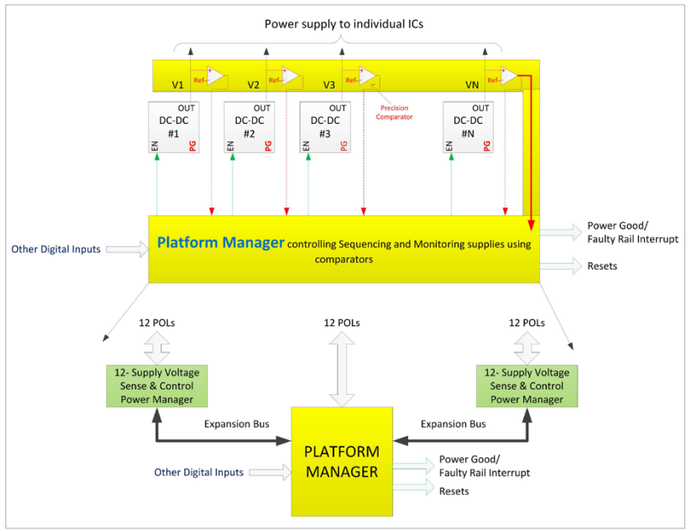

Figure 3: Distributed rail voltage sense and centralized control using platform manager

Manager ICs implement the arrangement and provide power management for up to 36 rails.

The Platform Manager integrates 12 supply voltage monitoring, a 48 macrocell CPLD and a 640 LUT FPGA. The Power Manager can sense and control up to 12 point-of-load supplies. The FPGA section of the Platform Manager implements the overall power-management algorithm and supports supply trimming and margining.

This approach brings seven advantages:

It provides flexible sequencing support for up to 36 rails because the FPGA implements the central power management. There is no limit to timing adjustment or sequencing response to each of the power failure conditions. The system generates supervisory signals with no compromise to reliability because the voltage monitoring accuracy is 0.7 %. In addition, because both the Platform Manager and the Power Manger support differential voltage sensing, they don't degrade measurement accuracy due to ground-voltage differences between various areas of the PCB.

Because the FPGA receives all supply-fault status signals, the algorithm responds to any fault within 100 µs and generates the supervisory signal immediately. This speed, coupled with high monitoring accuracy, minimizes the chance of Flash corruption.

The system can log any supply fault into non-volatile memory in 100 µs. This ensures that the fault log contains the primary fault.

Designers can implement the power-management algorithm using HDL code or using a simplified algorithm development tool called LogiBuilder. Engineers can simulate and fine tune the algorithm, minimizing the chances of errors that require a board re-spin.

In-field upgrading procedures can update the power-management algorithm without interrupting the board's operation. The device also stores a golden image, so if an event interrupts the in-system update, power cycling the board restores the previous algorithm and the upgrade procedure can begin again.

The communication between the Platform Manager and the Power Manager is simple and reference designs are available. The user simply adds the reference design to the board power-management algorithm. The reference design automatically manages the communication among all devices without intervening in the main power-management algorithm.

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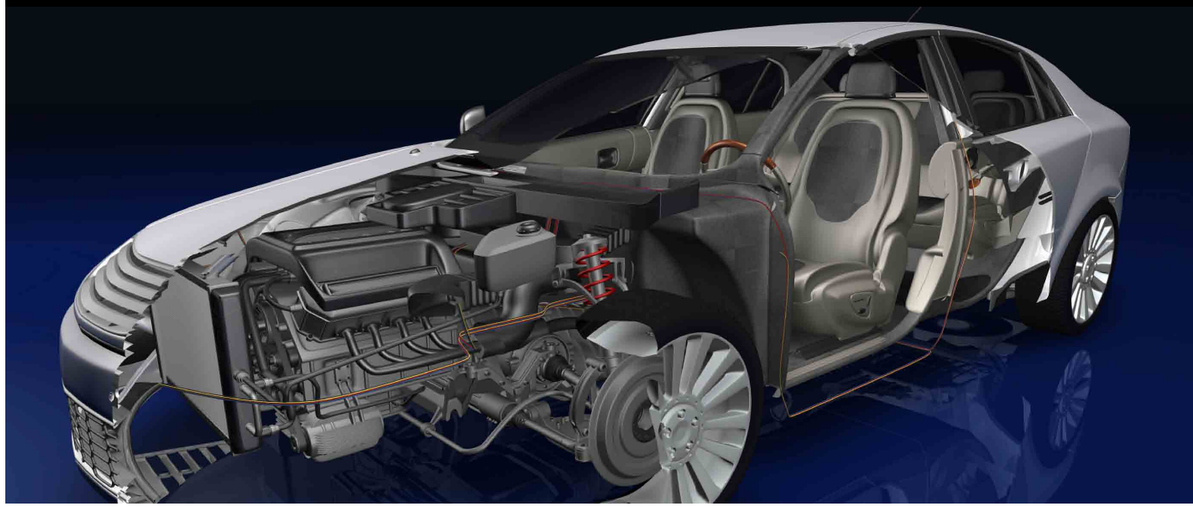
Special Report: Automotive

PSD EUROPE
Power Systems Design: Empowering Global Innovation



Inside:

SLEEPING CONSERVES ENERGY

How to reduce the power consumption of CAN networks using the Partial-Networking Mode

By: Fritz Burkhardt

Minimizing energy consumption has become a major factor for any new product design in recent years.

Hardly any industry can afford to disregard this issue in the definition, development, or marketing of their products and the automotive industry is no exception. Manufacturers have made significant efforts towards reducing fuel consumption by efficient engine management and weight minimization. Meanwhile, developers are focusing on the vehicle's electronic functions as well.

Until now, the use of low-power electronic-control units was particularly important for parked vehicles in order to achieve maximum standby times with existing battery capacities. In the meantime, however, current drain has become important for driving vehicles as well because the combustion engine must deliver the electrical energy with a direct influence on fuel consumption.

Comparatively low fuel consumption is a key selling point because it immediately affects operating costs for the car owner. Today, however, another factor complements this perspective.

The reduction of greenhouse-gas emissions, which are harmful to the earth's climate, has been the goal of many initiatives of the international community. Consequently, the European Parliament passed a regulation stating mandatory limits for the CO_2 emissions of new vehicles. The regulation fixes severe penalties for violating these limits to ensure that car manufacturers assume their responsibility to reduce their products' energy consumption.

The e-mobility trend may emerge as an additional motivation in the future: Minimizing energy consumption will become more and more important in electric vehicles whose operating range will be a significant factor for this technology's acceptance.

Apart from factors including engine efficiency, vehicle weight, and aerodynamic drag, the power efficiency of the electronic control units is a wide field of activity for designers willing to save energy.

Analyzing the electronics landscape in modern vehicles quickly yields several observations: The vehicle does not require all of the functions that the many control units offer all the time and in every driving situation. The continuous current drain these modules impose isn't, therefore, always necessary. This is particularly true for convenience functions including seat electronics, trailer-control units, or tailgate-control units because these functions only rarely operate or because they are not necessary all the time. Additional examples include door-control units, auxiliary heating, sunroofs, and rear-view cameras. On the other hand, it must be possible to activate these control units at any time in order to avoid any functional or convenience impairment.

For example, assume an average current drain of 100 to 150 mA and a battery voltage of 14 V, potential saving amounts to 1.4 to 2.1 W for each idling control unit. Total energy savings for 20 CAN nodes capable of partial networking therefore amount to an average of 35 W without any negative impact on functions or convenience features.

According to the established conversion formula, 40 W of electrical power represent 1.0g of CO_2 emissions per kilometer. Thus, the introduction of partial networking leads to potential emission reductions of 0.85 grams of CO_2 per km.

The aforementioned EU regulation stating a violation penalty of €95 for each gram of CO_2 per kilometer yields potential savings of approximately €80 Euros per vehicle for car manufacturers.

But there are even more reasons why designers should consider opportunities for partial networking. These includes the charging of electric vehicles. Although this requires a communication link to the supervising control unit, most of the control units that connect to the bus are not necessary for this task and thus the vehicle can selectively power them down.

The same is true for future application scenarios entailing data transmissions between a parked vehicle and mobile end devices. These future-use cases also result in increased requirements regarding the operating life of the components. Partial networking can compensate for this to a certain extent, resulting in reduced costs, which explains the industry's intensive efforts to exploit this potential.

At the Fachkongress Automobil-Elektronik, which took place on June 8, 2011 in Ludwigsburg, Germany, German OEMs jointly announced starting volume production of CAN partial networking in the short and medium term.

Although current CAN nodes already provide low-power modes, such as standby and sleep, they immediately wake up if any communication occurs on the bus. These low-power modes are thus only useful if all nodes on the bus disable simultaneously— a so-called bus idle— as is the case for a parked vehicle. When any message source transmits data on the CAN bus, transceivers wakeup all connected nodes. Consequently, individual control units cannot remain in sleep mode while communication on the bus is ongoing.

One suitable approach divides the network into sub-networks and disconnecting specific controllers from the supply voltage. Apart from the restrictions regarding the network layout, using multiple power supplies leads to additional overhead. Nonetheless, designs of

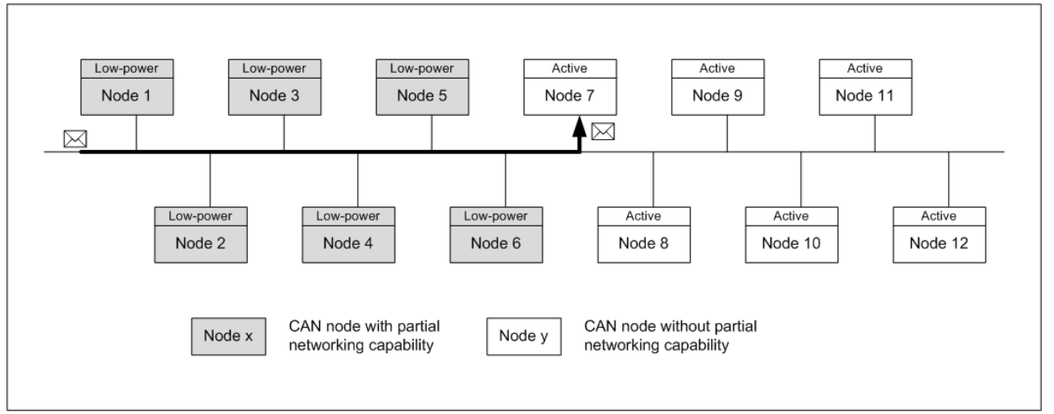


Figure 1: CAN network with partial-networking controllers during the transmission of a message to ECU7 (without partial-networking support)

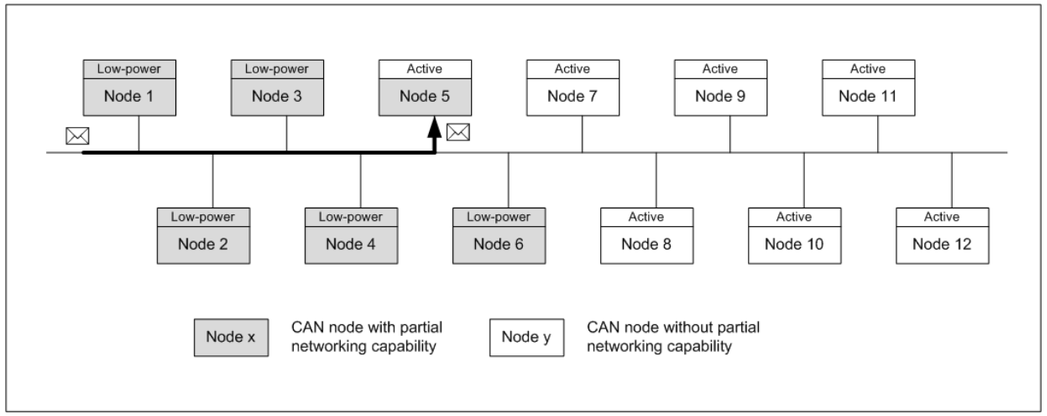


Figure 2: CAN network with partial-networking controllers during the transmission of a message to ECU5 (with partial-networking support)

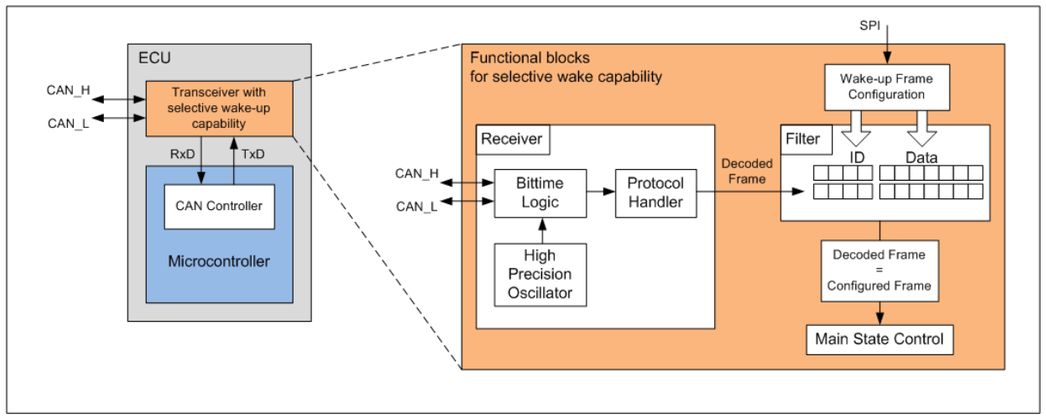


Figure 3: Functional blocks of a partial-networking transceiver

this kind are already in use today.

Obviously, the most flexible approach is to wake up specific nodes using dedicated, predefined wake-up messages. To support selective addressing, CAN controllers in a sleep or standby mode must be able to monitor CAN messages for previously-negotiated wake-up messages and to respond only if necessary.

Consider, for example, a network consisting of 12 nodes (Figure 1). Six nodes support partial networking while the remaining units use conventional transceivers without this capability. When the bus is active and a message addresses Node 7, Nodes 7-12 are active due to the ongoing bus communication while Nodes 1-6 remain in low-power mode because they did not receive a selective wake-up message.

Now consider a second scenario in which Node 5 receives a selective wake-up message (Figure 2). This node recognizes the wake-up request and enters active mode. Nodes 7-12 remain active also due to the ongoing bus communication while nodes 1-4 and 6 remain in low-power mode. Ideally, the detection of wake-up messages should occur in the transceiver because this is the only way to avoid activating the microcontroller with the resulting increased current drain.

The strength of conventional transceivers is their bus-level translation capability with full signal fidelity and immunity to external noise signals and bus interference. Having only very basic logic functions for detecting simple bus errors, every bus edge activates them. This, in turn, precludes capturing and evaluating any incoming messages because this is the task of the MCU's on-board CAN controller, which has the precise reference clock necessary for evaluating the message.

CAN transceivers capable of partial networking therefore need a highly precise internal reference clock in order to reliably capture and decode the incoming bitstream. In addition, this reference clock must be stable in the relevant temperature range. Considering the maximum tolerance of the transmitting node and common disturbances on the bus, including blurred edges, reflections, and EMI, the oscillator must provide precision of < 1% over the entire temperature range from -40 to +105 °C for the operating life of the component. The oscillator concept used in partial-networking transceivers therefore plays a primary role and represents the main challenge during the development of these devices.

The node must then extract the information payload from the bitstream according to the CAN protocol before the node can compare the data to its previously-configured wake-up message. The transceiver must thus provide an interface for configuring the partial networking mode and the dedicated wake-up message (Figure 3).

As mentioned above, car manufacturers are working hard to bring partial networking into volume production. However, these efforts will only be successful if the industry can standardize transceiver features.

For this purpose, a working group called SWITCH (Selective Wakeable Interoperable Transceiver CAN Highspeed) is preparing a standardization proposal based on a relevant requirement specification. The proposal is currently under discussion with the International Standardization Organization to define a supplement for ISO 11898 (Road Vehicles – Controller Area Network CAN). STMicroelectronics is contributing to the definition of this functionality and is working on the implementation of suitable transceivers.

The company has worked closely with a major German car manufacturer, which is running in-vehicle tests on a first device. The company expects to be in volume production of the device in Q4 2012.

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HALL EFFECT CURRENT SENSING IN HEVS AND EVS

Wide bandwidth and inherent galvanic isolation simplify current measurements in demanding automotive applications.

By: Shaun Milano, Michael Doogue, and Georges El Bacha

Consumers are embracing environmentally friendly green cars due to the rising cost of fossil fuels and a growing concern for the health of the environment.

Sales forecasts predict that green cars will comprise 3% to 4% of all vehicle sales by the year 2016. After 2016, estimates call for a more rapid adoption of green cars, with green car market share ranging from 8% to 19% in 2021. The most popular green car, both today and in forecasts through 2021, is the HEV (hybrid electric vehicle).

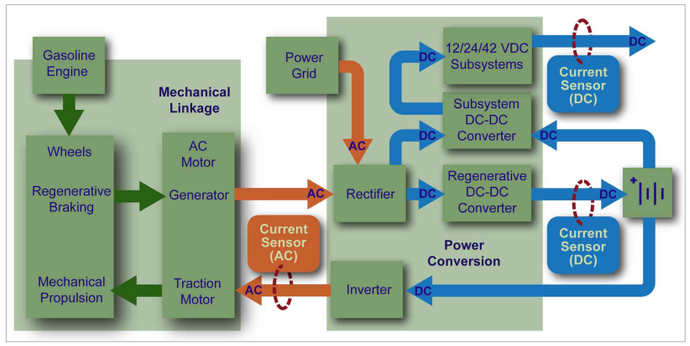

Figure 1: Typical HEV system block diagram.

HEVs employ complex power electronic circuitry to control the flow of electric energy through the vehicle. In a single motor HEV, the motor acts as a traction drive in parallel with the internal-combustion engine, or as a generator to charge the battery during regenerative braking. Both HEVs and EVs (electric vehicles) contain various systems that require electrical current sensors for maximally efficient operation, including AC-motor and DC-DC-converter applications.

The HEV Power Cycle

In the HEV power cycle the power converter inverts the main battery voltage and applies the resulting AC voltage to the traction motor, which in turn drives the wheels (Figure 1). During regenerative braking, the AC motor also serves as a generator. When the regeneration system is active, the power converter rectifies the output of the motor-generator to a DC voltage sufficient to charge the HEV battery cells, completing the power cycle. For EVs and plug-in HEVs, the power converter also rectifies the line voltage to charge the battery.

The regenerative braking process is a primary contributor to HEV's and EV's energy efficiency because the power converter partially recovers braking energy normally wasted in the form of heat, and uses it to charge the main battery. To power the low voltage infotainment and body-control subsystems in the car, a DC-DC converter reduces the battery voltage—typically 300 to 500 V—to a lower-level DC voltage.

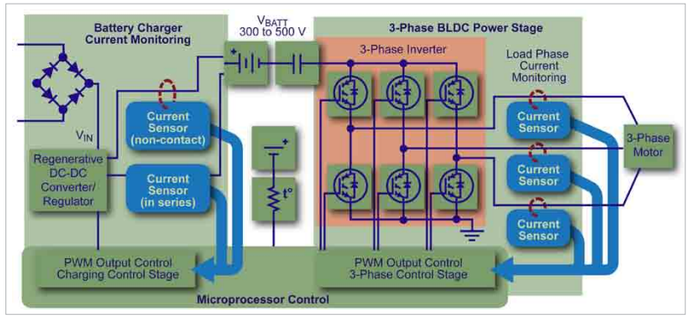

Figure 2: DC-DC converter charger (left) and 3φ DC-AC Inverter (right).

One drawback of conventional Hall-effect sensors in current sensing applications has been a general limitation in both accuracy and output signal bandwidth. Signal-processing and package-design innovations enable new Hall-effect current sensors with > 120 kHz output bandwidths, low output phase shift, high current resolution, and low noise spectral density.

Current Sensing in Inverter Applications

The driver in a typical inverter converts DC battery voltage to a 3φ AC voltage that the traction motor requires for efficient operation (Figure 2). Current sensors measure the three inverter phase currents and, typically, a controller uses the resulting information to control the PWM inverter switches—usually IGBTs. The inverter control loop requires high-bandwidth current sensors to improve accuracy, maximize motor torque, and maximize overall motor efficiency. High-side current sensors with fast response times also enable overcurrent protection during short circuit conditions from a motor phase to the system-ground node.

For example, the Allegro A1360 linear Hall device meets the voltage isolation, > 200 A load current, and high-bandwidth demands of HEV inverter applications. The Hall-effect sensor IC typically locates in the gap of a ferromagnetic toroid which surrounds each inverter phase conductor in the motor (Figure 2). As current flows in the conductor, the toroid concentrates the resulting magnetic field through the SIP (single inline package) device. The transducer provides an output voltage proportional to the current. The device is available in a proprietary, 1 mm thick package that reduces eddy current losses to improve sensor output bandwidth when compared to conventional IC packages.

The A1360 and similar devices have a typical output bandwidth as high as 120 kHz and offer high-resolution high-accuracy performance that allow for high-speed control of the PWM switches in an inverter system. Additionally, these SIP sensors offer a 3 µs output response time for IGBT over-current protection applications. The form factor of this current-measurement circuit is also smaller than current transformers. Nonetheless, it provides the necessary galvanic isolation because the sensor IC output leads do not connect to the high-voltage current-carrying conductor in each of the motor's phases.

Electric Motor Control

A prominent trend for improving energy efficiency in HEVs and EVs (and, to a lesser extent, in internal-combustion engines with idle-stop capability) has been the conversion of belt-driven and hydraulic actuators to electrically-driven actuators. For instance, in traditional internal combustion engines a fan belt drives the cooling fan, which operates continuously while the engine is running. The same applies to power-steering pumps and other belt-driven loads.

Replacing belt-driven actuators with electric motors improves energy efficiency and allows for greater control of the actuators. Precision, high-speed current-sensor ICs provide the bandwidth, response time, and accuracy performance necessary to optimize motor performance but must meet qualifications for the demanding under-hood environment.

DC-DC Converters

The current sensing range and the isolation voltage determine the optimum current-sensor IC pack-

age for use in DC-DC converters. Current sensors in DC-DC converters often must sense current in a spectrum that includes DC. This requirement precludes current transformers in fully optimized systems. Using shunt resistors in these applications is also challenging because the high input or output DC voltages require expensive, high-common-mode input operational amplifiers. A Hall-effect sensor with inherent galvanic isolation, wide current bandwidth, and a transduction response that extends to DC is a logical choice for DC-DC converter applications in HEVs.

A regenerative converter uses a current-sensor IC that can operate at traction-battery voltages. Accurately sensing the converter output current is a critical function because correctly metering the charge current that the converter delivers to the HEV battery extends its operating life.

The ACS714, for example, is a current-sensor IC suitable for many lower current, subsystem DC-DC converter applications. The ACS714 is a factory-trimmed, galvanically-isolated sensor IC available in an extremely small form factor SOIC-8 package with an integrated 1.2 mΩ conductor for low power loss. For higher-current applications, current sensor ICs such as the Allegro ACS758 incorporate a 100 μΩ conductor and a ferromagnetic core into a small form factor galvanically-isolated package capable of sensing 50 through 200 A. For greater measurement ranges, the SIP based toroid configuration mentioned earlier can sense currents above 200 A.

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NON-CONTACT DRIVER'S ECG MONITORING SYSTEM

Heart-rate variability analysis allows inference of driver awareness and fitness to drive.

By: Shrijit Mukherjee, Robert Breakspear, and Sean D. Connor

EPIC (Electric Potential Integrated Circuit) is a very-high-impedance electric-field sensor that measures the ambient electric field with minimal disturbance.

EPIC sensors are suitable for applications that depend on the measurement of the change in the ambient E-field. One EPIC application relates to non-contact measurement of ECG (electrocardiogram) signals from a car's driver, with a wireless interface that allows continuous monitoring of the driver's health.

Recent developments have resulted in a reliable technique for measuring the ECG through clothing, by means of sensors embedded in the drivers' car seat. A Bluetooth interface transmits data to a monitoring system or a mobile phone or tablet. The receiving system may monitor the data in real time or subsequently send it over mobile or cloud-computing networks for analysis.

Consider the EPIC sensor as a near-perfect voltmeter, which exhibits almost no loading affect

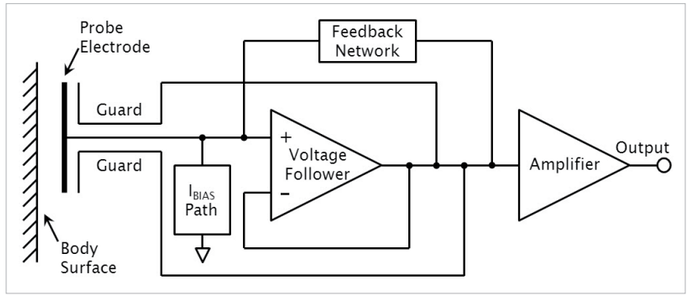

Figure 1: Block diagram of a typical EPIC sensor

to the signal it measures (Figure 1). The probe electrode does not require an ohmic contact with the subject's body, making the setup inherently electrically isolated. The EPIC product line includes sensors with bandwidths in the range of ~0.01 Hz to 100 kHz. This bandwidth is controllable either during the application-specific design stage or by changing external components. The sensor's AC operation makes it insensitive to static electric fields, which include earth's electric field. This ensures stable operation over its entire operating frequency.

For the spatial measurement of cardiac signals, the electrical activity of the human heart results in a well characterised ECG signal, readily detectable by suitable capacitively-coupled sensors. Off-body ECG measurement using a differential pair of sensors with some additional circuitry has been tested with an in-situ driver heart monitoring setup, where the driver's heart rate was monitored whilst driving. A Bluetooth interface wirelessly transmitted the sensor data to a mobile device. This configuration can capture ECG data for heart-rate variability analy-

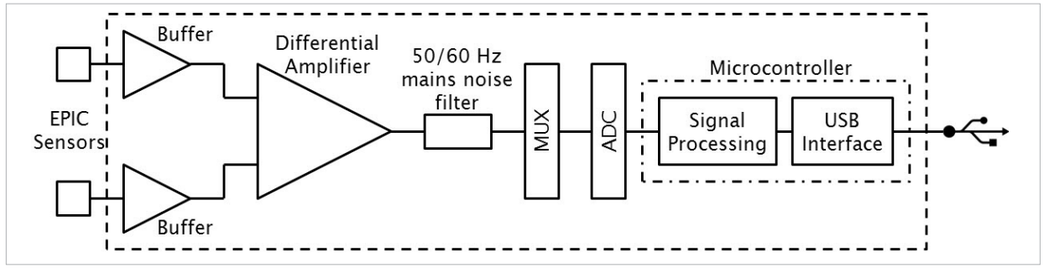

Figure 2: Block diagram of an ECG monitoring system with USB interface and relevant signal conversion and processing.

sis to infer important psychological and physiological information such as levels of driver awareness and fitness to drive.

ECG measurement system

ECG measurements usually use a pair of EPIC sensors. The electrodes have a dielectric capping layer, which isolates the subject's body from the sensor and provides a capacitive interface negating the requirement for conventional resistive contact. The sensors can operate through several layers of clothing or across a small air gap.

The monitoring-system electronics comprise the differential signal, which passes through amplification stages and feeds through a 50/60 Hz filter to eliminate mains supply signal present in the vicinity (Figure 2). A microcontroller with an ADC input digitises the signal and digitally filters the resultant data stream. At present, the ECG system has both USB and Bluetooth interface to support local and remote data analysis. Figure 3 shows images with the driver inside a car with the sensor and data-acquisition system.

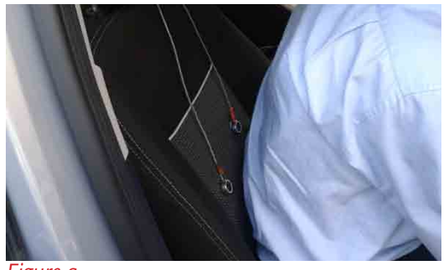

Figure a

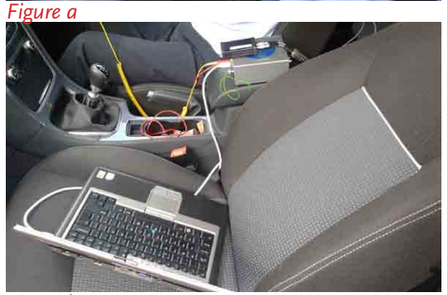

Figure b

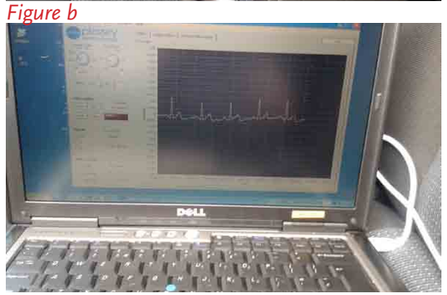

Figure c

Figure 3: The sensors mount on the driver's seat back (a) with the signal processing, data acquisition and visualization (b) and an ECG trace from the system captured whilst the car was in motion (c).

Driven-right-leg approach

Movement, artifacts, and environmental noise greatly affect signal quality. When driving the car, the driver constantly makes slight adjustments to limb position and, accordingly, produces motion artifacts. The sensing system has incorporated a DRL (driven right leg) approach to address this issue.

A DRL requires feeding back the noise signal to the subject's body in antiphase, which works as a noise cancellation technique. This system uses a conductive fabric around the steering wheel and on the driver seat, with the feedback signal connected to it and thus capacitively coupled back to the driver. This results in an increased dynamic range, which helps both in reduction of the movement artifact and stops the sensors from saturating.

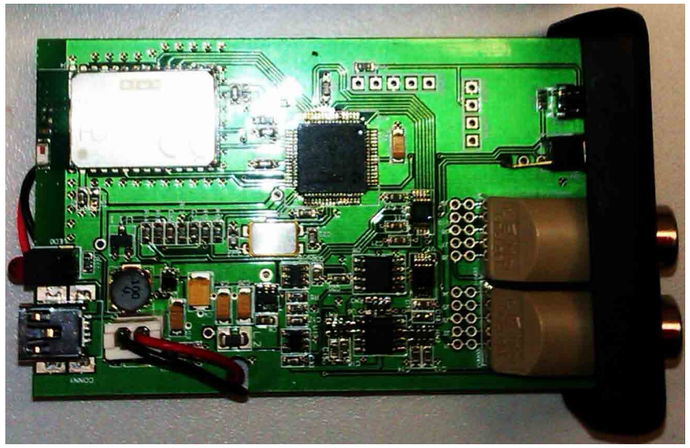

Figure 4: A Bluetooth module for wireless transmission of sensor data.

The Bluetooth interface for the EPIC ECG sensors is a battery-powered unit with differential input sensor ports, a 14-bit ADC, a high data rate Bluetooth 2.1 module with integrated radio antenna and protocol stack, onboard filtering, and gain blocks (Figure 4). The wireless ECG monitoring system for in-situ driver heart monitoring incorporating novel EPIC sensors provides off-body ECG monitoring, eliminating the need for conventional Ag-AgCl resistive-contact ECG electrodes. Future work will integrate the Bluetooth module and sensor pack into a single unit.

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IMPROVING ENGINE STOP-START SYSTEM DESIGN

Integrated MOSFET controllers help engineers overcome electrical challenges in automatic engine stop-start systems.

By: David Jacquinod

Automatic engine stop-start is effective in helping reduce CO_2 emissions from private cars.

When integrated in an otherwise conventional combustion-engine power train, engine stop-start technology can deliver fuel savings of 5 to 15% at a relatively low incremental cost of about 300 USD. Offering worthwhile reductions in fuel consumption and emissions, at a price accessible to a significant proportion of car buyers, the stop-start vehicle is an important staging point in the transition to so-called mild hybrids or full hybrids and, ultimately, plug-in electric vehicles. Market analyst Yole Développement predicts strong demand for stop-start vehicles, rising from 5 million vehicles in 2012 to some 45 million in 2020.

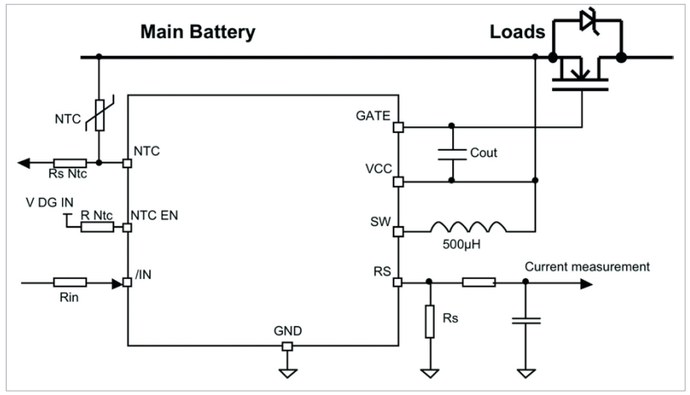

Figure 1: Integrated gate driver with external passive components.

Electrical design challenges

Automatic engine stop-start challenges several areas of vehicle electrical design. One is to protect systems such as the radio, climate control, GPS, and interior or exterior lights against supply-voltage fluctuations during engine cranking. The battery voltage can fall to as low as 6 V during cranking, whereas the electrical systems require a stable supply, or board-net voltage, of 13 V nom to ensure correct operation. Hence an additional subsystem is needed, containing a power switch and associated control circuitry, to disconnect the battery when the engine is cranking, allowing an auxiliary battery or DC-DC converter to supply the loads temporarily.

When the vehicle is operating normally, the power switch contained in this subsystem must supply all electrical loads in the car. Consequently, low conduction losses are imperative because the switch is on at all times except when cranking. This calls for a power MOSFET rated for continuous drain current on the order of 240 A and having low on-state resistance of about 1 mΩ. Connecting several devices in parallel can achieve a further reduction in on-state resistance. Because the battery must remain connected when the car is off, the power switches and the controller, combined, must have a low quiescent current to minimise battery drain. A quiescent current of around 50µA is acceptable.

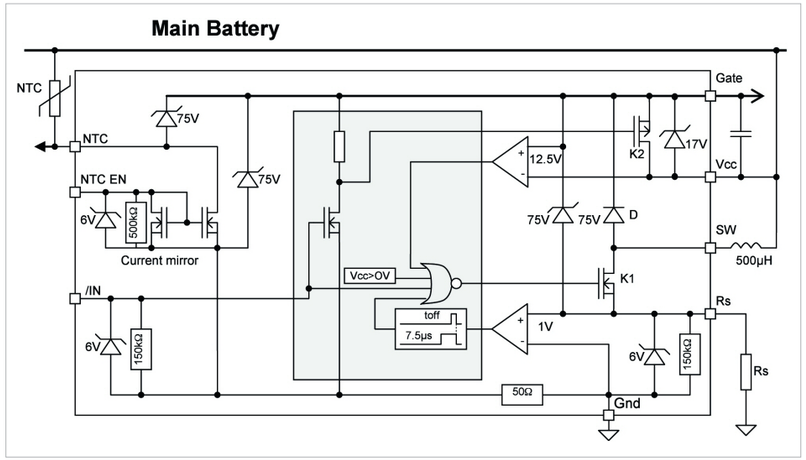

Figure 2: Internal functions of the start-stop gate driver

Controlling the power switch

As soon as the vehicle's auto-start function activates engine cranking, the main battery voltage begins to fall. The power switch must turn off quickly to allow the auxiliary supply to maintain the board-net voltage at 13 V. This is important, because the low resistance of the power switch can allow a high current to flow to the main battery side with a voltage drop of only a few mV. The turn-on time is less critical because the current will flow in the power switch's body diode.

A controller, or gate driver, is necessary to turn on and turn off the power switch. A suitable controller must be capable of providing a gate voltage of 12 V to 15 V when operating from the low main battery voltage. Additional circuitry performs voltage and current monitoring, on- and off-time control, fault diagnostics, and thermal protection.

Designing a driver having low quiescent current and meeting all these requirements, using discrete components, is challenging. Some integrated gate-driver ICs are available, which not only simplify design but can also help increase reliability. However, many are primarily for such applications as mobile phones or PDAs.

IR's AUIR3240S is an example of gate driver ICs for automotive engine stop-start applications. It contains a voltage converter capable of operating from an input voltage in the range 4 V to 36 V and provides a MOSFET-gate drive voltage of 12.5 V. The company optimized the device architecture for intermittent operation, reducing current consumption to less than 50 µA. The gate driver requires only a few external passive components to complete the design: an inductor and a capacitor for the boost converter and resistors for the IC's diagnostic and measurement circuitry (Figure 1).

Key functions include the main DC-DC switch, K1, and freewheeling diode, D, and two comparators to control K1's state (Figure 2). The uppermost comparator monitors the gate voltage compared to VCC, to turn K1 on. The lower comparator monitors the voltage across the shunt resistor connected to the RS pin, which controls the turn off.

A monostable timer with a typical interval of 7.5 µs guarantees a minimum boost converter off time. It activates when the inductor current reaches the peak current fixed by the shunt resistor (Figure 3).

The driver operates at variable frequency. K1's on time depends on the values of supply voltage, shunt resistor, and inductor. The output current fixes the off time. When the output voltage is below 12.5 V, the driver turns on the power MOSFETs and the monostable timer's off time, Toff, fixes the frequency. In this mode, the

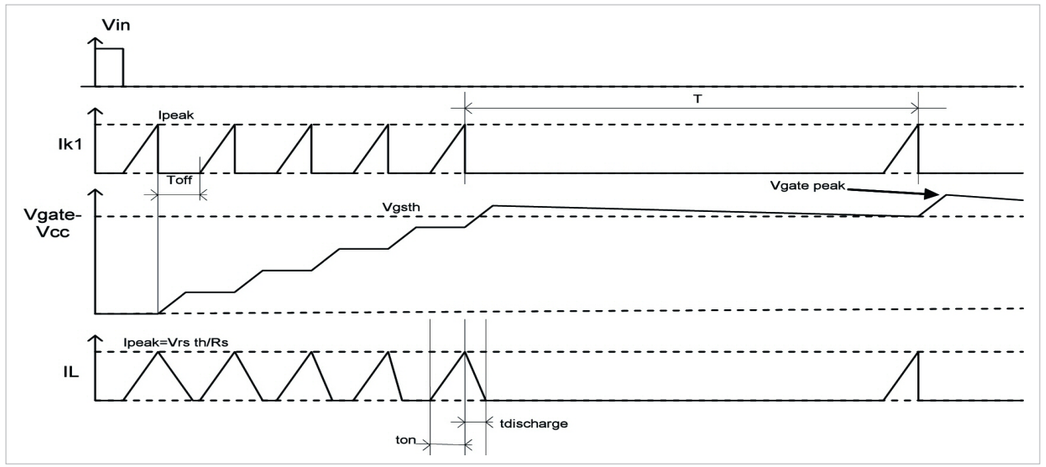

Figure 3: AUIR3240S driver voltage and current waveforms during turn on.

driver can provide a relatively large current—on the order of tens of mA—to charge the MOSFET gates quickly and turn on the power switch. The stop-start system can achieve maximum output current by optimising the values of the inductor and the shunt resistor.

Once the gates of the power MOSFETs charge above 12.5 V, the driver enters a low-current-consumption mode. Then the driver activates only when the gate voltage falls below 12.5 V. With this architecture, the driver can hold the power switch on, with very low current consumption. Gate discharge is mainly due to the driver's leakage current.

Safety and temp monitoring

Since the power switch supplies all the electrical loads in the car, it is a safety relevant function and must be able to detect failures. The AUIR3240S provides two diagnostic mechanisms for monitoring both correct output current and excessive system temperature.

By adding an RC filter to resistor RS, the system can monitor the average output current (Figure 1). The values of current flowing in the output and at the RS pin link by:

$$I_{OUT}(avg) = I_{Rs}(avg)\frac{V_{CC}}{V_{GATE} - V_{CC}}$$

In low-current-consumption mode, with current of 50µA and RS equal to 10 Ω, the voltage reading will be 0.5 mV. If a short circuit is present at the output, the driver will try to regulate the output resulting in a voltage of several hundred mV depending of the values of L and RS. Additionally, when the system operates to turn on the power MOSFET, a peak current will charge the gate. By monitoring the current during the turn-on, the system can detect continuity between the MOSFET and the output.

The driver provides an NTC interface allowing the system to monitor the MOSFET die temperature, using one standard resistor and one NTC device located close to the MOSFET's source. The circuitry operates as a current mirror between the NTC_EN and NTC pins. The ratio is typically 2:1 so 500 µA must flow in the NTC_EN to achieve a current of 1 mA in the NTC pin. R_Ntc and V_Dg_In determine the NTC current. For example, 7 kΩ and 5 V will result in an NTC current of 1 mA.

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VEHICLE ELECTRIFICATION SPARKS ENGINEERING DEMAND

By: David G. Morrison, Editor, How2Power.com

Though electric vehicles (EVs) and hybrid electric vehicles (HEVs) only account for a modest percentage of overall car sales, the sales of these more-electric vehicles are on the rise. According to a forecast by Pike Research, annual sales of EVs and HEVs will reach 2.9 million vehicles by 2017.[1]

Meanwhile, vehicle electrification is also taking root in the commercial and industrial markets. For example, another firm, IDTechEx, predicts that sales of heavy industrial vehicles like cranes and forklifts will grow nearly 70% over the next five years, reaching 763,000 vehicles in 2017 (Table 1.)[2] These growing EV and HEV markets have been creating numerous design challenges and career opportunities for power electronics (PE) engineers, as documented in prior articles.[3,4,5,6] But one issue that may have received little attention previously is how these design challenges and opportunities are cropping up in various segments of the automotive industry and at different points in the supply chain.

A recent survey of automotive industry websites reveals job opportunities in several types of companies. You can view a listing of these job openings in the online version of this article. As might be expected, there are opportunities for PE engineers at the larger, more-established automotive companies such as Ford and the tier 1 suppliers such as Delphi and Continental. But there are also a number of opportunities for PE engineers at EV specialist companies such as Tesla Motors, VIA Motors, and GreenTech Automotive. Similarly, there are companies specializing in electric power train and propulsion technology such as Mission Motors and AC Propulsion that seek experienced PE engineers.

But there's also another dynamic segment of this industry that needs power electronics expertise—the battery companies who are developing the advanced cells, packs, and systems that will be critical to the success of new EV and HEV designs. These companies need EEs with various PE skills to address battery management issues and develop related hardware. The list of these companies currently seeking EEs includes the likes of Dow Kokam, Sion Power, Valence Technology, and Johnson Controls.

Regardless of where engineers

Vehicle type	Unit sales	
	2012	2017
Heavy Industrial (includes mobile cranes, forklifts, and trucks)	453,000	763,000
Buses	22,000	58,000
Light Industrial/Commercial (catch-all category that includes a golf carts, airport baggage transports, lawn mowers, and many other miscellaneous types)	263,000	333,000

Table 1. Current and projected sales of commercial and industrial electric and hybrid-electric vehicles (Data courtesy of Dr. Peter Harrop, Chairman of IDTechEx.)

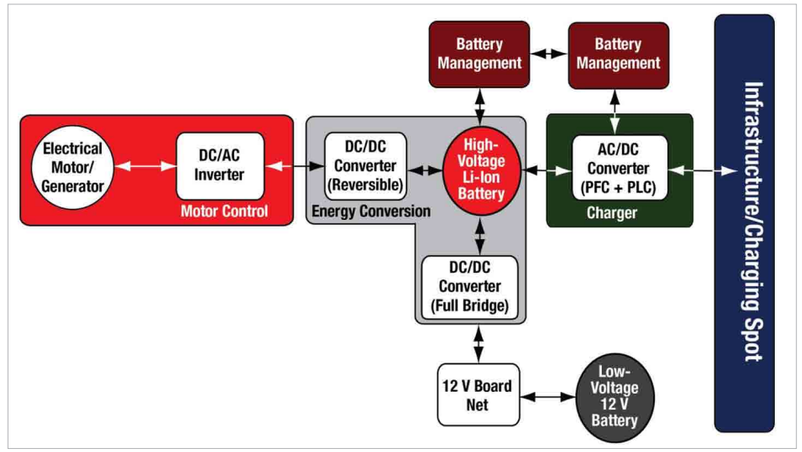

Figure. An example power system architecture for a hybrid electric vehicle. (Courtesy of Texas Instruments.)

are in the automotive supply chain, there is an imperative to develop solutions at the lowest possible cost. This goal takes on even greater significance in the development of EVs and HEVs, since the industry is trying to reduce the price premium associated with these vehicles. Naturally, this issue impacts the design of all the power electronics functions.

Table 1. Current and projected sales of commercial and industrial electric and hybrid-electric vehicles (Data courtesy of Dr. Peter Harrop, Chairman of IDTechEx.)

Gary Cameron, currently Director—Advanced Electronic Controls Engineering at Delphi, has pointed out that the techniques for managing power in electric and hybrid-electric vehicles are understood, but the cost of implementing the various power conversion and power management functions needs to be driven down.

"The big challenge is doing them at an affordable cost. If you're going to convert a large percentage of the vehicles produced into electric drive power trains, you've got to get the cost closer to parity with the alternatives. They continue to make improvements in internal combustion engines, diesel, gas, etc. but they're still going to need electrification. The overall car can't be too expensive for the public to buy," says Cameron.

Technology Developer	Partner	Description	Type
A123	Fisker	A123 has invested $23 million in Fisker and will supply batteries as well.	PHEV
NEC	Nissan	Supply packs for PHEV, HEV, and EV.	P/H/EV
Argonne National Laboratory (ANL)	LG Chem, GM, Toda Kogyo, BASF, Envia Systems	ANL has licensed its composite NMC cathode material to numerous corporations.	P/H/EV
BYD	Daimler	BYD and Daimler formed a joint venture called Shenzhen BYD Daimler New Technology to develop an EV for the Chinese market.	EV
Envia	General Motors	GM Ventures invested $7 million in Envia.	--
GS Yuasa	Mitsubishi; Honda	GS Yuasa and Mitsubishi formed a joint venture to produce Li-ion batteries called Lithium Energy Japan; GS Yuasa and Honda formed a joint venture to produce Li-ion batteries for HEVs.	EV; HEV
JCI-Saft	Ford	JCI-Saft supplies batteries to Ford for a PHEV.	PH/EV
LG Chem	Eaton, Ford, GM, Hyundai, Volvo	LG Chem has secured numerous supply relationships for vehicles across the spectrum.	P/H/EV
Panasonic	Toyota	Panasonic and Toyota formed a joint venture called Primearth EV Energy to create battery packs for Toyota.	P/H/EV
Sanyo	Audi, Volkswagen, Suzuki	Sanyo has supply contracts with multiple OEMs for Li-ion batteries.	P/H/EV
SB LiMotive	BMW, Chrysler, Volkswagen	SB LiMotive is a 50:50 joint venture between Samsung SDI and Bosch, and has secured supply relationships with multiple automakers.	EV
Shin-Kobe	Hitachi	Hitachi and Shin-Kobe formed a JV Hitachi Vehicle Energy that will supply batteries for 100,000 GM HEVs through 2015.	HEV
Toshiba	Mitsubishi	Toshiba will supply its SciB batteries to Mitsubishi for its Minicab i-MiEV	EV

Table 2. Key Partnerships in Electric Vehicles (Source: Lux Research).

Fig. 1 shows the block diagram of an example power system architecture in a hybrid electric vehicle,[7] identifying the key power functions that PE engineers are working to develop with low-cost and other performance goals in mind.

In this diagram, the main traction battery is depicted in red, looking like the very heart of the system that it is. Perhaps, then, it is not surprising the amount of industry attention that is now focused on advanced battery development, which is evidenced by the numerous partnerships between automakers and battery developers. The chart in Table 2, provided by Lux Research,[8] highlights the various industry alliances to develop better, more-economical batteries for electric vehicles and hybrids. These alliances also suggest potential sources of employment, now or in the future, for PE engineers looking to play a role in putting more EVs and HEVs on the road.

About the Author

When he's not writing this career development column, David G. Morrison is busy building an exotic power electronics portal called How2Power.com. Do not visit this website if you're looking for the same old, same old. Do come here if you enjoy discovering free technical resources that may help you develop power systems, components, or tools. Also, do not visit How2Power.com if you fancy annoying pop-up ads or having to register to view all the good material. How2Power.com was designed with the engineer's convenience in mind, so it does not offer such features. For a quick musical tour of the website and its monthly newsletter, watch the videos at www.how2power.com and http://www.how2power.com/newsletters/.

David G. Morrison
Editor

How2Power.com

COMETH THE HOUR, COMETH THE MAN

By: Gail Purvis, Europe Editor, Power Systems Design

When BASF, Bosch, Merck, and Schott throw a combined weight and €300M in funding behind the German Ministry of Education & Research energy self-sufficient homes OPV (organic photovoltaics) project, it is worth watching.

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When that combines with the 2012 'Umsight' science award to Dr Jan Meiss for "New material concepts for organic solar cells," in cooperation with Heliatek GmbH and Fraunhofer IPMS – COMEDD achieving "an organic solar cell with 4.9% efficiency and 20% transmission," both the hour and the man have arrived.

As iconic older solar energy companies expire, rising star is Dresden-based OPV Heliatek GmbH in whom both BASF Venture Capital and Robert Bosch are investing φ.6m.

Low temperature (< 400°C) technology, cost-saving materials, a solar cell thinner than 500 nanometers, using carbonate dyes promises to yield light-weight, thin, rollable, plastic foil active cells, weighing 500 g/m2.

Keeping nextgen PV competitive, Switzerland's EMPA labs led by Ayodhya Tiwari has gathered up 12 university, research, and industrial organisations in the more modestly φom funded SCALENANO project. The aim is to scale-up materials and processes for low-cost, high-efficiency chalcogenides (Cu2ZnSn(S, Se)2-based absorbers, kesterites) using cheap, abundant materials.

It has three years to develop vacuum-free, electro-deposition processes for nanostructured precursors, industry players being Merck KGaA (chemicals), NEXCIS (photovoltaics), IMPT (TFT) and Hungary's Semilab (metrology).

It's going to be an energetic race to that grail of PV efficiencies and longer cell life.

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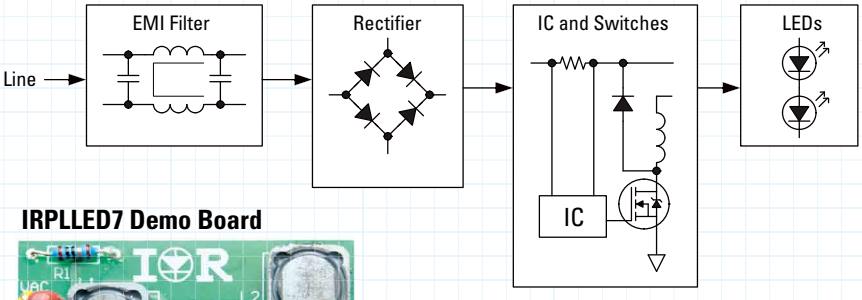
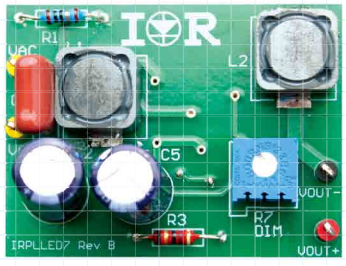
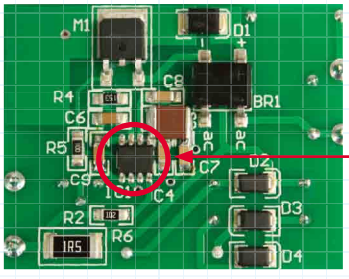


IRPLLED7 Demo Board





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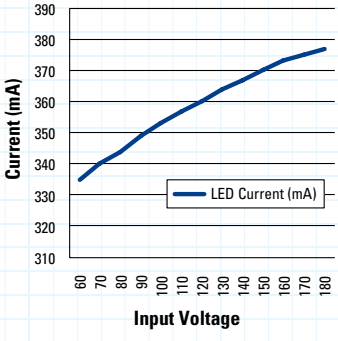
IRPLLED7 Demo Board
LED Current vs Input Voltage



IRS2980 Features

- Internal high voltage regulator
- Hysteretic current control
- High side current sensing
- PWM dimming with analog or PWM control input
- Free running frequency with maximum limiting (150kHz)

IRS2980 Benefits

- Low component count
- Off-line operation
- Very simple design
- Inherent stability
- Inherent short circuit protection

Demo Board Specifications

- Input Voltage 70V to 250V (AC)
- Output Voltage 0V to 50V (DC)
- Regulated Output Current: 350mA
- Power Factor > 0.9
- Low component count
- Dimmable 0 to 100%
- Non-isolated Buck regulator

Part Number	Package	Voltage	Gate Drive Current	Startup Current	Frequency
IRS2980S	SO-8	450V	+180 / -260 mA	<250 µA	<150 kHz
IRS25401S	SO-8	200V	+500 / -700 mA	<500 µA	<500 kHz
IRS25411S	SO-8	600V	+500 / -700 mA	<500 µA	<500 kHz

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