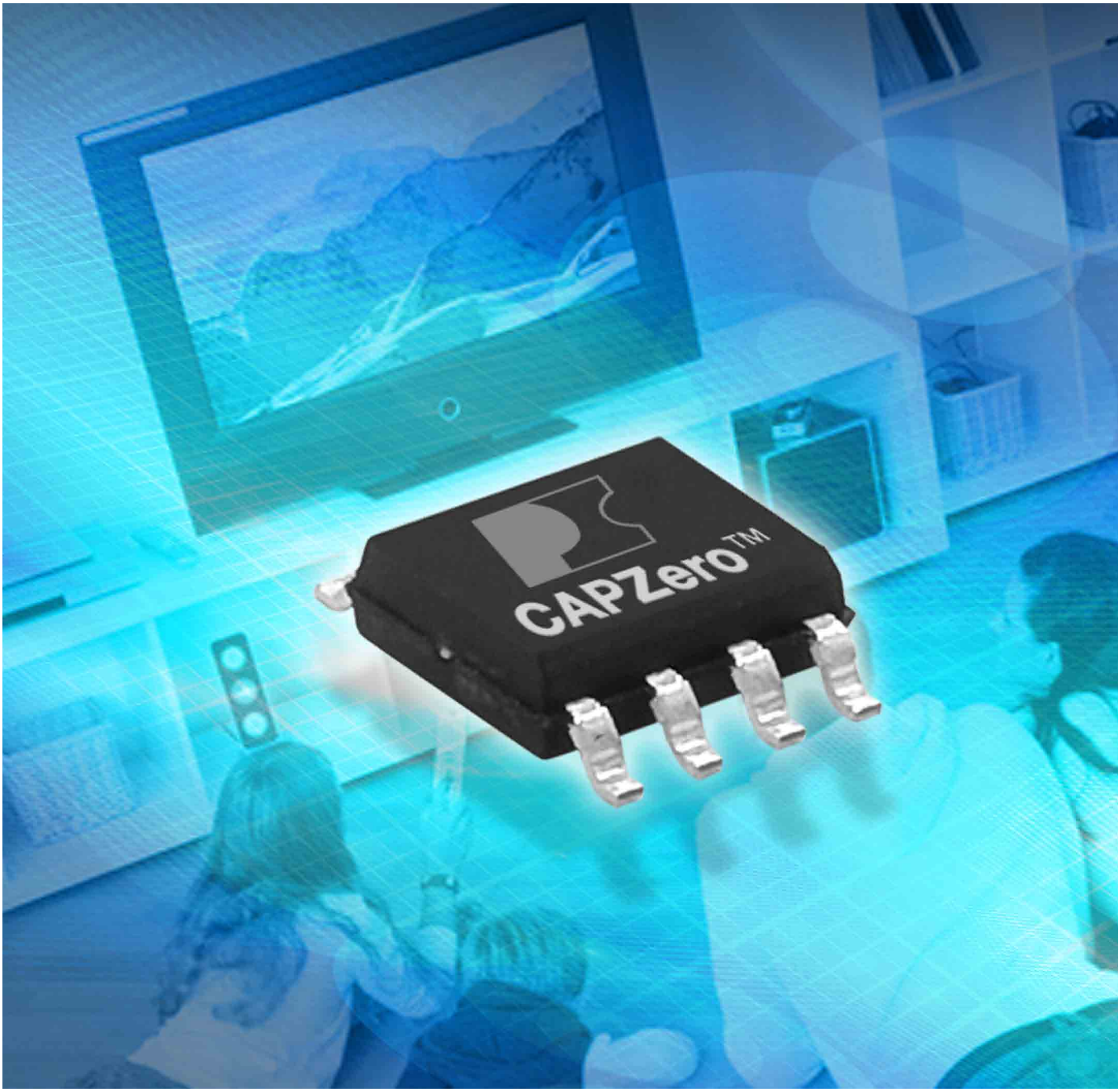
September/October 2012

PSD NORTH AMERICA

Power Systems Design: Empowering Global Innovation

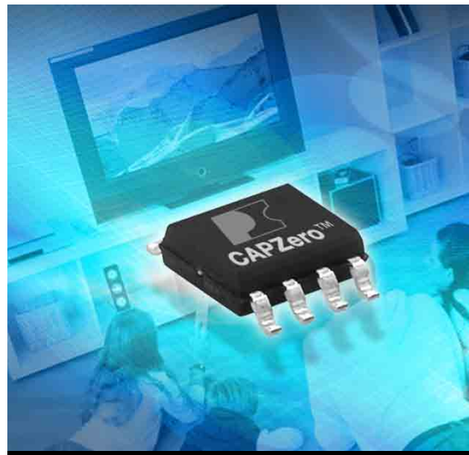


SPECIAL REPORT: GRID POWER (PG39)

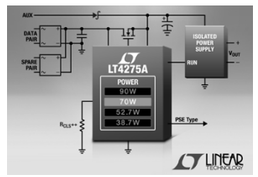
PSD NORTH AMERICA
Power Systems Design: Empowering Global Innovation

WWW.POWERSYSTEMSDESIGN.COM

Visit us online for exclusive content; Industry News, Products, Reviews, and full PSD archives and back issues



COVER STORY
Meeting Safety Standards for A/V and IT (pg 18)



Highlighted Products News, Industry News and more web-only content, to:
www.powersystemsdesign.com

PSSD NORTH AMERICA

AGS Media Group
146 Charles Street
Annapolis, MD 21401 USATel:
+410.295.0177
Fax: +510.217.3608
www.powersystemsdesign.com

Editor-in-Chief
Joshua Israelsohn, Editor-in-Chief,
Power Systems Design
joshua@powersystemsdesign.com

Contributing Editors
Gail Purvis, European Editor,
Power Systems Design
Gail.Purvis@powersystemsdesign.com

Liu Hong, Editor-in-Chief, Power Systems Design China
powersdc@126.com

Ash Sharma, IMS Research
Ash.*sharma@imsresearch.com*

Dr. Ray Ridley, Ridley *Engineering*
RRidley@ridleyengineerng.com

David Morrison, How2Power
david@how2power.com

Publishing Director
Jim Graham
jim.graham@powersystemsdesign.com

Publisher
Julia Stocks
Julia.stocks@powersystemsdesign.com

Circulation Management
Kathryn Philips
Kathryn.phillips@powersystemsdesign.com

Magazine Design
Louis C. Geiger
louis@agencyofrecord.com

Production Manager
Chris Corneal
chris.corneal@powersystemsdesign.com

Registration of copyright: January 2004
ISSN number: 1613-6365

Volume 4, Issue 5

GET SMART

This month's Special-Report focus is on grid power and, in the current era, that topic invariable calls for discussions centered on various smart-grid concepts, many and broad. The section's leadoff article, IEC 61850 increases grid reliability, is an interesting case study from ABB describing how engineers using IEC-61850-compliant gear were able to reduce feed-switchover time for an industrial energy user by 55% and convert a marginally performing system to a reliable one.

Grid security is a topic that piques even the interest of the popular press, albeit all too often in forms more appropriate to television crime dramas than to sober discussions of technologies, public policy, or the intersection of the two. So, I was intrigued by the article, Securing the life cycle in the smart grid from Maxim Integrated Products, which demonstrates how extensive smart-grid security must be to ensure a safe, robust, and reliable electric-energy supply.

Given the variability of operating conditions for grid-connected inverters, the notion of safe, robust, and reliable supply also demands thorough proving of PV inverter designs. Test today your PV inverter for tomorrow from DNV KEMA provides useful insight into the issues and challenges related to such testing.

Of course smart grid doesn't hold a monopoly on smarts or ingenuity in the power sector—a fact amply demonstrated by five other articles in this issue. For example, our cover story, Meeting safety standards for A/V and IT from Power Integrations, introduces a clever way to ensure user safety while meeting stringent standby-power goals. Performance vs power in off-chip DDR SDRAM from Synopsys explains how intelligent memory control can allow applications to set the balance dynamically.

How high-TJ TRIACs benefit your applications from STMicroelectronics and Integrated Current Sensing from On Semiconductor both demonstrate how innovative components can give you additional design flexibility and, in many applications, save energy simultaneously. Finally, Power electronics based on GaN MISHEMPTs from EpiGaN provides an update to developments in GaN on Si processing and a preview of the switching device of tomorrow.

Pretty smart.

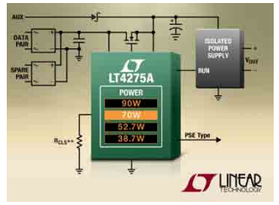
Of course that's just part of what this issue has in store for you, but it's all the room I have for a preview so read on and enjoy!

Joshua Israelsohn

Editor-in-Chief
Power Systems Design
joshua@powersystemsdesign.com

POWER BEYOND PoE+

As standards-based PoE (power over Ethernet) nears its 10th anniversary, several important applications are outstripping both the original 802.3af and 802.3at power levels.



Early applications for PoE, such as enterprise telephony, could be satisfied with 802.3af's 13-W limit for PD (powered-device) input power. As applications for remote data nodes grew, so did power demands, resulting in PoE+, which can deliver 25 W per node as codified by 802.3at in 2009.

In keeping with the old adage, nothing succeeds like success (or is it give 'em a foot and they'll take a yard), applications have again grown with ever more use for ever more power. The 802.3 standards committee, however, has yet to agree on a second extension or the classification method that will allow the PSE (power sourcing equipment) to detect the power levels appropriate for particular PDs.

Alas, the world does not stand still, not even for IEEE standards committees. So product designers seeking to power their circuits through Ethernet data cables are looking to power IC makers with proprietary devices—the market demand that Linear Technology responded to with its LTPoE++ line of devices.

LTPoE++ supports PoE and PoE+ standard power levels and four more that go beyond the standards' limits: 38.7 W, 52.7 W, 70 W, and 90 W. Among applications that benefit from the higher power levels are heated security cameras, picocells, POS (point-of-sale) devices, digital signage, and medical monitoring devices—any network client application that needn't be located near mains-power access.

The new LT4275, for example, is a PD controller compliant with PoE, PoE+, and LTPoE++. Unlike traditional PD controllers that integrate the power MOSFET, the LT4275 controls an external MOSFET to drastically reduce overall PD heat dissipation and maximize power efficiency, especially important at higher power levels. This approach allows product designers to size the MOSFET to their application's specific heating and efficiency requirements.

The LT4275 pairs autonomously with Linear Technology's PSE controllers without reliance on the LLDP (link-layer discovery protocol), which can require extensions to standard Ethernet stacks and represent a significant software development effort. Instead, one external resistor sets the PD controller's classification code to PoE and PoE+ power levels and a second external resistor identifies the LTPoE++ power level to the PSE during startup.

The PD controller tolerates line surges to 100 V, protecting PDs from common line surges. It's available in industrial (-40 to 85 °C) and automotive (-40 to 125 °C) grades and includes on-chip over-temperature protection. The LT4275 is available in 10-lead MSOP and 3 x 3 mm DFN packages with prices starting at $1.45 each in 1000-piece quantities.

www.linear.com

BATTERY-ENERGY STORAGE BOLSTERS RENEWABLES

By: Alexandra Goodson and Joe Fox

Efforts and investments to meet wind- and solar-energy potential continue to accelerate.

As a result, the ability of wind and solar facilities to provide consistent, high-quality power to the grid becomes increasingly important for the reliable operation of large-scale installations. Though advancements in wind turbine technology, for example, have enabled wind facilities to comply with stringent grid code requirements, the intermittent nature of wind continues to be a key challenge for achieving bulk wind penetration.

Through high-tech features and configurable options, BESSs (battery-energy-storage systems) can enhance the performance of wind facilities by providing grid-code compliance and ancillary service capabilities. Specifically, BESSs provide performance characteristics not traditionally seen in wind facilities, including but not limited to power smoothing (capacity firming), grid stability, and regulation. The inherent reactive-power and voltage-control capabilities of the system also provide the wind facility with an additional mechanism for providing regulation, diversifying grid investments, and enhancing reliability.

Key drivers & challenges

The drivers to achieve higher levels of sustainable, clean electrical energy are well known. Load growth forecasts, coupled with energy prices, supply uncertainties, and environmental concerns are forcing nations around the world to rethink their energy mix and develop diverse sources of renewable energy.

To facilitate this drive, governments have implemented policy mechanisms such as tax incentives, feed-in-tariffs, and RPSs (renewable portfolio standards) to accelerate investments in renewable energy technologies. To date, 33 states within the United States have identified targets of up to 20% renewable penetration in the next 10 to 20 years to promote growth further, and supporters continue to make a strong case in the US Congress for a national RPS . There are costs and challenges associated with a 20% wind scenario, but the target is considered achievable, given the current flexibility in the US grid infrastructure.

Key to achieving these targets is the robustness of the electrical grid itself. As the amount of wind generation continues to represent a larger percentage of overall energy mix, the existing flexibility of the grid is inherently stressed, forcing utilities and grid operators to consider critical upgrades and operational considerations, such as curtailment to maintain reliable power.

Energy policies typically require the use of wind energy when available. Coupled with higher

penetration levels, scenarios could exist where levels of fast responding generators, such as gas-fired plants, are exceeded. This results in the operation/reduction of slower responding generation, such as coal-fired plants adversely affecting system efficiency and maintenance intervals per the following: Thermal plants operating at lower capacity factors; thermal plants ramping more frequently; thermal plants operating more sporadically; and lower efficiency, higher fuel consumption, and higher emissions.

In addition, there continues to be recognition that remotely located wind facilities, coupled with variability, create a need to consider carefully voltage control, regulation, and system stability. Grid operators are forced, therefore, to tighten grid connection rules, or grid codes, to limit the effects of wind-power parks on the network quality and stability.

Battery storage

Given the various challenges to bulk renewable integration, BESSs have emerged, allowing renewable generators to perform more like conventional generators. As wind-turbine and solar-farm technologies continue to improve, in many instances employing advanced control and power electronic systems, the value of fast-responding, customizable storage for renewable energies can be derived from the following enhancements:
Capacity firming, smoothing, and ramp-rate control compensates for short-term intermittency from wind and solar. These features also keep renewable production within an acceptable forecasted window and reduce the amount of fossil fuel generation needed to compensate for variable generation.

BESSs also add to grid stability by maintaining power until alternative sources are brought online or dispatchable loads are disconnected. They also avoid power-system collapse when renewables are quickly dispatched from the network.

Electrical-energy storage resources support regulation and grid code compliance with respect to power factor and voltage regulation, power quality, and ancillary services. These enhancements allow wind facilities to overcome grid constraints, offer ancillary services, and stabilize frequency.

Connecting storage to the grid

Smart Grid connected power converters combine bi-directional, four-quadrant power electronic devices, such as IGBTs or IGCTs (integrated gate commutated thyristors), with an advanced control-and-monitoring platform. When combined with an energy source, such as batteries, flywheels, or ultra capacitors, power converters can dynamically control active and reactive power to facilitate a number of grid functions, including, but not limited to voltage control, frequency regulation, capacity firming, ramp-rate control, dynamic power control, generator emulation, and islanding.

Specifically, the dynamic power-control capability of the PCS (power-converter system) is customizable to the grid application, including voltage and frequency control set points, prioritization of Q over P for VRT (voltage ride-through) grid support, and market-based control signals. The PCS's advanced control and monitoring systems allow for communication and integration into local EMSs (Energy Management Systems), site control systems, and network-level SCADA systems, further permitting a wind or solar facility to mimic the capabilities of conventional generators.

Renewable energy penetration is only going to increase—that much is inevitable. Without a means to overcome known challenges, however, customers won't gain the benefits, and utilities won't see the full return on their investment. Fortunately, BESSs, along with smart-grid converters, will play a major role in the emerging smart-grid-modernization movement.

Alexandra Goodson
Business Development Manager
Energy Storage Modules, ABB

Joe Fox
Sales Application Engineer, ABB

www.abb.us

DO RECENT WEATHER EVENTS IN NORTH AMERICA HELP THE SMART-GRID MOVEMENT?

By: Michael Markides

In late June 2012, a severe storm hit parts of the eastern US, leaving residents and businesses without power for upwards of one week (http://yhoo.it/RjpxAn).

Over the past several years in North America, these events seem to have become more common, or at least more visible, often leading to intense criticism directed towards the electric utilities responsible for taking too long to restore power. This latest outage left some residents without electricity during a record-breaking heat wave, with temperatures reaching above 100 °F.

Overhead power lines present a significant liability in North America, as a large violent storm can take out lines across a large service area. This leaves behind a mess for the operating utility, who must locate all downed lines and restore power, often requiring manpower beyond what may be regularly on hand. Utilities and residents alike acknowledge that downed lines are inevitable; however, growing anger from residents is rooted in the excessive time needed to restore power, particularly during harsh weather.

New regulations, along with increased understanding and deployment of new technology are being implemented to cut downtime. IMS Research has recently published an update to its annual market study on the distribution automation market, highlighting utility investment in new technology on the medium voltage layer of the electric grid. IMS Research forecasts more of the available utility funds will be shifted towards investment on distribution automation equipment and related platforms, with a critical portion going towards FDIR (fault detection, isolation, and restoration) schemes. Automated switches, smart reclosers, retrofit switch-control modules, and communicating fault detectors are all forecast to see increased sales globally, with the highest market volumes seen in North America.

Michael Markides, Associate Director
Metering & Energy Management Group
IHS

www.ihs.com

INPUT IMPEDANCE MEASUREMENTS

By: Dr. Ray Ridley

In this third part of this series of articles, Dr. Ridley discusses the fourth important frequency-response measurement made during full characterization of a switching power supply. The closed-loop input impedance is measured to be a negative resistance at low frequencies. The input impedance of a power supply is also complicated by the inclusion of input filter parameters in most practical measurements that are made.

Power Supply Transfer Function Measurements

There are four fundamental transfer functions that characterize the small-signal performance of a switching power supply. They are as follows:

1. Loop gain and phase – determines the stability of your design, and available margin to accommodate variations in components.
2. Output impedance – determines the output regulation, dynamic load response, and susceptibility to complex loading.
3. Audiosusceptibility – determines the transmission of noise from input to output.
4. Input impedance – determines the sensitivity of the power system to input filter or input power system components.

The first three parameters, loop gain, output impedance, and audiosusceptibility were discussed in the first two articles of this series. It is highly recommended that all three of these measurements are made on every switching power supply that you design and build. The loop measurement is essential to guarantee stability over the lifetime of the power supply, and the output impedance gives comprehensive information about the performance in the presence of load variations. The audiosusceptibility is measured is very useful for showing the rejection of noise from input source to output.

An input impedance measurement gives information about the characteristics of the power supply input terminals. It is usually a requirement of the documentation package in the aerospace industry. As with the audiosusceptibility measurement, a signal must be injected on top of the high-power input rail. Once you have set up your test equipment to do audiosusceptibility measurements, input impedance measurements are straightforward to do.

Input Impedance Measurements

The input impedance measurement can predict how well the power supply will integrate into a system. If the input impedance is too low, it can load down the source and provide adverse system interactions. In order to measure input impedance, a voltage source must be injected in series with the input of the power supply as shown in Figure 1.

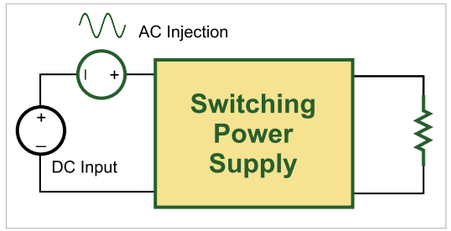


Figure 1: Input impedance is measured by adding a voltage signal at the input terminals of a power supply and measuring input voltage and input current perturbations.

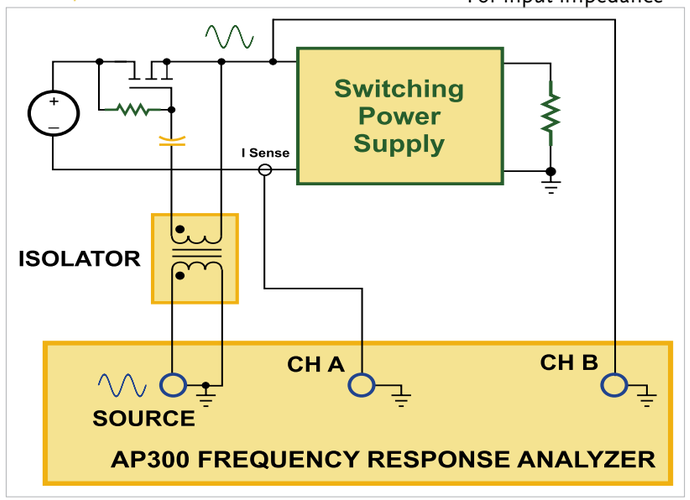


Figure 2: Practical test setup for injecting voltage signal and measuring input impedance.

Figure 2 shows how this is implemented practically using a frequency response analyzer and a few discrete devices. The output of the analyzer is connected to wide-bandwidth isolator which is then AC coupled to a FET hooked up as a voltage follower. The size and rating of the FET may vary according to the power level and voltage level of the converter that is being driven. This injection technique is much simpler and more cost effective than inserting a high-power amplifier in series with the input source, and will allow sufficient signal to be injected for most applications.

The only difference between this setup and the setup for audio-susceptibility is that the signals sent to the analyzer are different. For input impedance measurements, Channel B of the analyzer measures the input voltage perturbation, and Channel A measures the input current perturbation. The current is measured with some kind of transducer – either a small sense resistor, current transformer, or active probe. Dr. Middlebrook, in his famous paper on input filter interactions, specified that the input impedance of a converter should be analyzed and measured at the switching cell input. This is the point at which the interaction analysis can be properly applied to predict whether the input filter will affect the control loop. However, in most practical situations, the input impedance measurement includes some or all of the input filter components in parallel with the input impedance of the power supply. This can lead to false low measurements that are not relevant to Middlebrook's original discussions. More information on this topic can be found in [3].

Before closing the control loop on a converter, it is useful to measure the open loop input impedance of the power supply. The results of this measurement are shown in Figure 4. There are four asymptotes to gain curve of this figure. The first, A, is proportional to the load resistance of the converter. Notice that the phase of the impedance at this point is zero degrees, denoting a positive value of resistance.

Just before 100 Hz, the

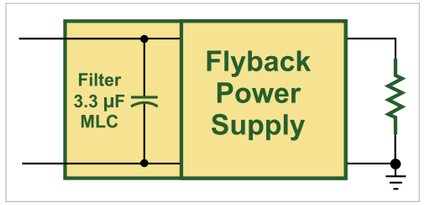


Figure 3: Flyback converter with input filter capacitor. In most cases, practical measurements require some input filter components to be included in the impedance measurement.

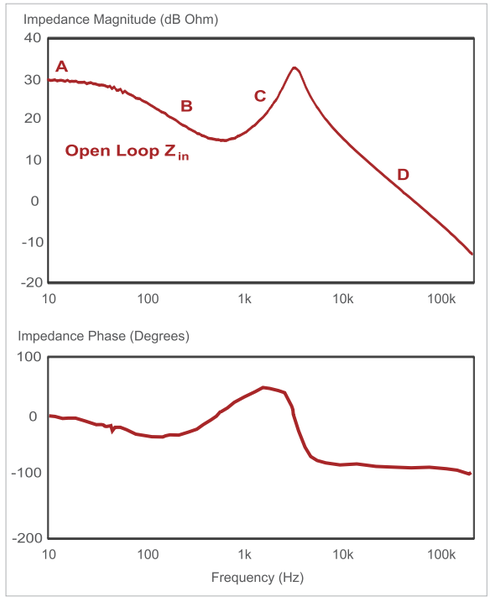


Figure 4: Open-loop input impedance measurement of a flyback converter.

asymptote B is due to the output capacitance of the power supply, and the input impedance starts to drop. This continues until to the resonant frequency of the LC filter of the power supply, and then the impedance climbs along asymptote C, according the value of the flyback inductance.

Eventually the impedance of the input filter capacitor becomes lower than the impedance of the inductor, so the final impedance follows the asymptote D. Notice that the final value of the phase of the input impedance is -90 degrees, corresponding to a capacitive value.

The open-loop input impedance is quite a complex curve, even with just a single capacitor as the input filter. With more complicated input filters included in the measurement, the complexity of the measured or predicted impedance will increase.

Figure 5 shows the input impedance of the same converter with the control loop closed.

The green curve of Fig. 5 shows the closed-loop input impedance of the converter. At low frequencies, along asymptote A, the dc value is determined by the power output of the converter and the input voltage. You can see from the green phase curve that the impedance now has a starting phase of -180 degrees, denoting a negative resistance. This is the classic characteristic of all constant-power switching power supplies, and it is at the heart of the stability problem that can arise when coupling switching power supplies with input filters.

This closed-loop input impedance stays relatively constant until the impedance of the input filter capacitor becomes lower than the starting negative resistance. The impedance then follows the asymptote B, with a 90 degree phase delay, as observed for the open-loop characteristic.

Notice that there is not the same simple relationship between the open-loop and closed-loop input impedance and loop gain that exists for the audiosusceptibility and output impedance. For these two quantities, the open-loop characteristic was attenuated by 1+T(s). Input impedance is different. When there is significant loop gain, the input impedance is transformed into a fixed-value negative resistance. Without any input filter components, the input impedance rises with frequency after the crossover frequency. However, as can be seen in this example, the input impedance is heavily influenced by the present of the input filter capacitor.

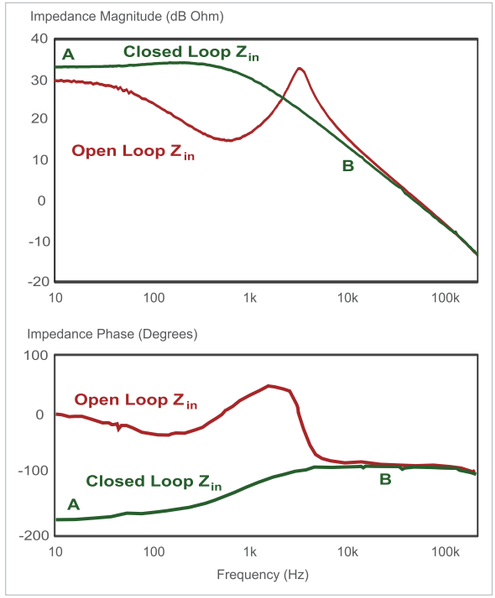


Figure 5: Closed-loop and open-loop input impedance measurements of a flyback converter.

Summary

This article discusses the significance of power supply input impedance, and shows how it can be practically measured. Most aerospace designs require a power supply input impedance measurement in order to properly assess the impact of integration of power supplies into larger systems. In most cases, input impedance measurements include the impedance of the input filter, and this complicates the proper application of Middlebrook's impedance interaction criteria. [3].

References

1. Ridley Engineering Frequency Response Analyzer from AP Instruments, www.ridleyengineering.com/index.php/analyzer.html
2. Ridley Engineering Design Center, www.ridleyengineering.com/index.php/design-center.html
3. "Power Supply Design. Volume 1: Control", by Dr. Raymond B. Ridley. Full-color textbook available at http://www.ridleyengineering.com/index.php/books.html.

Dr. Ray Ridley
President
Ridley Engineering

www.ridleyengineering.com

MEETING SAFETY STANDARDS FOR A/V AND IT

Capacitor-discharge ICs provide IEC-62368 safety-standard compliance without sacrificing standby power

By: Edward Ong

The convergence of consumer and information technologies has stimulated the development of new safety standards and a new approach to ensuring the safety of electronic systems.

New components, safe-by-design, allow the system developer to address these new challenges. It is no exaggeration to state that electronics technology has undergone a revolution in recent years, resulting in products such as the smart phone. Smart phones represent the ultimate convergence of computer, communication, and consumer technologies into a single hand-held device. A similar convergence with mains-powered equipment is right around the corner: smart TVs with Ethernet connections are already capable of browsing networks and provide a gateway to streaming media services. TVs with more powerful processors become capable of delivering an internet-browsing experience similar to that of PCs. At the same time, consumers frequently use PCs now to listen to music and watch video clips, streamed TV shows, and movies.

These developments are being echoed by changes in the evolution of safety standards. Not so long ago the IEC (International Electrotechnical Commission) hosted several technical committees, individually covering Audio/Video, Information, and Communications Technology equipment, and each producing its own safety standards. As the technologies and applications continued to merge, it became clear that the duplication should stop and the different specifications should combine into one common standard. The first sectors to combine were Office Equipment (IEC 380) and Data Processing Equipment (IEC 435). This merger gave rise to the Technical Committee TC74 and the creation of IEC 60950 covering Information-Technology Equipment.

On the consumer side, Technical Committee TC92, covering Audio, Video, and Similar Apparatus, had meanwhile developed IEC 60065, which was significantly different from IEC 60950. Combining computer and consumer sectors into a new single standard was to be much more than a merging of specifications. The new standard, IEC 62368-1, produced by Technical Committee TC 108, was based on a new principle—HBSE (hazard-based safety engineering)—covering Audio/Video, Information and Communication Technology Equipment (References 1 and 2).

Hazard-based safety engineering

Hewlett-Packard first formalized the principles of HBSE, which ECMA, Europe's prominent computer-industry association, subsequently introduced in an industry standard. Following HBSE, the developer first identifies potentially hazardous energy sources then analyzes the mechanisms by which energy could transfer to the user. Finally, the developer must either reduce the potentially hazardous energy level to a non-injurious magnitude, or prevent the transfer mechanism from operating. This results in a product that remains safe under multiple fault conditions.

Engineers can always design products to provide a physical barrier between the user and AC mains supply voltages with the exception of the AC mains plug. While the appliance may seem harmless when unplugged because there are no high voltages present, the fact is, due to the energy stored in the input filter, it is still possible to get a shock.

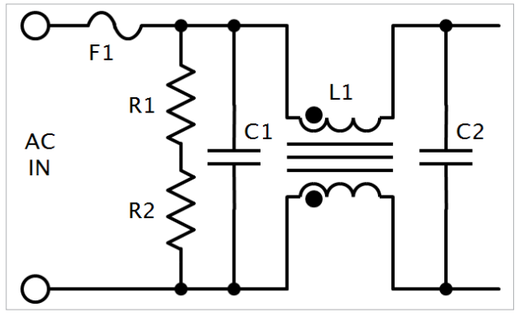


Figure 1: Example EMI filter stage of a switching power converter using a choke, two class-X capacitors (C1, C2) and discharge resistors (R1, R2).

Products that operate with off-line switching power electronics—now ubiquitous in computer and consumer-electronics equipment—have high-voltage and high-current switching waveforms that generate EMI. To reduce EMI, power-supply designs include a filter stage at the AC input (Figure 1).

As part of this filter, capacitors commonly connect directly across the AC input terminals to reduce differential mode EMI. As the capacitance appears across the input terminals, a voltage, up to the peak of the incoming AC, can appear across the pins of the AC plug. This could potentially cause an electric shock to the user if touched. To prevent this risk, safety agencies mandate that capacitance values above 100 nF discharge automatically with a time constant < 1 s when the appliance is unplugged. Typically, designs meet this requirement by placing discharge resistors directly across the capacitor. Two resistors usually connect in series to meet safety agency single-point-of-failure testing. Should one resistor short, then the presence of the second prevents a short circuit across the AC input.

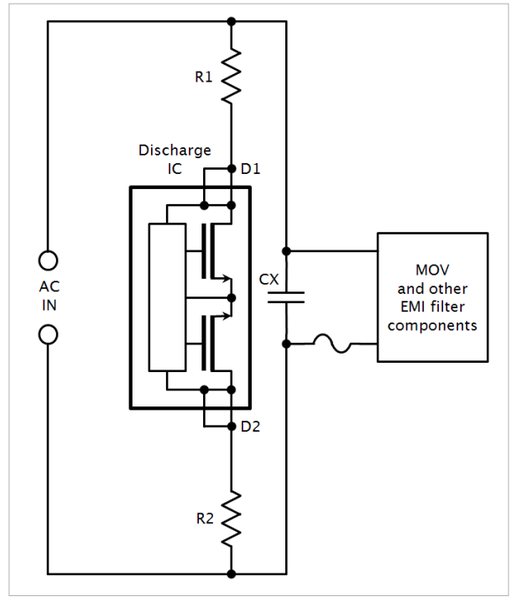


Figure 2: Capacitor-discharge ICs like CAPZero devices connect across a class-X capacitor. A loss-of-AC detector turns the back-to-back MOSFETs on when mains power is removed.

Power loss

Unfortunately, the presence of discharge resistors results in a constant power loss while AC is applied. With the stringent no-load and standby input-power requirements demanded by ENERGY STAR and EuP (energy-using-products directive) Directive Lot 6, for example, this power loss represents an unacceptable portion of

the overall power budget. For instance, a power supply that uses a capacitance of 1 µF across the incoming AC will require a maximum discharge resistance value of 1 MΩ which dissipates 53 mW at 230 VAC independent of the output load. Designs can eliminate this power loss by including an automatic capacitor-discharge IC such as those from Power Integrations' CAPZero family (Reference 3). Capacitor-discharge ICs like CAPZero devices integrate a loss-of-AC detector with back-to-back MOSFETs (Figure 2).

When the AC input voltage is present, the discharge IC remains in an off state, blocking current flow in the discharge path and eliminating power loss. When the AC disconnects, the device automatically turns on, connecting the resistors and discharging the input filter capacitance. The discharge IC is self-powered from the AC line with a power consumption of less than 5 mW at 230 VAC.

As the capacitor-discharge device is typically placed at the AC mains input of an appliance, it is a key contributor to compliance for equipment under the scrutiny of IEC 62368-1's approach to HBSE. In particular, no single point of failure can result in a user exposure to a hazard. The practical result of this is that the IC must continue to provide the full protection function with any single pin either open or shorted.

Class	Differential Mode Surge	Common Mode Surge	Comments
	Z_{OUT} = 2Ω	Z_{OUT} = 12Ω	
1	No requirement	0.5 kV	Protected environment
2	0.5 kV	1 kV	Electrical environment where cables are well separated
3	1 kV	2 kV	Electrical environment where cables (power and electronic) run in parallel (residential environment)
4	2 kV	4 kV	Electrical environment where cables (power and electronic) run in parallel (industrial environment)
5	> 2 kV	> 4 kV	Severe surge environment (rural/sparsely populated areas)

Table 1: Surge-voltage levels (per IEC 61000-4-5).

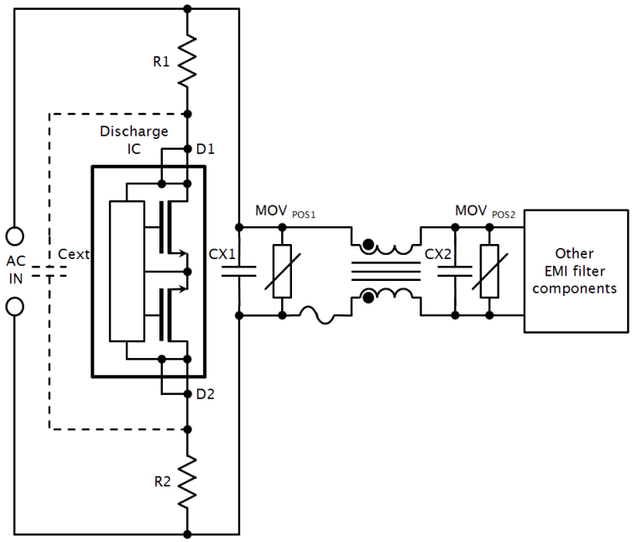


Figure 3: The use of MOVs and an external capacitor across the CAPZero device reduces voltage stress during a surge event.

The CAPZero IC's package and pinout design ensures compliance with this requirement for single-point-of-failure testing.

There are two dedicated pins for the D1 and D2 terminals, which add redundancy during single-point-of-failure testing (pin-short / pin-open testing). If one pin disconnects from the device or PCB, the IC will continue to function normally. During pin shorting, the outcome is the same as if the device had not been used and simply results in the discharge resistors being connected in series continuously—a safe condition.

Surge severity

Another factor in HBSE is the ruggedness of the equipment to withstand damaging electrical surges. The IEC 61000-4-5 standard defines the severity of surge signals. Table 1 describes the surge-voltage levels, which depend on the power supply's operating environment.

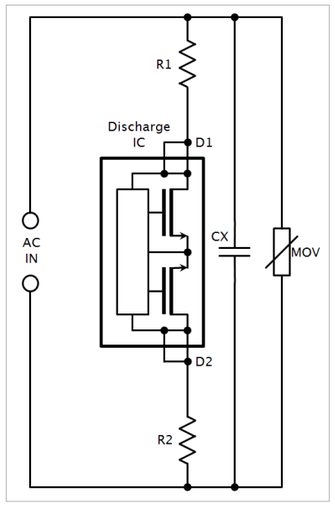


Figure 4a

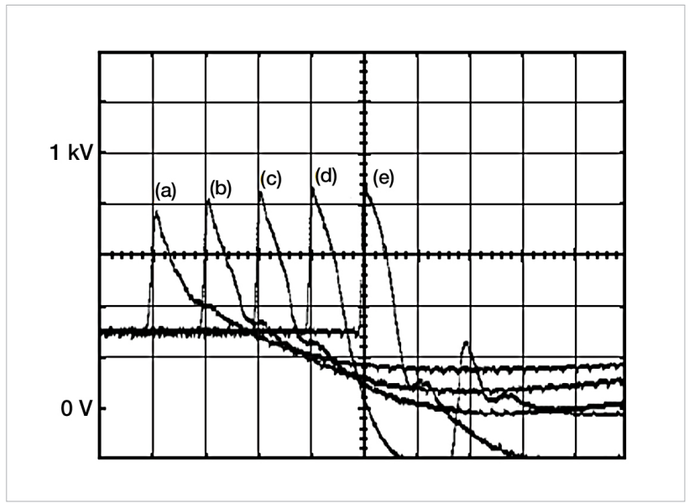


Figure 4b

Figure 4: Recommended position of CAPZero IC for a single stage EMI Filter (a). Waveforms show peak voltage across a CAPZero capacitor-discharge IC in the presence of an MOV (b).

The capacitor-discharge IC is one element of the power supply's AC-input design. Other components and the board layout influence the surge performance. Figure 3 indicates possible options for the placement of MOVs (metal oxide varistors) and capacitors to provide the required level of surge tolerance (Reference 4).

Figure 4 shows the test circuit and results for surge testing of a typical CAPZero application.

The waveform scales are 200 V/div, vertical and 50 µs/div, horizontal. Peaks (a) Through (e) represent the voltage measured across a CAPZero capacitor-discharge IC with differential-mode input-surge voltages of 1, 1.5, 2, 2.5, and 3 kV, respectively. The MOV in this test was a 14-mm 275-VAC device. Exhaustive testing has been undertaken using many different power supply configurations at voltages up to 6 kV, far beyond the requirements of current and envisaged standards.

Working to the new standard

IEC 62368-1 provides greater flexibility in deploying new technologies, but it also places new demands and a new discipline on the design engineer. The example of capacitor-discharge ICs illustrates that compliance with IEC 62368-1 does not necessarily involve extra cost or compromise. The device provides the means to reduce power consumption in the input filter of a power supply while its safety features inherently support compliance to IEC 62368-1, both in new designs or as a retrofit to existing products.

Edward Ong
Senior Product Marketing Manager
Power Integrations

www.powerint.com

References:

1. IEC 62368-1 Technical Brief. Underwriters Laboratories Inc, 2010.
2. The ABCs of IEC 62368-1, An Emerging Safety Standard. Tom Burke. 2010.
3. CAPZero Family Zero Loss Automatic X Capacitor Discharge IC. Power Integrations Inc. November 2011.
4. Application Note AN-48 CAPZero Family Design Considerations. Power Integrations Inc. December 2011.

PERFORMANCE vs POWER IN OFF-CHIP DDR SDRAM

Memory-system management reduces dissipation while meeting application-performance demands

By: Graham Allan

To deliver new features and higher performance in consumer-electronic products, SoC developers constantly look to integrate more functionality into their designs.

SoCs with more features and performance typically operate with higher clock frequencies, which require faster access and greater bandwidth to memory. DDR (double-data-rate) SDRAM, the most cost-effective off-chip memory, is the memory of choice to meet the increasing bandwidth needs of today's SoCs.

DDR-SDRAM subsystems offer cost and performance benefits, but higher performance usually translates to increased power consumption. Whether the design is for mobile or wired applications, it is critical that designers optimize their DDR-SDRAM subsystems to manage power consumption while maximizing system performance. Designers can build a complete DDR subsystem that balances power and performance requirements by drawing on their application knowledge and taking advantage of available DDR SDRAM power-management features.

Issues for mobile products

Power management is a primary concern in mobile-product designs because battery capacity limits the product's available source energy. The less power the product consumes, the longer it can operate before the user must recharge the battery. Even though battery technology is dramatically improving, the desire to support multi-tasking applications increases the power requirement. Multi-tasking applications demand higher bandwidth from the DDR-SDRAM subsystem, which often translates to a faster clock rate that requires more power.

Mobile products do not operate constantly, so power management targets two areas: active power (power consumed while the product is in use) and standby power (power consumed while the product is on but inactive). Because of the sensitivity to both active and standby power, mobile products typically use low-power SDRAM such as LPDDR2 (low-power DDR2) or LPDDR3 (low-power DDR3). Low-power DDR SDRAM consumes less power in active mode. For example, the low-power variants forgo the common parallel termination mainstream DDR2 and DDR3 devices use. They also reduce power in standby mode by, for example, forgoing the on-chip DLL (delay-locked loop) that standard DDR memory includes.

In contrast to LPDDR3 SDRAM, mainstream DDR3L memory consumes slightly more power for the same operating frequency in active mode but approximately nine times more power in standby mode (Figures 1 and 2).

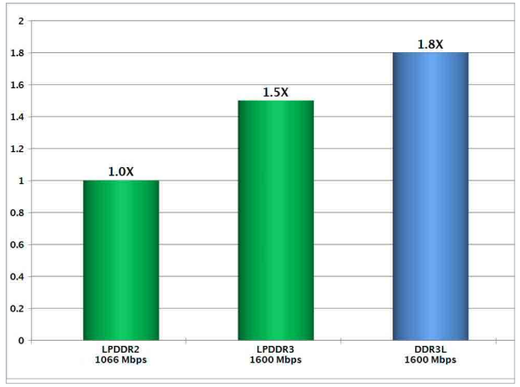


Figure 1: Relative active power

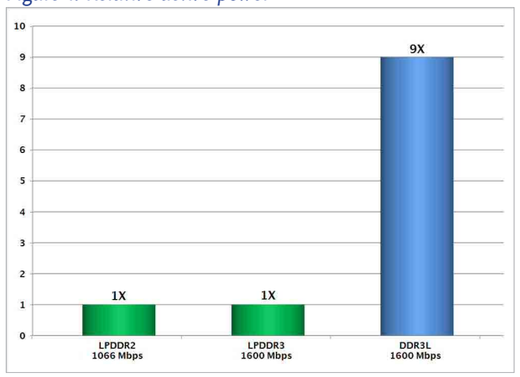


Figure 2: Relative standby power

Between LPDDR2 and LPDDR3, several features support the low-power requirements of mobile products including low I/O supply voltage, PASR (partial array self-refresh), and deep power down. Mobile SoC developers leverage these and other LPDDR SDRAM features to minimize power in the SDRAM interface.

Low I/O supply voltage: Switching power in CMOS chips is directly proportional to CV2f where C is the capacitance of the switching node, V is the voltage swing, and f is the operating frequency. Due to its square-law relationship to power dissipation, reducing the voltage swing has the greatest potential to reduce power consumption. As a result, LPDDR2 and LPDDR3 SDRAMs offer a low I/O supply voltage of 1.2 V as compared to DDR3 SDRAM's 1.5 V or DDR3L SDRAM's 1.35 V.

PASR: Because their data is stored on small capacitors, SDRAMs require periodic refresh operations to maintain their data integrity. Self-refresh is a mode that puts the SDRAM into a low-power state and the device manages its own refresh requirements to maintain data integrity without intervention from the memory controller. SDRAMs that support PASR allow the system to determine if it needs to maintain all of data stored in the SDRAM or if only a portion of the entire SDRAM needs to be refreshed. Since any refresh operation consumes power, excluding parts of the SDRAM from self-refresh saves overall system power. Both LPDDR and LPDDR2 SDRAM support PASR.

Deep power down: Mobile products can also take advantage of the deep-power-down command in low-power SDRAMs. Designers use deep power down when the SDRAM does not need to retain its contents and when the system can handle a longer than normal activation cycle. In deep power down mode, the LPDDR SDRAM can disconnect all internal power from within the memory and will consume the least amount of power as compared to all other modes.

Issues for wired products

Power management is also an issue for wired systems including HD TVs, set-top boxes, computers, and other products that draw power from a wall outlet. Power consumption affects wired consumer products on two fronts: cost and conformance to national or international regulations.

To be competitive, consumer products need to be available at the lowest possible cost. Systems that consume more power often require advanced packaging to dissipate the heat chips generate and may require cooling elements such as heatsinks or fans, increasing total cost. LPDDR SDRAM is not a good option for non-mobile consumer devices because it is more expensive compared to mainstream DDR SDRAM and it typically cannot support the performance requirements those products impose. Therefore, wired devices usually use mainstream DDR SDRAM such as DDR3.

Frequency (MHz)	Power Reduction (%)
1600	0
1066	33%
800	50%
400	75%
200	88%
100	94%
50	97%

Table 1: Frequency reduction and potential active power savings

DDR3 SDRAM does not support as many power saving modes as LPDDR SDRAM because the target use model typically has not been as sensitive to power as mobile devices. In addition, DDR3 SDRAMs are often in systems with 8 to 16 SDRAMs requiring features such as on-chip DLLs and ODT (on-die termination) to accommodate the large number of SDRAMs driven by one controller. DDR3 SDRAM supports both active power-down and precharge power-down modes. The SDRAM disables its on-chip DLL during precharge power-down and consumes less power than in active power-down, which doesn't disable the DLL.

DDR power options

Although DDR SDRAM's power features can help reduce memory-subsystem dissipation, the realized energy savings typically are not sufficient to be competitive. To improve power management of a DDR subsystem further, SoC and system designers can leverage their knowledge of how their system accesses the DDR SDRAM.

Designers can apply active and standby power-management techniques to DDR SDRAM subsystems. These techniques can apply to both mobile and wired applications.

Active power management: To determine the best active power-management structure for a DDR subsystem, recall the switching power determined by the CV2f relationship. The capacitance is usually fixed so designers focus on how to manage the voltage, which has a squared contribution, and the frequency, which contributes linearly.

The largest consumer of active power is the I/O interface, which drives commands and data off-chip during write operations, and receives data during read operations. Designers can reduce power consumption by using DDR3L instead of DDR3, which will cut the voltage from 1.5 V to 1.35 V, saving nearly 20% of the memory device's power .

In addition to I/O voltage reduction, system designs can reduce active power by scaling the operating frequency. Part of the drive for more performance is that consumers are demanding more capabilities in electronic products. Not all of these applications operate all the time, nor do they often operate simultaneously. Additionally, not all of the applications require the same amount of bandwidth from the SDRAM. Conceptually, designs can add intelligence to a DDR SDRAM subsystem that will manipulate the operating frequency depending on the running applications' bandwidth requirements. Through frequency scaling, a DDR SDRAM subsystem can consume less power (Table 1). Systems can implement frequency scaling in either low-power or mainstream DDR SDRAM but it is favored in low-power SDRAM due to its lack of an on-die DLL.

Standby power management: When a modern consumer product connects to its energy source, it is always consuming some power. Even if an SoC stops reading and writing data to SDRAM, it still consumes power, albeit at a lower rate. Reducing this standby power is the second type of power reduction and requires other system power-management techniques.

One technique removes the power from your chip or SDRAM interface by disconnecting the source. When power removal is a practical option, the system must be capable of controlled and

rapid power switching. In addition, the system must be able to pick up where it left off so as not to consume unnecessary time cycling through an entire power up sequence.

Features for power reduction: Certain power-reduction techniques depend on feature support in the DDR controller and PHY (physical layer). SoC designers must understand the bandwidth demands each of the IC's applications impose, and then leverage these techniques to architect a lower-power system.

For example, in frequency scaling, the DDR controller and PHY must be able to communicate with each other to manage the frequency transitions. Likewise, when enabling system power shut down, the controller and PHY provide the appropriate handshakes to ensure the complete DDR SDRAM interface operates appropriately throughout the different modes. Therefore, not only must the DDR controller and PHY support these modes, but their implementations must be mutually compatible. This typically occurs only when the complete DDR interface IP comes from a single supplier and the memory controller can interoperate with the PHY to optimize performance and power conservation.

A complete, integrated DDR subsystem can support other power-management techniques as well. For example, a tightly integrated DDR controller and PHY can leverage the controller's look-ahead capability to manage the PHY's power intelligently by enabling and disabling certain PHY functions and capabilities at appropriate times.

Graham Allan
Senior DDR IP Product Marketing Manager

www.synopsys.com

HOW HIGH-TJ TRIACS BENEFIT YOUR APPLICATIONS

Designers gain flexibility exploiting the benefits of high-temperature power devices

By: Laurent Gonthier and Martial Boulin

High-temperature TRIACs present several benefits particularly useful in applications demanding high current density or imposing high-temperature environments.

These applications include vacuum cleaners, electric ranges, water heaters, air blowers, and small home appliances such as blenders, rice cookers, and bread makers.

High-temperature TRIACs—those that are able to work up to a TJ (junction temperature) of 150 °C—help designers design more efficient control boards by offering enhanced features compared to standard TRIACs.

The benefits of these high-temperature devices are evident in four cases: Applications working at elevated ambient temperatures, those without enough space for a full-size heatsink, cost-sensitive

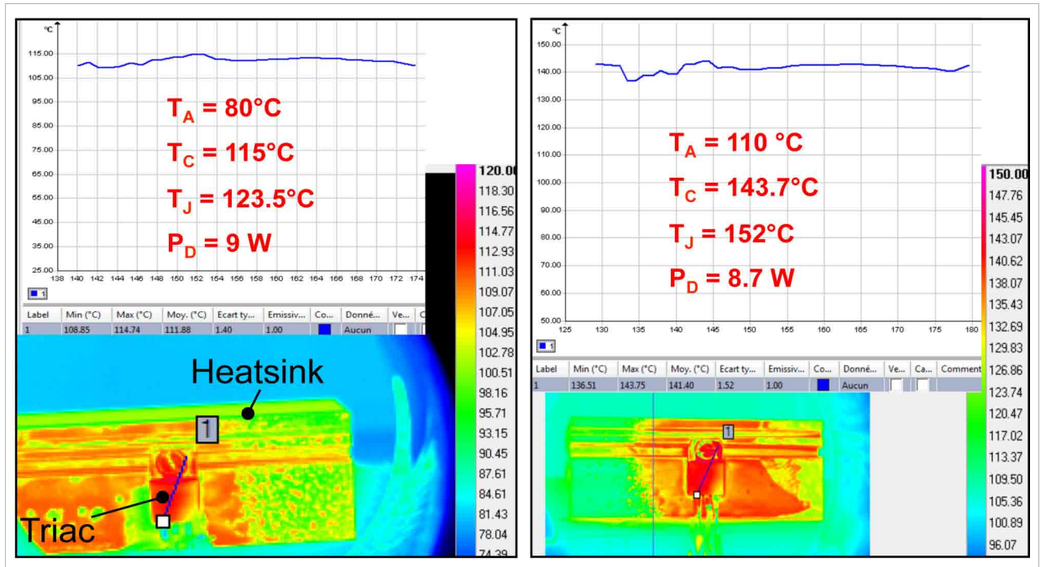


Figure 1: Two TRIACs operating near their Tj(max): The BTB16-600CW standard TRIAC (a) and the T1635H-6T high-temperature TRIAC (b).

applications that use lower-current-rated TRIACs, and applications controlling a higher load current without upgrading the device rating.

Higher-TA operation

To validate experimentally that a TRIAC can operate at a higher TA (ambient temperature), STMicroelectronics engineers mounted two different TRIACs on 3.7 °C/W heatsinks. A test circuit ensured that each device dissipated the same power by applying 10-A RMS currents to both.

The engineers calculated the TA necessary to operate each TRIAC near its own maximum TJ (junction temperature): 125 °C for a BTB16-600CW sample and 150 °C for a T1635H-6T high-temperature TRIAC. Figures 1a and 1b show the temperature measurements as reported by an IR camera during the tests. They set the TA, confirmed by thermocouple measurement, at the calculated values: 80 °C for the standard TRIAC and 110 °C for the high-TJ TRIAC.

The measured values of TC (case temperature) confirmed the calculated TJ using the formula:

$$T_J = T_C + P_D Rth(J-C)$$

where P_D is the dissipated power

$$P_D = \frac{2\sqrt{2}V_t I_{RMS}}{\pi} + R_D I_{RMS}^2$$

and V_t is the TRIAC's on-state forward voltage.

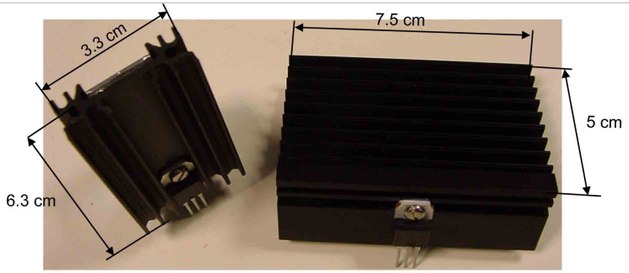


Figure 2: The heatsink-size reduction, when switching from standard to a high-temperature TRIAC, can approach 4:1.

The BTB TRIAC junction temperature was, then, TJ = 115 + 0.95 x 9 = 123.5 °C, and the T1635H junction temperature was TJ = 143.7 + 0.95 x 8.7 = 152 °C. These tests results demonstrate that the high-TJ TRIAC is able to withstand 30 °C higher TA than the standard TRIAC.

Alternatively, with these two TRIACs in the same ambient environment at 80 °C, the high-TJ TRIAC has a temperature margin of 30 °C with respect to its 150 °C maximum TJ while the standard TRIAC is already reaching is maximum TJ. This temperature margin has a direct positive effect on device reliability.

Heatsink size

The next test placed both previous TRIACs into an ambient temperature of 80°C with the high-TJ TRIAC on a 7 °C/W heatsink and the standard device on a 3.7 °C/W heatsink (Figure 2). With both devices conducting the same 10-A RMS current, TC measured 115 °C and 132 °C for the BTB16-600CW and the T1635H-6T, respectively. Using previous formula, the BTB TRIAC TJ = 115 + 0.95 x 9 = 123.5 °C and the T1635H TJ = 132 + 0.95 x 9.4 = 141 °C. Junction temperatures were below the maximum allowed temperatures for each device, but the temperature margin was better for the T1635H-6T device despite its smaller heatsink.

Designers facing size constraints can take advantage of the heatsink-size reduction achievable with a high-TJ TRIAC. The heatsinks these tests used show a thermal resistance increase by a factor of 1.8, implying a heatsink-size reduction of around 4:1, which reduces costs as well.

TRIAC current rating

High-TJ TRIACs are able to drive loads at higher junction temperatures without parameter derating, so they can allow designers to specify lower current rated TRIACs in place of standard TRIACs.

For example, the STMicroelectronics engineers performed tests to evaluate a 12-A high-TJ TRIAC (T1235H-6T) replacing a 16-A standard TRIAC (BTB16-600CW). They mounted both devices on 3.7 °C/W heatsinks and applied the same 10-A RMS load to both.

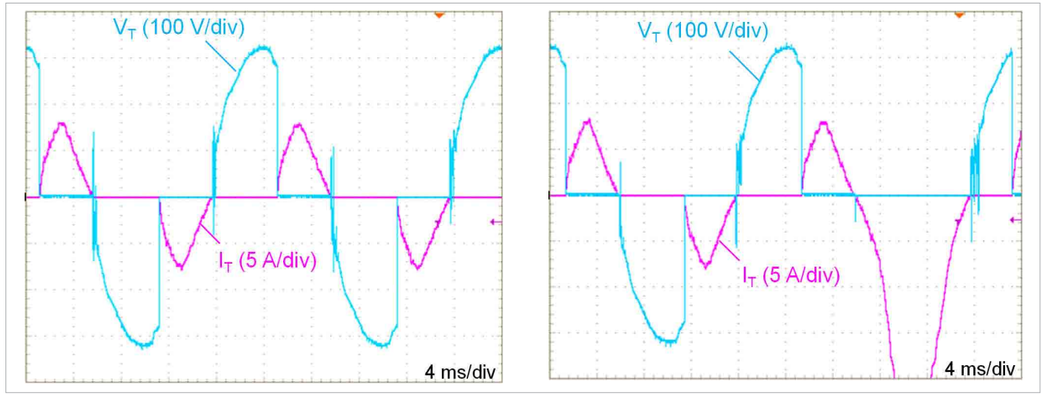


Figure 3: A TRIAC exhibiting proper turn-off (a) contrasts with one operating under condistions that exceed its turn-off capability (b).

Measurements of the BTB16-600CW revealed a TC of 115 °C while dissipating 9 W in an 80 °C TA. Corresponding measurements of the T1235H-6T indicated a TC of 144 °C while dissipating 9.3 W in a 105 °C TA.

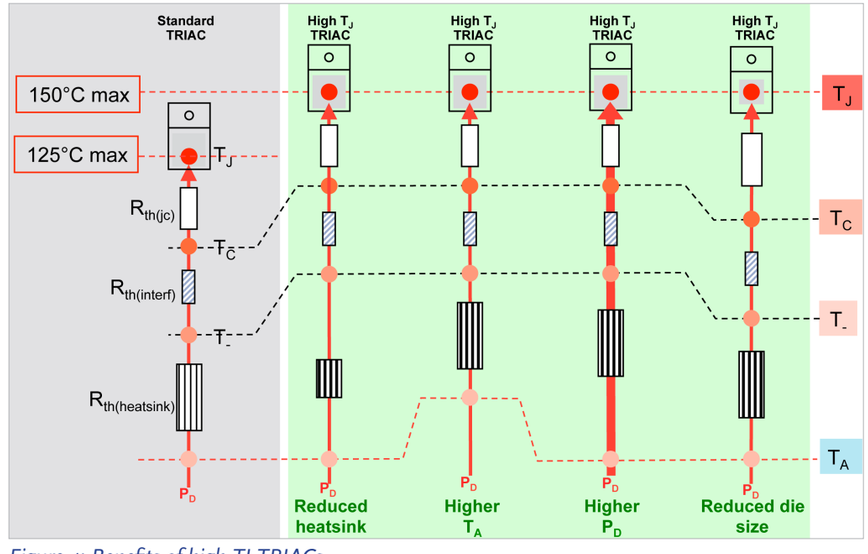


Figure 4: Benefits of high-TJ TRIACs

The BTB TRIAC junction temperature was 123.5 °C and the T1235H junction temperature was 154 °C—slightly above maximum allowed temperature but not critically so for experimental purposes. These results clearly shows an advantage to high-TJ TRIAC since the TA can be set 20°C higher (or 16°C if one wants to keep T1235H-6T TJ below 150°C) than for a standard TRIAC.

Higher TRIAC current

The engineers mounted two 16-A TRIACs (BTB16-600CW and T1635H-6T) now on two identical 3.7 °C/W heatsinks and put them into the same 80 °C ambient temperature. This test increased the load current until each TRIAC was operating at its own maximum allowed junction temperature. For the BTB16-600CW, that applied RMS current was 10 A, at which point the device dissipated 9 W and its TJ was 125 °C. For the T1635H-6T, was able to pass 14 A, dissipating 14.59 W with a TJ of 148 °C.

One key parameter in the choice of TRIACs operating at a high TJ is the turn-off capability—the ability

to remain in the off state even in the presence of a fast voltage excursion after the current has fallen to zero. The turn-off constraint is higher with inductive loads due to the current-voltage phase shift and thus the high dV/dt occurring at TRIAC turn-off.

Figure 3a shows an application example where a TRIAC in phase-control mode is properly driving a universal motor. The load current (pink waveform IT) goes to zero at each half cycle and remains at zero.

Figure 3b, by contrast, shows another TRIAC under the same drive and load conditions. This device loses control of the load because the operating conditions exceed its turn-off capability at high TJ: The high level of the load current during the negative half period shows that the load remains energized even when the TRIAC's drive is off.

Compared to standard TRIACs (TJ[max] = 125 °C), high-temperature TRIACs (TJ[max] = 150 °C) provide significant benefits such as reduced heatsink size, higher TA working capability, higher load-current capability (higher power-dissipation capability), or smaller-current rated device selection potential, reducing die size and cost (Figure 4).

Laurent Gonthier and
Martial Boulin
Application Development
Managers
ST Microelectronics

www.st.com

NEW POWER ELECTRONICS BASED ON GaN MISHEMPTS

GaN-on-Si may hold the key

By: Marianne Germain, Joff Derluyn, and Stefan Degroote

GaN appears to be a highly suitable material for power switching devices operating at high frequencies without suffering major losses.

The Promise of GaN

This is due to the drastically lower on-state resistance of GaN power transistors, combined with considerably reduced input and output capacitances. The higher switching frequency substantially reduces the volume of accompanying passive components such as inductors, transformers, and capacitors.

Thus, a GaN-based power system is smaller and more lightweight than MOS- or IGBT-based systems. Eventually, GaN power electronics will combine these significantly improved operational properties with lower costs. Active components limit the efficiency of present systems.

Converting GaN's potential into success hinges on scaling production to larger wafer sizes and employing appropriate passivation techniques. There is a tremendous opportunity for substantially lowering the energy losses associated with AC-DC and DC-DC conversion. If a new generation of devices can combine higher power levels with lower switching losses at higher operating frequencies, they will boost the efficiency of power systems, while trimming size and weight.

Making Nitrides Affordable

As wide-band-gap semiconductors, GaN-on-silicon devices belong to a superior class of materials: One of their biggest advantages is their high breakdown voltage, which stems from a breakdown field strength that is an order of magnitude higher than that of silicon. Due to the high carrier mobility and concentration associated with the 2DEG (two-dimensional electron gas) of the AlGaN/GaN heterostructure, nitride devices in switching applications also combine a low on-resistance with high switching speed. Additionally, their wide-band-gap properties enable them to operate at high temperatures.

Development of nitride power devices has been underway for more than a decade, and their progress has enabled today's switching devices to outperform their silicon rivals. In the performance stakes, SiC is a tougher opponent, but GaN more than holds its own.

GaN-on-silicon is the most cost-efficient wide-band-gap technology. It has developed to a point where it is feasible to deposit advanced heterostructures on silicon substrates up to 150 mm in diameter. In the near future, this will extend to 200 mm. There is also an opportunity to develop process compatibility with standard CMOS technology. This would open the door for further cost reduction by using existing

lines at 200 mm silicon fabs operating around the globe.

No wonder GaN power-electronics technology is attracting increasing interest. Until very recently, no one was able to achieve a real breakthrough—a reliable device operating at 600 V. This, however, is beginning to change. There have been demonstrations earlier this year of fully qualified 600 V GaN switches and they are slowly finding their way into commercial equipment. Cost, of course, is still an issue, but this reflects the typical learning curve that all novel technologies must undergo.

One of the technical—and economic—challenges is to establish a compound-semiconductor technology in a field where silicon dominates. Although the performance of SiC diodes is attractive for power converter manufacturers, they are too pricey. In addition, until recently these diodes could not pair with SiC transistors, which had been detrimental to the uptake of this first-on-the-market wide-bandgap technology. For GaN technology to be commercially attractive, 600 V devices must be reliably producible on GaN-on-silicon epitaxial structures.

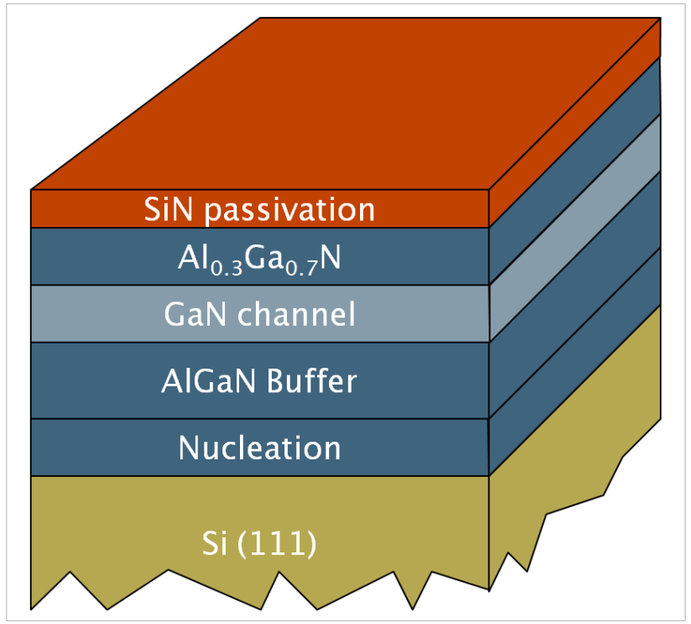


Figure 1: EpiGaN deposits a unique in-situ SiN capping layer, grown by MOCVD on top of HEMT epi wafers.

Taking out the Strain

EpiGaN's epitaxial growth process tackles the grid strain that arises in processes that deposit GaN on silicon. The two materials show different crystalline properties and thermal expansion coefficients. Left unchecked, this can lead to unchecked strain in the epi layer and substrate that can ultimately cause the wafer to bow and even crack.

Carefully managing this strain yields wafers suitable for regular silicon processing lines. The company now routinely manufactures 150 mm epi wafers with a bow well below 50 µm—typically 20 to 30 µm, depending on wafer specs. Uniformity, in terms of standard deviation of either layer thickness or electrical characteristic, is typically better than 3%.

The process optimizes these epi wafers for high-voltage high-frequency operation, which requires the formation of a buffer layer that withstands high voltages. This is because, in devices formed with high-quality GaN layers, the silicon substrate limits the upper breakdown voltage. EpiGaN's epi wafers for high-voltage devices show a buffer leakage current well below 1 µA/mm at 600 V. Operating frequencies above 100 GHz are possible due to the reduction of buffer traps.

Stress engineering certainly is a challenging aspect of forming GaN-on-Si. Even more challenging is the passivation of surface states. A piezoelectric material, GaN has an excellent high-electron concentration associated with high electron mobility—obtained without extra doping.

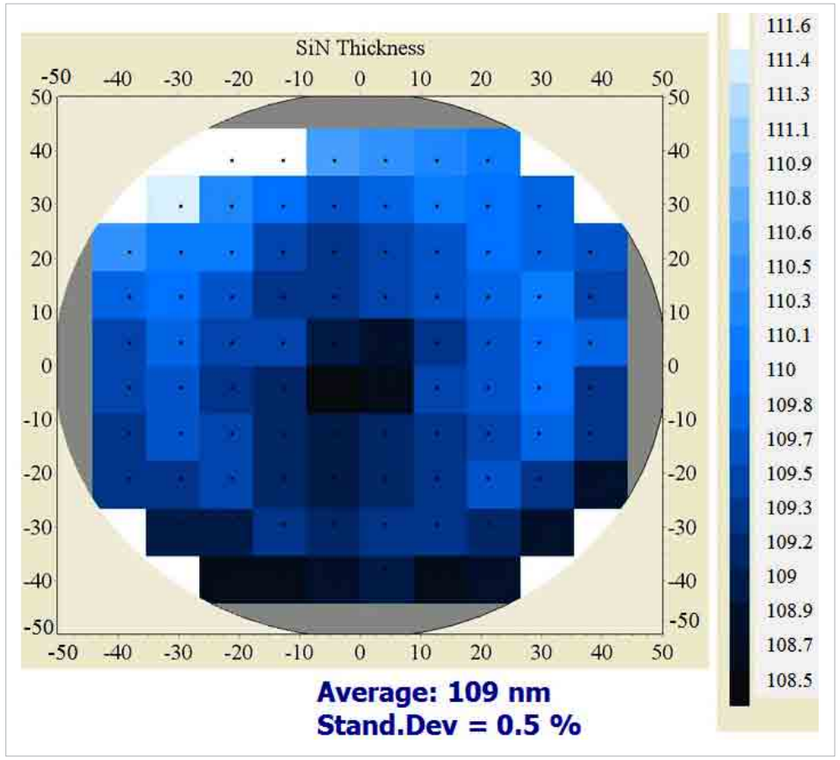


Figure 2: The uniformity of the in-situ SiN layer

The price to pay is an extreme sensitivity governing device characteristics, such as current density and threshold voltage on the filling of those surface states, which have a density comparable to that found in the channel. If passivation is poor, the device's dynamic behaviour suffers. To combat this so-called dispersion problem, fabricators must process devices in a carefully controlled manner using high-quality epi wafers, because this leads to optimized buffers and controlled surface states. Uncontrolled charging or discharging of these surface states, which processing and device operation can modify, can severely degrade the device's dynamic properties. As a countermeasure, EpiGaN deposits a unique in-situ SiN capping layer, grown by MOCVD (metalorganic chemical vapour deposition) as part of the epitaxy process on top of HEMT (high electron-mobility-transistor) epi wafers (Figure 1). The interface between this capping layer and the top nitride surface is incredibly smooth, and it enables excellent passivation of surface states. Many processes use a GaN capping layer, which is less sensitive to the formation of these surface states than the AlGaN barrier in combination with PECVD (plasma-enhanced chemical vapor deposition) SiN that deposits after the MOCVD process as part of the device processing. However, this approach does not have the advantages of the in-situ deposited SiN.

The capping layer can properly control surface-state filling during device operation. It is believed that SiN can provide enough charge to neutralize the surface charge of the AlGaN barrier layer so that its surface potential no longer contributes to 2DEG depletion. In addition, the SiN layer aids device stability at elevated temperatures.

In-situ deposited SiN films can also lead to lower channel resistance. This enables adjusting the top part of the FET so that it can meet particular

device specifications. GaN FETs are lateral devices, and optimizing their performance demands a trimming of conduction losses. This means that, for switching applications, aluminum-rich barriers are preferred in a typical AlGaN/GaN structure, because it yields a higher piezoelectric field, higher current density, and lower specific on resistance.

One of the major benefits of the SiN cap layer is that it enables higher aluminum concentration without any significant material degradation. This is not the case in transistor structures with an uncapped or GaN-capped AlGaN/GaN 2DEG, where relaxation of the strained top AlGaN layer typically prevents high aluminum content in the top layer.

For the SiN/AlN/AlGaN design, sheet resistance falls to 235 Ω/□ with appropriate passivation (Figure 2). For this structure, Hall measurements indicate that the electron sheet concentration is 2.15 x 10^{15} cm^{-2} and electron mobility is 1,250 cm^2/Vs. These are very promising values and they enable the fabrication of devices with high transconductance, even when the gate length is relatively large. They highlight the potential of this device for high-frequency operation.

The neutralization of surface charges provided by the SiN layer also unlocks the door to an innovative approach for making enhancement-mode devices. This form of transistor, which is generally preferred for power converters, can form by combining a thin AlGaN barrier layer with local removal of SiN under the gate.

As for examples of the alternative use of depletion mode transistors, there are very few applications in practice. Using depletion mode devices generally means a work-around on the circuit level to separate the input side from the output side and ensure safe operation. One example thereof is the cascade configuration where a low voltage enhancement-mode Si MOSFET combines with a high-voltage GaN depletion-mode HEMT.

From 600 V to 1.2 kV

EpiGaN now makes GaN-on-silicon wafers with a breakdown voltage above 600 V and very low leakage current. This is by no means the upper limit, however. Recent work has yielded FETs with a breakdown above 2 kV.

GaN is already used for power products in the 30 to 200 V, and 600 V range, and 1,200 V will soon be added. This will pave the way for replacing two silicon MOSFETs with a single GaN HEMT—trimming the cost and weight of power converters.

Future products based on this process will complement the existing range of 4-inch and 150-mm epi wafers for high-voltage and high-frequency applications. Production capacity for these products is currently ramping up. In parallel, processes for 200 mm GaN epi wafers operating at 600 V and 1,200 V are developing. Larger wafer sizes will spur a cost reduction and enable GaN to deliver in a field where, until now, no compound semiconductor has seriously challenged silicon.

Marianne Germain, PhD, CEO
Stefan Degroote, PhD, COO
Joff Derluyn, PhD, CTO
EpiGaN

www.epigan.com

IMPROVING ENGINE STOP-START SYSTEM DESIGN

Integrated MOSFET controllers help engineers overcome electrical challenges in automatic engine stop-start systems.

By: David Jacquinod

Automatic engine stop-start is effective in helping reduce CO_2 emissions from private cars.

When integrated in an otherwise conventional combustion-engine power train, engine stop-start technology can deliver fuel savings of 5 to 15% at a relatively low incremental cost of about 300 USD. Offering worthwhile reductions in fuel consumption and emissions, at a price accessible to a significant proportion of car buyers, the stop-start vehicle is an important staging point in the transition to so-called mild hybrids or full hybrids and, ultimately, plug-in electric vehicles. Market analyst Yole Développement predicts strong demand for stop-start vehicles, rising from 5 million vehicles in 2012 to some 45 million in 2020.

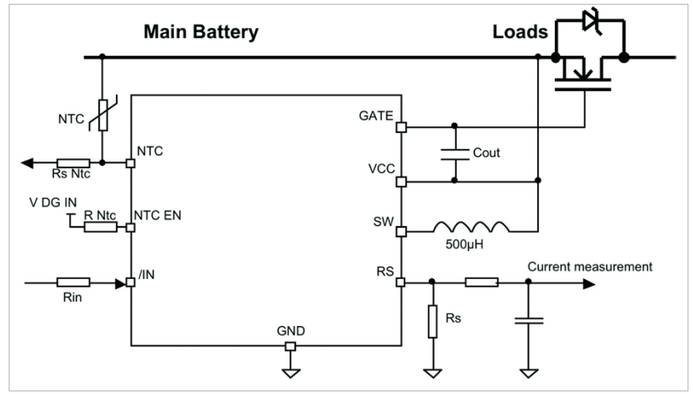


Figure 1: Integrated gate driver with external passive components.

Electrical design challenges

Automatic engine stop-start challenges several areas of vehicle electrical design. One is to protect systems such as the radio, climate control, GPS, and interior or exterior lights against supply-voltage fluctuations during engine cranking. The battery voltage can fall to as low as 6 V during cranking, whereas the electrical systems require a stable supply, or board-net voltage, of 13 V nom to ensure correct operation. Hence an additional subsystem is needed, containing a power switch and associated control circuitry, to disconnect the battery when the engine is cranking, allowing an auxiliary battery or DC-DC converter to supply the loads temporarily.

When the vehicle is operating normally, the power switch contained in this subsystem must supply all electrical loads in the car. Consequently, low conduction losses are imperative because the switch is on at all times except when cranking. This calls for a power MOSFET rated for continuous drain current on the order of 240 A and having low on-state resistance of about 1 mΩ. Connecting several devices in parallel can achieve a further reduction in on-state resistance. Because the battery must remain

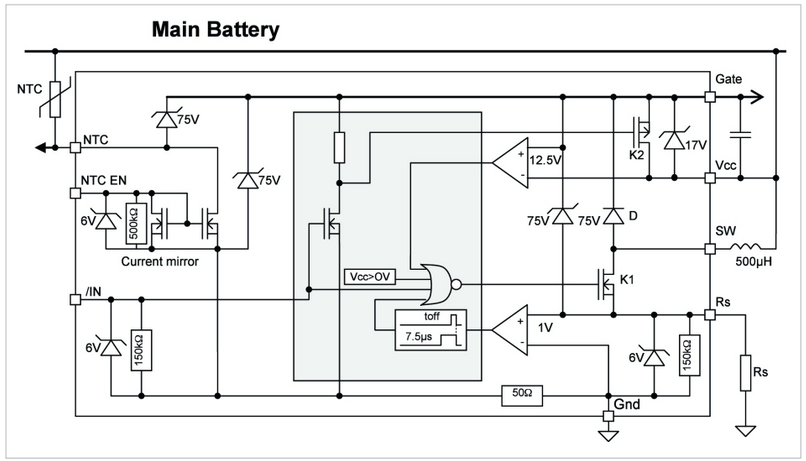


Figure 2: Internal functions of the start-stop gate driver

connected when the car is off, the power switches and the controller, combined, must have a low quiescent current to minimise battery drain. A quiescent current of around 50µA is acceptable.

Controlling the power switch

As soon as the vehicle's auto-start function activates engine cranking, the main battery voltage begins to fall. The power switch must turn off quickly to allow the auxiliary supply to maintain the board-net voltage at 13 V. This is important, because the low resistance of the power switch can allow a high current to flow to the main battery side with a voltage drop of only a few mV. The turn-on time is less critical because the current will flow in the power switch's body diode.

A controller, or gate driver, is necessary to turn on and turn off the power switch. A suitable controller must be capable of providing a gate voltage of 12 V to 15 V when operating from the low main battery voltage. Additional circuitry performs voltage and current monitoring, on- and off-time control, fault diagnostics, and thermal protection.

Designing a driver having low quiescent current and meeting all these requirements, using discrete components, is challenging. Some integrated gate-driver ICs are available, which not only simplify design but can also help increase reliability. However, many are primarily for such applications as mobile phones or PDAs.

IR's AUIR3240S is an example of gate driver ICs for automotive engine stop-start applications. It contains a voltage converter capable of operating from an input voltage in the range 4 V to 36 V and provides a MOSFET-gate drive voltage of 12.5 V. The company optimized the device architecture for intermittent operation, reducing current consumption to less than 50 µA. The gate driver requires only a few external passive components to complete the design: an inductor and a capacitor for the boost converter and resistors for the IC's diagnostic and measurement circuitry (Figure 1).

Key functions include the main DC-DC switch, K1, and freewheeling diode, D, and two comparators to control K1's state (Figure 2). The uppermost comparator monitors the gate voltage compared to VCC, to turn K1 on. The lower comparator monitors the voltage across the shunt resistor connected to the RS pin, which controls the turn off.

A monostable timer with a typical interval of 7.5 µs guarantees a minimum boost converter off time. It activates when the inductor current reaches the peak current fixed by the shunt resistor (Figure 3).

The driver operates at variable frequency. K1's on time depends on the values of supply voltage, shunt resistor, and inductor. The output current fixes the off time. When the output voltage is below 12.5 V, the driver turns on the power MOSFETs and the monostable timer's off time, Toff, fixes the frequency. In this mode, the

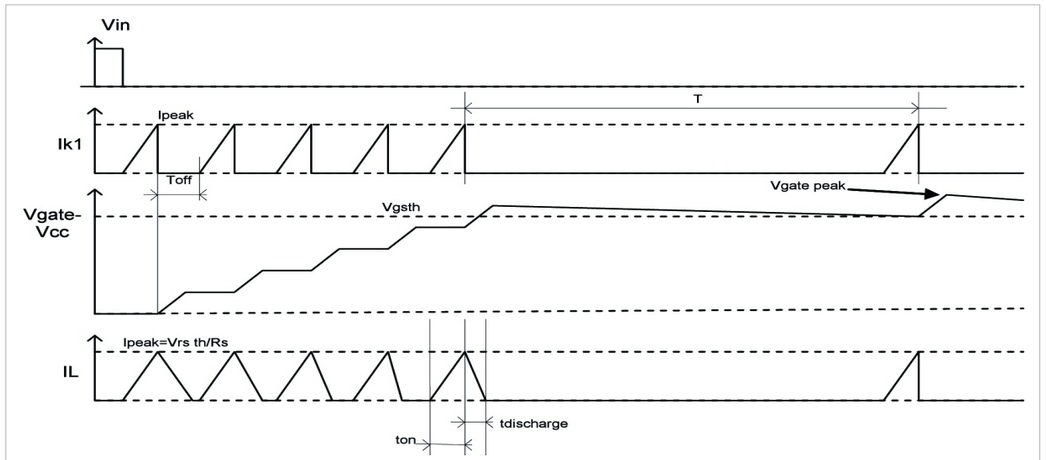


Figure 3: AUIR3240S driver voltage and current waveforms during turn on.

driver can provide a relatively large current—on the order of tens of mA—to charge the MOSFET gates quickly and turn on the power switch. The stop-start system can achieve maximum output current by optimising the values of the inductor and the shunt resistor.

Once the gates of the power MOSFETs charge above 12.5 V, the driver enters a low-current-consumption mode. Then the driver activates only when the gate voltage falls below 12.5 V. With this architecture, the driver can hold the power switch on, with very low current consumption. Gate discharge is mainly due to the driver's leakage current.

Safety and temp monitoring

Since the power switch supplies all the electrical loads in the car, it is a safety relevant function and must be able to detect failures. The AUIR3240S provides two diagnostic mechanisms for monitoring both correct output current and excessive system temperature.

By adding an RC filter to resistor RS, the system can monitor the average output current (Figure 1). The values of current flowing in the output and at the RS pin link by:

$$I_{OUT}(avg) = I_{Rs}(avg)\frac{V_{CC}}{V_{GATE} - V_{CC}}$$

In low-current-consumption mode, with current of 50µA and RS equal to 10 Ω, the voltage reading will be 0.5 mV. If a short circuit is present at the output, the driver will try to regulate the output resulting in a voltage of several hundred mV depending of the values of L and RS. Additionally, when the system operates to turn on the power MOSFET, a peak current will charge the gate. By monitoring the current during the turn-on, the system can detect continuity between the MOSFET and the output.

The driver provides an NTC interface allowing the system to monitor the MOSFET die temperature, using one standard resistor and one NTC device located close to the MOSFET's source. The circuitry operates as a current mirror between the NTC_EN and NTC pins. The ratio is typically 2:1 so 500 µA must flow in the NTC_EN to achieve a current of 1 mA in the NTC pin. R_Ntc and V_Dg_In determine the NTC current. For example, 7 kΩ and 5 V will result in an NTC current of 1 mA.

David Jacquinod
Application and Marketing Manager
Automotive Business Unit
International Rectifier Corporation

www.irf.com

Special Report: Grid Power

PSD NORTH AMERICA
Power Systems Design: Empowering Global Innovation

Inside:

SECURING THE LIFE CYCLE IN THE SMART GRID

Hardware-based security precautions enhance grid security

By: Kris Ardis

Investment in smart meters and smart-grid end equipment continues to grow worldwide as countries try to make their electric delivery systems more efficient.

As critical as the electric delivery infrastructure is, it is normally not secure, and thus is subject to attack. The concept of life-cycle security encompasses the idea that embedded equipment in the smart grid must have security designed into the entire life of the product, even back to the contract manufacturer.

Security is an increasingly critical subject in the smart grid. With regular attacks on smart-grid infrastructure, there is a clear threat: The stable supply of electricity in every nation is at risk of compromise by unfriendly forces.

In response, there is a great focus on IT security. Many systems support end-to-end encryption between embedded data-collection devices on the smart grid and the SCADA (supervisory control and data acquisition) systems that analyze and react to the data. This focus on IT security is undoubtedly critical, as systems must protect data in flight with standards-based cryptography. However, even with the strongest end-to-end encryption, there is a severe shortcoming in smart-grid security: The embedded device itself is highly vulnerable to attack.

Encryption is security, right?

While cryptographic tools are critical for ensuring the privacy and authenticity of transmitted data and commands, it is important to note that it is only solves one part of the problem. Encryption's greatest value is to protect data when it is in transit or in storage to prevent deciphering or forgery. While there are some who believe that a complex RF or power-line carrier that relies on frequency hopping provides enough security to obscure data, this is a protection easily broken by attackers.

Imagine if an attacker could generate an arbitrary command to open the remote disconnect switch in a smart meter. Such an act could disrupt electric service for a large number of people and service requests would swamp the utility. Not only could this result in a significant loss of revenue to the utility and impose severe inconveniences on its customers, it could be life threatening in regions where, for example, air conditioning is a necessity.

What happens to the data before it enters the pipe and after it exits? There are encryption keys at either end of communication pipes that encrypt, decrypt, authenticate, or validate the data in transit. While the encryption of the data in the pipe is critical to secure information as it passes from embedded sensor to the control system, the protection of the secret keys used in the encryption is even more important. A security compromise affecting the keys can compromise the security of the network. Embedded endpoints in the smart grid must consider key security to provide more complete system security. Secure financial terminal technology, for example, emphasizes key protection, using multiple layers of protection to protect on-chip keys from physical and analytical attacks.

The validity of data and commands flowing in the smart grid is not the only avenue of attack to disrupt the supply of electricity. Clever viruses such as Stuxnet have proven the danger of attacks that change the fundamental behavior of embedded equipment in a manner that is difficult to detect. A class of threats called zero-day attacks exploits systems that allow erasure or reprogramming, breaking a system in undetectable ways. We need not only worry about equipment when it is deployed, but at any time it is vulnerable to improper programming—including during manufacturing.

But what could go wrong?

Designing for security is difficult, time consuming, and requires security expertise. Is the investment really worth it? For a moment, let's consider a deployed smart meter. Since meters generally sit unprotected on our homes, it is easy for an outsider to gain access. If a meter uses a conventional microcontroller for applications and communication processing, it is likely that there is an attack path through the programming interface, allowing the attacker to reprogram the meter or read out its contents.

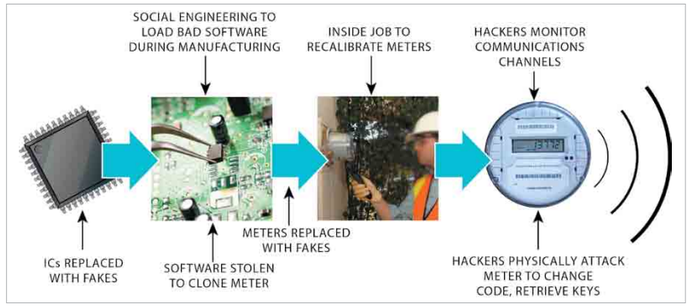


Figure 1: A conscientious life-cycle design will consider threats at every step of product development and manufacturing.

With enough resources and time, someone could even create a program that behaves exactly like the previous meter program, but with hidden viruses that collect key data or alter the reporting of electricity consumption.

Deployed meters require protection to ensure their functions are inalterable. However, if we look back in time, we see a moment when the meter is even more vulnerable—the manufacturing floor. There is always the possibility that social engineering can give attackers access to your IP and manufacturing flow. Armed with a few thousand dollars, an attacker could procure your software, reverse engineer it, alter it, and provide a new program to the manufacturing flow. Additionally, the attacker could sell the software to a competitor, giving another company an unfair benefit from your research and design expenses.

How to secure the life cycle

A conscientious life-cycle design will consider threats at every step of product development and manufacturing, and determine if those threats warrant countermeasures (Figure 1). To implement a secure life cycle, consider the following:

1. Make sure you procure valid silicon. Purchasing through authorized or direct channels can help, but there are cryptographic techniques as well. Some IC manufacturers, including Maxim Integrated Products, sell secure microcontrollers and smart-grid products preprogrammed with the customer's key or certificate, ensuring that only the intended customer can unlock and program that IC.

2. Protect your IP. Deliver signed, encrypted code to your manufacturing operation. This requires cooperation from a secure bootloader inside your system microcontroller to decrypt and authenticate the software once delivered to the chip. The encryption protects against reverse engineering or cloning.

3. Only run the code you intended to run. A secure bootloader

can use the digital signature on your software to validate the authenticity of the code before loading or running the application.

4. Trust who you are communicating with. Encrypt and sign new configurations, firmware updates, and commands to validate that they issue from a trusted source.

5. Protect your keys in the field. Don't store encryption keys in an IC separate from where you will use the key, such as in an external EEPROM. If you have a separate secure microcontroller and applications processor, keep the keys in the secure chip and never send them anywhere else. Keys transmitted across PCB traces are easy for an attacker to extract.

6. Protect your keys inside your company. Use development keys for engineering to design security features into your products. Protect access to the production keys by requiring multiple users to authorize the use of production keys. An HSM (high-security module) can help implement some of these policies.

7. Don't rely on a single point of failure. If an attacker only needs to extract keying material from one meter to break the system, they can invest more time and money into that attack knowing that they can then break the entire system. Sophisticated attackers might even decapsulate the IC package and microprobe memories in search of keying material. Use unique keys or use asymmetric cryptographic schemes like elliptic-curve digital signatures.

Kris Ardis
Business Director, Smart Grid Products
Maxim Integrated Products

www.maxim-ic.com

IEC 61850 INCREASES GRID RELIABILITY

Substation automation bolsters transfer performance

By: Howard Self and Cleber Angelo

A power industry consultant recently asked for assistance solving a reliability problem for a municipal utility.

The utility had recently experienced disturbances on its system, negatively affecting one of its industrial customers. The customer connects to an old portion of the city's distribution grid that requires upgrading, but due to budget constraints, an upgrade is not currently an option. The city serves this customer from two 46 kV to 8.46 kV substations (Figure 1). The two overhead 46 kV circuits are several miles long and are susceptible to the challenges of overhead distribution systems, including lightning strikes.

The consultant and the utility reviewed the service requirements and determined the need to isolate a fault and then transfer to an un-faulted source in only a few cycles. Their requirements also dictated the use of outdoor circuit breakers or pole-mounted reclosers. The city's existing communications infrastructure included a high-speed fiber network available at all subject locations and available for protection or control when required.

The utility operates with the two main 8.46-kV circuits closed, and a transfer-tie breaker open (Figure 1). Any disturbance on either 46-kV circuit severely affects the utility's equipment by dragging the 8.46-kV bus voltage to unacceptable limits. The rotating machines on the customer side decouple if the 8.46-kV bus voltages fall below 0.85 kV nominal for 10 cycles.

To support utilities' grid enhancement efforts, ABB recently established a Distribution Automation Verification Lab in Raleigh, NC as part of its new Smart-Grid Center of Excellence. This lab enables utilities to verify functionality, interoperability, and operational expectations for distribution-grid management subsystems, including verification of non-ABB assets. In the ABB verification lab and demonstration area, there are five 15-kV 12.5-kA

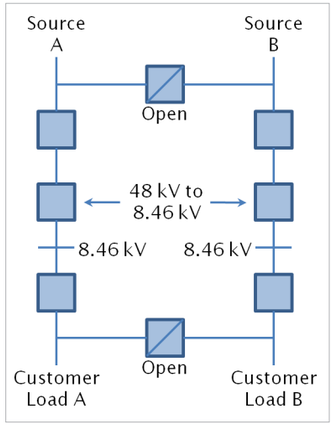


Figure 1: Redundant 8.46 kV lines power an industrial customer's facility.

reclosers equipped with recloser protection-and-control relays, and two 15-kV 25-kA outdoor circuit breakers equipped with feeder protection-and-control relays.

All of the relays have secondary phase-voltage inputs (Va, Vb, and Vc) and phase-current inputs (Ia, Ib, Ic, and In) connecting back to a central test panel where an Omicron C356 test set can inject precision analogs signals. Inputs

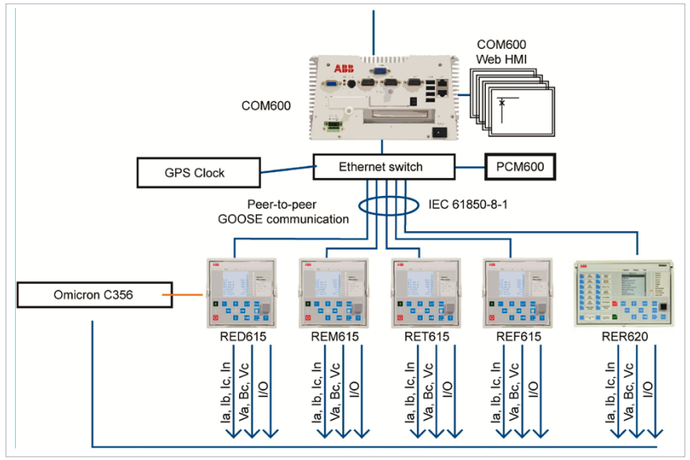


Figure 2: ABB's Distribution Automation Verification Lab configuration can replicate a utility's field configuration.

and outputs also wire back to the central control panel from each IED (intelligent electronic device) for monitoring circuit breaker position, triggering the test set, and allowing for input triggering on all IEDs simultaneously. A substation computer or a communication gateway that emulates the SCADA/DMS (supervisory control and data acquisition / distribution management system) can control the overall system. The overall system configuration replicates the utility's field configuration in a lab environment (Figure 2).

One of the project objectives was the accuracy and repeatability of results, and this data was a part of the deliverables expected by both the consultant and the utility. Due to the multiple IEDs used to gather results in these tests, precision timing was critical. To support these requirements, a GPS clock with an SNTP (simple network time protocol) output connected to the network (Figure 2). The IEDs synchronized to the main system clock source within 1 ms time accuracy and several pre-test checks ensured result accuracy. A series of triggers via binary outputs and Generic Object Oriented Substation Events (GOOSE) messages issued on all IEDs simultaneously to validate controlled triggers and to produce the same events across the network to within 1 ms. The performance validation used the SOE (Sequence of Events) records and fault recording data from the IEDs.

The first test involved the outdoor circuit breakers with protective relays. In addition to protection, control, and metering, each relay has many standard features. These include graphical user-programmable logic, digital fault (waveform) capture, SOE and fault recording, monitoring, load profile, internal web server, and advanced Ethernet communications supporting IEC 61850-8 with GOOSE (peer-to-peer) messaging (Figure 3).

Test 1 measured three events: (1) The time for the outdoor breaker equipped with relay to operate under no-load conditions for a manual trip. (2) The time for the remote relay to receive the GOOSE message the auxiliary contact triggered. (3) The time for the outdoor breaker to open upon receiving the GOOSE trigger. The

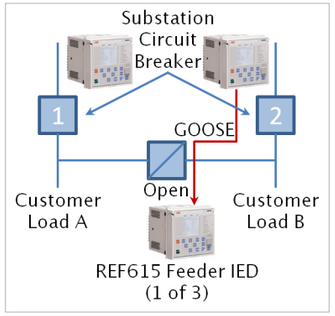


Figure 3: An application example of feeder protection-and-control IECs.

relay's digital fault recorder was set to sample at 32 samples per cycle and record for 50 cycles. Recordings began on rising edge triggers.

After triggering events in both relays, engineers combined the recordings for analysis. In summary, the text executed with 58 ms open time, 2 ms GOOSE time, 71 ms close time, and 131 ms total time. The test team conducted this test 25 times to ensure consistent results. GOOSE time stayed very consistent and the breaker open and close times varied by no more than 2 ms.

The second test applied fault current of 25 times I nominal to the relay using an Omicron test set. The instantaneous over-current element initiated the trip when it detected the disturbance. The test produced virtually identical timing results from the initiation of trip through complete transfer. The test results consistently achieved less than 8-cycle transfer times under no-load conditions with the outdoor circuit breakers: 58 ms open time, 2 ms GOOSE time, 71 ms close time, and 131 ms total time.

Test 3 used reclosers equipped with RER620 multifunction IED controllers in place of the breakers and REF615 IEDs in a topology similar to Figure 3, to determine if the performance could improve. The test executed with 38 ms open time, 3 ms GOOSE time, 41 ms close time, and 82 ms total time. The test delivered improved results from the initiation of trip through complete transfer. The test validated that less than 5-cycle transfer times were achievable under no-load conditions.

Engineers tested multiple scenarios using different over-current and under-voltage conditions to ensure the results were accurate and consistent. These tests were the consultant's first exposure to the IEC 61850 Standard and GOOSE messaging capabilities. Upon sharing the test results and procedures with the consultant, he was both pleased and surprised at the ability to initiate actions between devices without the need for physical IO, the ability to monitor GOOSE health, and the ease in which these actions were configurable using the relay's engineering software.

Based on the success of the first three tests, the consultant requested an additional test simulating a transfer scheme. The test scenario applied an under-voltage condition to the local recloser, allowing the trip element to issue a trip command and simultaneously transmit a GOOSE message to the remote recloser to close. The results were 50 ms open time, 18 ms GOOSE time, 59 ms close time, and 59 ms total time.

The results of the transfer scheme test verify that it is possible to detect and transfer in less than 4 cycles. The system fault detection, isolation, restoration, and transfer scheme was based on the ABB Relion family of relays' native IEC 61850 capabilities with GOOSE, combined with R-MAG distribution outdoor breakers, and GridShield reclosers.

About the author:
Howard Self
Program Manager

Cleber Angelo
Medium Voltage Global Outdoor Product Manager, ABB

www.abb.com

TEST TODAY YOUR PV INVERTER FOR TOMORROW

Independent test facilities demonstrate inverter performance to utilities' requirements

By: Erik de Jong

An increasing number of DERs (distributed energy resources), which include storage systems, are connecting to the grid by means of inverters.

This is already evident in countries with dedicated stimulus programs, such as Germany, which has seen the amount of PV-production increase significantly over the last few years. Now that solar PV power plants have reached MW scale, the question arises as to whether these large-scale systems can integrate into the power system and maintain the currently accepted levels of security and power quality.

Challenges ahead

One of the greater challenges that utility companies face in integrating solar PV energy is to guarantee the same level of power quality at any moment in all circumstances. The fluctuating production of solar energy is a threat to stability. Although short power fluctuations diminish with the growing scale of the systems, the supply of solar energy is hard to predict. PV power plants do not have controls or other generating capacity to compensate for frequency fluctuations; the installation switches off immediately once clouds cover the sun.

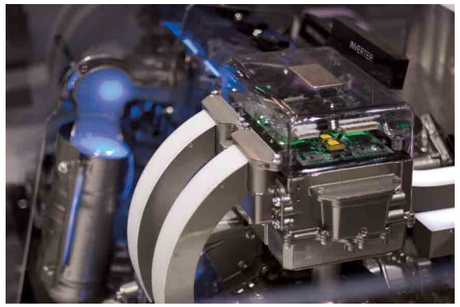


Figure 1: Micro-inverters convert direct current from individual solar panels into alternating current for the electric grid.

Inverters convert the DC electricity from sources such as solar panels to AC electricity at any required voltage. Micro-inverters convert direct current from individual solar panels into alternating current for the electric grid (Figure 1). They are grid-tied designs by default. The larger the PV power plant, the larger the inverter capacity, the greater the impact on the power quality because inverters and control systems cannot affect raw solar-power production. Grid irregularities, such as frequency variations, phase shifts, or voltage dips, should not affect the PV plant's production.

Assured performance

Operators of solar PV power plants have to be sure that their PV inverters behave as specified in all circumstances. Performance evaluations at independent test facilities, such as DNV KEMA's FPGL (Flex Power Grid Laboratory), can assure both supplier and operator that inverters perform to utility requirements (Figure 2). The FPGL simulates the operation of an integrated 10 kV distribution network and is equipped for testing gird-tied low- and medium-voltage

Figure 2: Performance evaluations at independent test facilities, such as DNV KEMA's FPGL (Flex Power Grid Laboratory), can assure both supplier and operator that inverters perform to utility requirements.

inverters with power ranges up to 1 MVA.

A manufacturer of inverters or supplier of turnkey PV power plants needs to demonstrate that grid-tied designs meet the network owner's demands. "The proof of the pudding is in the eating". A better place to test inverter than under live grid conditions is hard to imagine. The test facility can pollute the electrical environment to the clients' demands and according to international standards, with test results reflecting the consequences for grid stability.

As there is no international standard for testing PV inverters at this moment, a number of existing international and German standards fill in the gap. In facilities like the FPGL, grid-tied inverters are often tested to the IEC 61683:1999—PV systems - power conditioners, procedure for measuring efficiency.

Additionally, the German BDEW (Bundesverband der Energie- und Wasserwirtschaft) Guidelines are applicable such as the FGW-Technical Guidelines for Power Generating Units - Part 3 - Determination of electrical characteristics of power generating units connected to MV, HV, and EHV grids. Other relevant sections include Part 4 -Demands on Modeling and Validating Simulation Models of the Electrical Characteristics of Power Generating Units and Systems, and Part 8 - Certification of the Electrical Characteristics of Power Generating Units and Systems in the Medium, High and Highest Voltage grids.

It is also common for test facilities such as DNV KEMA's to offer test programs that conform to IEC 60068 Environmental Testing. Successfully passing industry-accepted tests opens the gateway towards the large emerging market of large-scale PV power generation.

Transformers and harmonics
When inverters, especially those with sub-standard emission levels, become commonplace in low- and medium-voltage distribution grids, they risk exposing distribution grid equipment, such as MV/LV transformers, to more severe power-quality phenomena such as increased THD (total harmonic distortion). This situation can expose the transformer (and remaining grid equipment) to extra losses due to the harmonic content, which will, apart from the audible noise and vibration, result in increased operating temperatures and a reduced power capacity.

The FPGLab in cooperation with Alliander has performed research to quantify in detail the thermal effect of an extensive range of individual harmonics (all harmonics up to the 15th with the maximum allowed voltage amplitudes according to the EN 50160) on specific parts of a 250 kVA, 10 to 0.4 kV distribution transformer. The FPGLab facility provided the harmonics on demand on both the MV and LV side of the transformer at full-load. Temperature sensors (fibre-optic as well as PT100) specially installed throughout the transformer's internal structure reported the various temperatures.

Researchers recorded power loss contributions up to 11% of the total power for the 9th and > 5% for the 3rd harmonic. Notably, the combination of 5th and 7th harmonic (six-pulse bridge) resulted in a relatively low 4% loss contribution. The research results are applicable together with other transformer data to verify specific models for use in grid planning and asset management.

Erik de Jong
Managing Director
Flex Power Grid Laboratory

www.kema.com

ENERGY-STORAGE SYSTEMS POSE SMART-GRID DESIGN CHALLENGES

By: David G. Morrison

Renewable energy systems such as solar arrays and wind farms provide the utility grid with new sources of power generation to meet growing energy demands.

However, these systems do not inherently support the grid through various types of disturbances and fluctuations in grid operation. That's where energy storage systems (ESS) come in. Typically battery-based, energy storage systems have the ability to inject real or reactive power onto the grid, or conversely absorb real or reactive power from the grid, as a means of stabilizing the grid and compensating for any changes in voltage or frequency. Such systems are expected to play an important role in the development of the smart grid. Both the venture capital now flowing into the industry and the proposed legislation on investment tax credits attest to the great expectations for grid-tied ESS.

Power electronics are integral to these systems providing bi-directional power conversion and managing the flow of energy between the batteries and the grid. In some applications, the power electronics may also be handling power conversion and energy flow among other energy sources and loads such as solar arrays and electric vehicles. Consequently, power system designs for energy storage systems can be quite complex (see the figure.)

Figure

Figure. Complex, high-wattage power systems such as this 50-kW multi-port inverter from Dynapower Company—which provides power conversion and manages energy flow between batteries, solar arrays, and vehicle chargers—are at the heart of grid-tied energy storage applications.

Power systems developed for grid-tied energy storage are also distinguished by their

megawatt-scale power levels, and their requirements for extreme reliability and safety. There also additional demands imposed on these power systems because they interface with the power grid and are subject to certain utility industry standards, which are sometimes in conflict with the design goals for the energy storage system. As a result, the grid interconnection requirements lead to certain challenges for power electronics engineers in developing power systems for energy storage. Specifically, there are difficulties associated with the design of transformers that connect the ESS to the grid and the design of the system's response to certain fault conditions on the grid.

I recently discussed these design challenges with Kyle B. Clark, Advanced Systems Engineering Manager at Dynapower Company, a firm that develops power converters for energy storage systems. Clark explained why these challenges affect the work done by PE engineers in this industry, and talked about the technologies that will influence the advance of power system design for ESS. Clark also shared his thoughts on the types of skills and experience that make PE engineers well suited to work in this industry.

Unique Design Challenges

Large transformers are a key element of grid-tied energy storage systems. On one end of the system there's a dc energy source, typically a battery, which then connects to the power conversion equipment. That generally includes an inverter/ac-dc converter (i.e. a bi-directional power converter). This power converter interfaces to the grid through a large, line-frequency transformer. Utilities would prefer this to be a conventional, oil-filled power distribution transformer, like the standard 2-MVA transformers that provide distribution to an industrial complex or a feeder line. Utilities favor this type of transformer mainly because it's what they are accustomed to using. However, its characteristics are wrong for the energy storage applications, which require more of a pulse transformer.

Clark describes how a transformer optimized for an energy storage system will differ from a distribution transformer. "It's going to be smaller and less costly with a smaller thermal mass, but it's going to have the capability to operate at very high peak power—a cross between a power transformer and pulse transformer," says Clark.

For power electronics engineers, there is the challenge of designing the transformer to optimize the performance of the system but also of working with the utilities and others in the industry to define new standards for such transformers, so that the utilities can specify and approve them on a large scale. For example, IEEE C57 defines power distribution transformers, but since these specifications do not match the requirements of ESS, a new standard needs to be developed. As Clark explains, a transformer designed to meet IEEE C57 is inherently mismatched to an energy storage system. "It would be grossly overdesigned for long time-constant heat rejection and it would be underdesigned for short time-constant overloads."

In addition to transformer design and specification, there's another fundamental challenge in the design of ESS concerning the interconnection of these systems to the grid.

"There's a big roadblock in interconnecting energy storage systems because the utility either views them as a load or as a generation source. And if grid-tied energy storage systems are viewed in the same light as, for example, small solar photovoltaic systems, they impose IEEE 1547 on the grid-tied energy storage system," says Clark. The requirements of this standard compromise the performance of the energy storage system in stabilizing the grid.

"As an example, if the frequency and the voltage start to drop on the grid, in certain cases the worst thing for a generating facility to do is to jump off line because it will only exacerbate the problem. But if you are viewed the same as a small solar farm, then you are mandated to jump off line when you drop below the 1547 voltage protection thresholds," says Clark, who explains that the energy storage system should behave differently to support the grid.

"The best thing for it [a grid tied energy storage system] to do is to start injecting high amounts of capacitive VARs. That will help stabilize the grid. So there's a big opportunity for grid-tied energy storage systems to provide grid support by injecting VARs when there are grid perturbations. That requires not only the engineering to make that happen elegantly—so that your entire power system isn't fighting with itself—but also that the utilities be able to palate the fact that a grid-tied energy storage system does not fit into the same category as a solar array, wind farm or any generation source for that matter. It's really an animal of its own because it can provide controllable real and reactive power in both directions." Again, the challenges here for engineers involve both the design of the power electronics, but also working with the utilities to create appropriate industry standards.

Potential Impact of New Technologies

A number of technological developments are expected to improve performance of energy storage systems in the future. On the topology front, a move away from three-legged standard PWM-controlled power conversion is expected. "I think that the interesting developments are going to come when we go to multi-layer, multi-level inverters for higher-voltage energy storage, so we can operate more efficiently," says Clark.

Meanwhile, as with other high-power applications, the arrival of new power switches based on wide-bandgap materials should be a game changer. "The silicon carbide revolution is coming on. We're just getting our hands on the first couple commercially available silicon carbide switches. We're going to reduce costs, increase efficiency and grossly reduce harmonics with the ability to switch at two to three times the frequency that we're switching now with the same or lesser losses. That's going to be a great revolution," says Clark.

There will also be improvements through the development of what Clark describes as "hybrid systems." "There are going to be systems that have a very fast component and a slow component. We're going to be merging and mixing IGBT-based systems with thyristor-based systems to get to the 100-megawatt levels of power conversion while still maintaining the dynamic four-quadrant operation of the smaller power IGBT-based systems. So the hybrid power electronics systems are going to get us on the multi-megawatt transmission-level of energy storage."

To learn more about the types of engineering experiences that help prepare power electronics engineers for work on grid-tied energy storage applications, see "Finding the Right Engineers," in the online version of this article. For more information about Dynapower, see http://www.dynapower.com/.

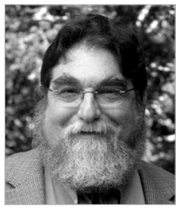
About the Author

When he's not writing this career development column, David G. Morrison is busy building an exotic power electronics portal called How2Power.com. Do not visit this website if you're looking for the same old, same old. Do come here if you enjoy discovering free technical resources that may help you develop power systems, components, or tools. Also, do not visit How2Power.com if you fancy annoying pop-up ads or having to register to view all the good material. How2Power.com was designed with the engineer's convenience in mind, so it does not offer such features. For a quick musical tour of the website and its monthly newsletter, watch the videos at www.how2power.com and http://www.how2power.com/newsletters/.

David G. Morrison, Editor, How2Power

How2Power.com

SMALL-SCALE RENEWABLES ARE PART OF A BALANCED GRID STRATEGY



By Joshua Israelsohn, Editor-in-Chief, Power Systems Design

I've spent much time this year speaking with experts at companies involved with renewable generation and power conversion.

Few of these failed to point out concerns with the current state of electric-transmission and -distribution infrastructure, particularly here in the United States. Punctuating this observation, the refrain "but near-term upgrades aren't likely" is all but automatic.

Although from a generating-site perspective, bigger is better, from a distribution perspective, large-scale generating facilities can raise issues further down the line, particularly if site selection is based on local raw-resource availability—usually wind or sunlight—rather than proximity to need. Among these issues are power losses through transmission and distribution networks and infrastructure capacity.

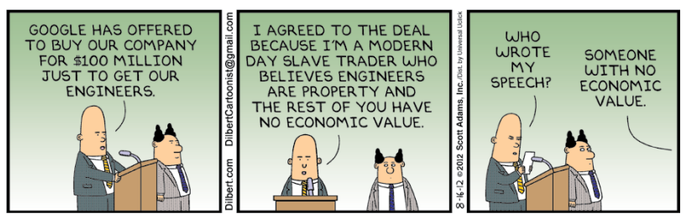
By contrast, small-scale renewables generate electricity at or near their loads and, thereby, reduce stress on the distribution network. In some cases, the variability of renewable generation fits a site's energy-use profile, reducing the effect generating variability has on the resource's grid value—a sharp contrast to large-scale renewables.

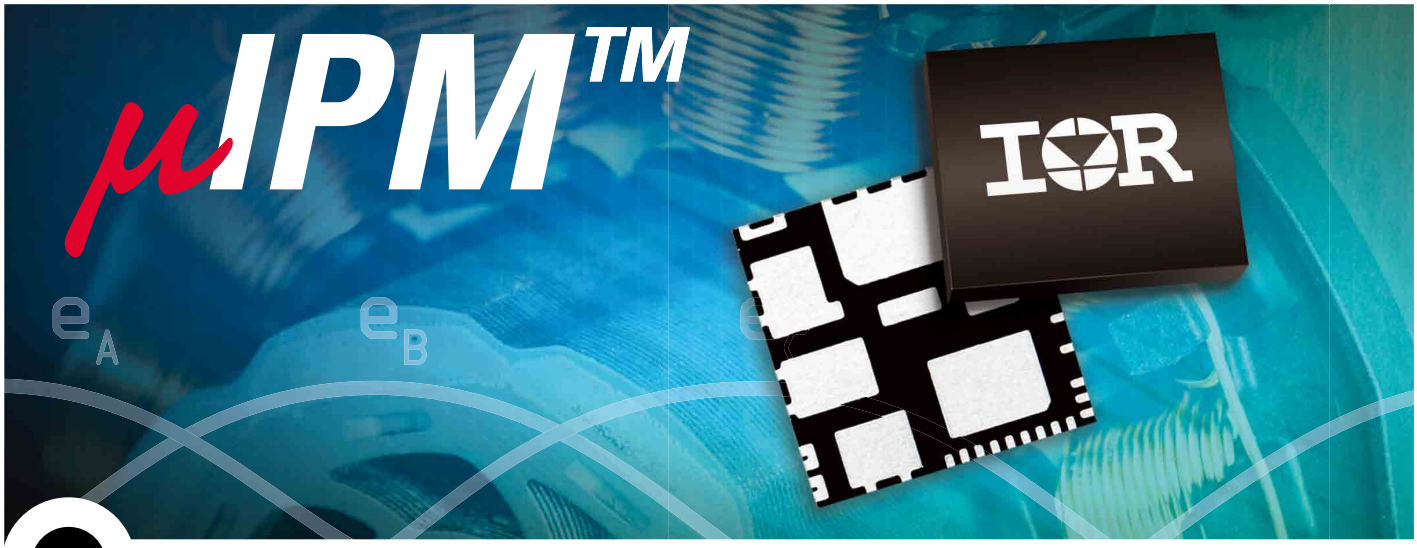
For example, the 2-million-sq-ft Cummings Center in Beverly, MA was, from its construction in 1903 until 1937, the world's largest reinforced concrete building (http://bit.ly/OdK8Ho). Converted to a business and technology campus in the late 90s, the site started solar-generation operations this past June.

The campus hosts 600 kW of solar arrays and two installations in development should raise on-site capacity to > 1.5 MW, saving about $2.5 million annually. The benefit extends beyond the site's bottom line: As generating capacity grows with energy demand, the site stresses the local utility's distribution network less, which benefits the surrounding community as well.

A balanced grid strategy takes advantage of renewables at both ends of the scale.

www.powersystemsdesign.com





Innovative Power Module Reduces System Size

µIPM™ Power Modules Deliver up to 60% Smaller Footprint

Specifications:

Part Number	Size (mm)	Voltage	IO (DC@ 25°C)	Motor Current**		Motor Power VO=150/75VRMS	Topology
				w/o HS	w/HS		
IRSM836-024MA	12x12	250V	2A	470mA	550mA	60W/72W	3P Open Source
IRSM836-044MA	12x12	250V	4A	750mA	850mA	95W/110W	3P Open Source
IRSM836-025MA	12x12	500V	2A	360mA	440mA	93W/114W	3P Open Source
IRSM836-035MB	12x12	500V	3A	420mA	510mA	108W/135W	3P Common Source
IRSM836-035MA	12x12	500V	3A	420mA	510mA	100W/130W	3P Open Source
IRSM836-045MA	12x12	500V	4A	550mA	750mA	145W/195W	3P Open Source

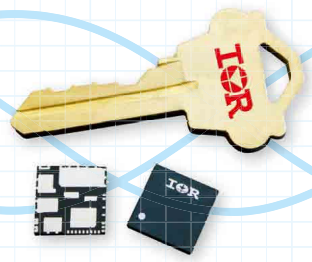
Features:

- 3-phase motor control IC
- 12x12x0.9mm PQFN package offers up to 60% smaller footprint
- Eliminates the need for heat sink
- DC current ratings from 2A to 4A
- Voltage range of 250V – 500V

µIPM™ Advantages:

- Shortens design time
- Shrinks board space requirements
- Simplicity - Eliminates Heat Sink
- Replaces more than 20 discrete parts to deliver a complete motor drive stage
- Slashes assembly time and cost
- Simplifies procurement and inventory management
- Reference design kits available for quick evaluation on any 3-phase motor

iMOTION™ *
INTEGRATED DESIGN PLATFORM
DIGITAL ANALOG POWER



* IR's iMOTION™ (ai mo shan), representing the intelligent motion control, is a trademark of International Rectifier
** RMS, Fc=16kHz, 2-phase PWM, ΔTCA=70°C, TA ≈ 25°C

for more information call 1.800.981.8699 or visit us at www.irf.com

Visit us in Hall A5, Booth 320

electronica
New Munich Trade Fair Centre
13-16 November 2012

International
IOR Rectifier
THE POWER MANAGEMENT LEADER