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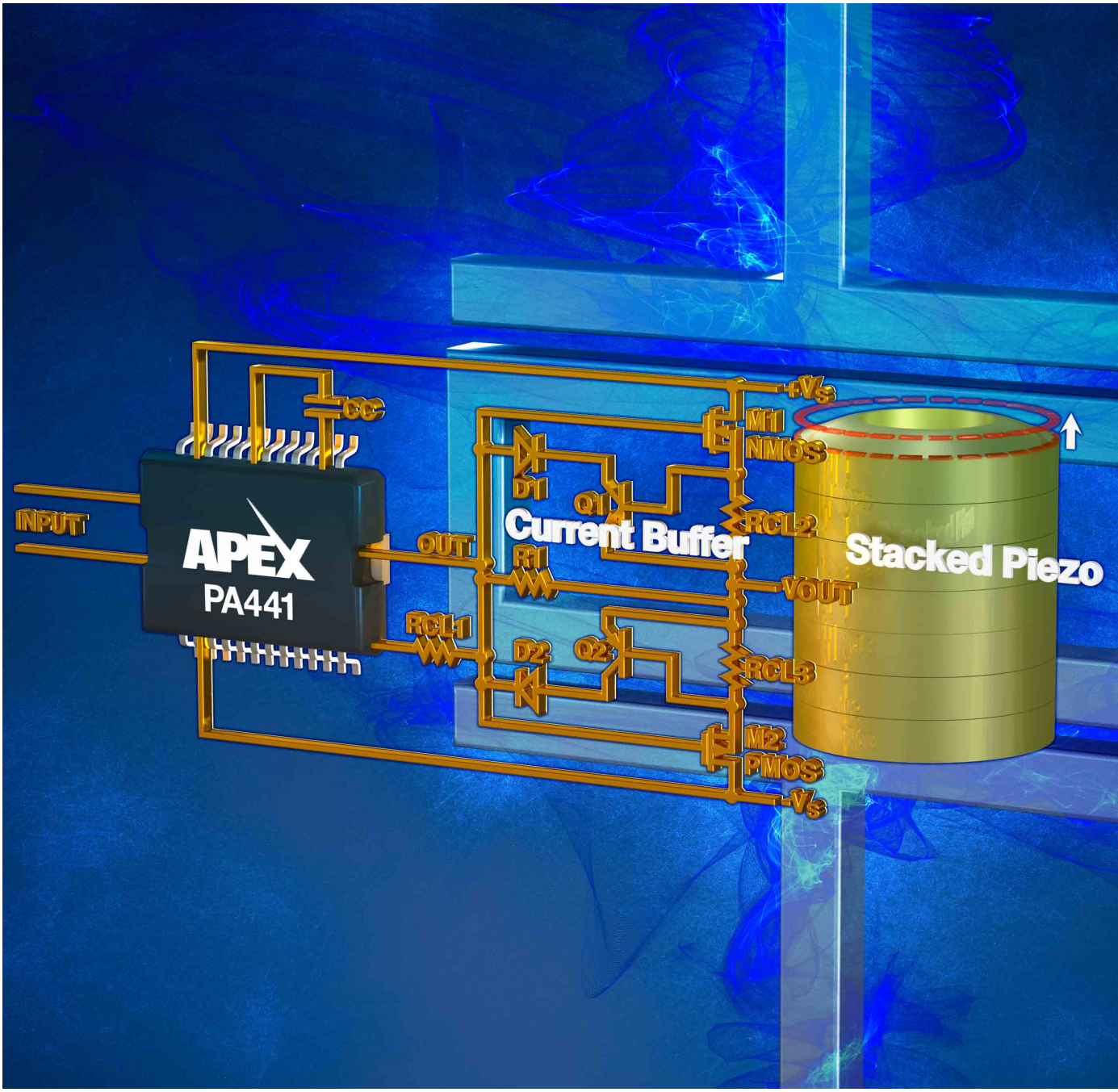

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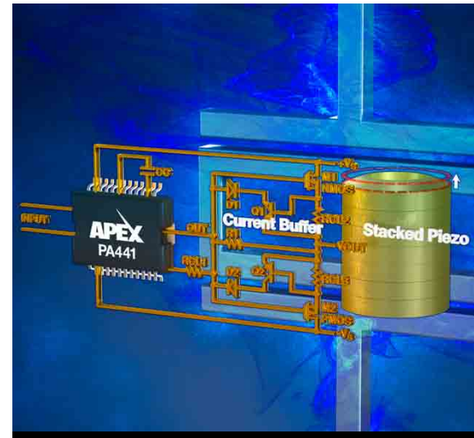

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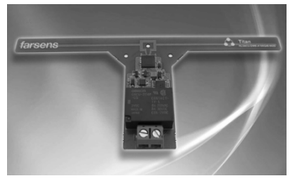

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The new industrial revolution

Industrial technology and processes have been under constant development since the invention of the wheel. From the potter's wheel came the lathe, fire went from cooking to pottery to steam, and precision went from rough measurements based on body parts and other natural comparators to rulers and levels. The tools get better, then the processes get better, than the precision improves, then the cycle begins again.

Sometime that process of change and development is smooth, and sometimes it's precipitous. Usually with every significant advance, there is a disruptive period of challenge and resistance. On rare occasions, that advance is a technology or procedure that the entire industry wants and needs, enabling growth with minimal pain. The migration to intelligent industrial systems is one of those developments.

Smart factories

The drive to smart factories, facilities, and systems has been an evolutionary one, as the primary disruptive aspects of the consumer marketplace are not as influential in the industrial space. Industry has different needs than consumers, so while some aspects of the consumer technology revolution strongly impact industry, they do so in ways differently than they impact consumer markets.

For example, the explosion in personal electronics and the resulting pressures on RF power, battery management, and device miniaturization have only peripherally hit industrial systems in the same manner. Areas such as control systems and portable test devices may shrink and become portable, but the real impact in industrial systems is the ability to insert logic into every powered subsystem in the facility and link them to central command and control through web-based communications infrastructures for enhanced performance and improved reliability.

Better tools

Improved motors and actuators enable more precise processes, improved sensors and microcontrollers enable precise measurement, and improved control systems allow the two to work optimally together for the best result at the highest efficiency. Even the most stubborn manufacturer can see the performance as well as financial advantages to upgrading a facility with smart automation and control solutions today.

This month's issue has some interesting items on industrial systems for your enlightenment. From Linear Technology we have an article on powering low-voltage devices, dealing with properly handling the intermediate bus voltages commonplace in industrial systems where series-connected batteries may be a backup power source and 12V bus architectures tend to be impractical due to distribution losses. We've also got an item from Eaton on optimizing rack power distribution, and something from Exar on programmable power for industrial applications.

Best Regards,

Alix Paultre

Editorial Director, Power Systems Design
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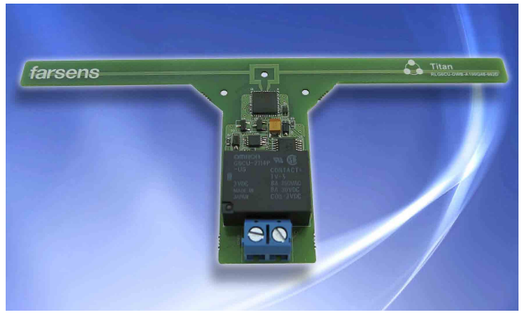
Farsens' TITAN battery-free bistable RFID relay triggers wirelessly

The TITAN from Farsens is a battery free RFID bistable relay tag compatible with commercial EPC C1G2 readers. They can be wirelessly activated and deactivated via their unique ID and the relay keeps its latest status even when the RFID reader is gone.



The TITAN has a 96 bits EPC number, a 32-bit TID and a password protected Kill command. Built in a PCB format, it is available in different sizes. The communication range is up to 1.5 meters and the operating temperatures are from -30°C to +85°C (-22°F to +185°F). These actuator tags are available in a variety of antenna design and sizes, depending on the specific application. It can be encapsulated in an IP67 or IP68 casing for usage in harsh environments.

The fact that the actuator is full passive makes these relays ideal for hardly accessible or restricted areas and those where the use of batteries is not recommended. The TITAN will never require a battery change, saving the costs associated to maintenance. The TITAN tag consists of a ANDY100 IC for energy harvesting and wireless communication, an G6CU-2114P-US relay, an MSP430 microcontroller and start-up circuitry based on the AX6427 IC from Maxim Integrated.

In order to read the EPC of the TAG, commercial EPC C1G2 readers can be used. However, some considerations have to be taken into account. As the tag has a large supply capacitor connected to VDD, the power-up of the system can be slow, lasting several seconds. In order to speed up the charge process, the reader can be configured to send power as continuously as possible. Once the supply capacitor is charged, the TAG will respond with its EPC. From this point on, memory access commands can be used to control the G6CU-2114P-US relay via the SPI bridge.

TITAN tags are used in energy scarce applications where the stored energy is limited and the system/circuit is controlled via a wireless battery-free relay. The circuit can be opened and closed from a commercial RFID reader. The bistable relay allows the system to run so that the limited battery is only switched on during the time the user actually needs it to be running.

Battery-free relays are also a good fit for retrofitting in places where lots of mechanical relays are being manually operated. The fact that each relay is uniquely identified by its ID number makes automation a lot easier and activation/deactivation can easily be implemented in easy-to-use reader software. Mistakes due to human intervention can be reduced to the minimum this way.

Farsens designs and manufactures full passive RFID sensor solutions. Their proprietary UHF RFID IC allows Farsens to develop long-range solutions for asset tracking – via the unique ID – and monitoring – via the attached sensor – without the need of any battery on the tag.

www.farsens.com

Network Convergence Design Strategies

By: George Kairys, Molex

Industrial network convergence necessitates a high degree of integration of hardware and software. Lately we've seen a trend towards extending Ethernet to the plant as the link-layer protocol to one or more of the legacy protocol applications, and even extending Ethernet down to the device level on the machines. Technology advancements have set the stage for convergence, offering network tools to effectively link machine processes, control systems and plant-wide information to the enterprise.

Convergence Strategies

Unlike proprietary protocols commonly used in years past, industrial Ethernet is built on a standard Ethernet structure and Transmission Control Protocol/Internet Protocol (TCP/IP) standards, which allow computers to share resources across a single local area network. TCP/IP also facilitates rapid and accurate file transfer and user communications on both the commercial and industrial sides.

At the plant level, Industrial process control and automation typically require more stringent real-time data transmission rates. Ethernet not only improves transmission speed, it can span distances and accept more devices without performance degradation often seen in prior network technology. Examples of industrial Ethernet platforms include PROFINET, Profibus and EtherNet/IP.

Industrial Ethernet uses twisted pair cable, fiber optics, wireless networks, and may also include Power-over-Ethernet (PoE) where power passes along with the data. In addition to physical layer components, system designers also need to carefully consider network architecture, as well as interoperability, security, and data management, to enable convergence to work efficiently today and allow for future expansion.

The right network architecture can effectively link business management to plant floor controllers such as PLCs, PACs and PCs, which control operation and collect data from machines and devices. However, ubiquitous data transparency can be both empowering and overwhelming, depending on how it is used.

Real-time raw data from the plant typically doesn't reach management level, nor does it need to. Translating raw production data into usable intelligence for management is likely the most challenging hurdle for companies seeking to converge on Ethernet—and here, too, technology is the enabler. To manage plant floor data effectively, various types of executive dashboards and other business intelligence and analysis software can help to filter data and focus on key metrics and performance indicators and other information needed for high-level decision-making.

Benefits of Convergence

The benefits of plant and enterprise convergence depend largely on the network configuration and the strategies driving a company's decision to integrate these two sectors. Significant business and operational advantages include improved efficiency and resource management, faster data transmission, enterprise-wide increased business intelligence, improved equipment monitoring and control, and the ability to meet secure real-time data traffic requirements.

www.molex.com

Life to Return to the Power Supply Industry in 2014

By: Jonathon Eykyn, IHS Technology

The global market for power supplies crashed in 2012 as economic uncertainties led to low consumer demand and the postponement of large industrial projects. Whilst 2013 bought growth, it was limited to a few markets and the overall market grew by just 2.4%. However, the outlook for the global power supply market is much brighter in 2014 with the market growth projected at 4.4%.

Unlike 2013, this growth is projected to be across the board with strong growth forecast in nearly all applications. This growth will be driven by a couple of key factors. Firstly, a forecast uplift in end-equipment demand in the traditional power supply markets of telecommunications and industrial. There has been a higher business confidence across many industries despite some less than favorable economic conditions leading to postponed projects being restarted and new projects green-lighted.

The second factor is the meteoric growth of the emerging applications for power supplies. Demand for power supplies used in LED lighting and tablet PCs is projected to grow by more than 40% in terms of units shipped.

The data communications sector is also set to grow strongly in 2014 with revenues for power supplies for servers and storage devices projected to increase by 4%. This is more than double the growth for 2013 and is driven by the need for continual refreshment of IT systems and the growth of cloud computing and associated data-centers.

This growth in the market will also be spread across all three major regions. Asia continues to grow the fasted with revenues projected to grow by almost 5% in 2014. Revenue growth for both the Americas and the EMEA regions is forecast to more than triple after a weak 2012 where growth was estimated at just over 1% for both regions. However, it is not a perfect outlook for the industry. The majority of the growth by application and region is predicted to be driven by both the AC-DC commodity and non-commodity markets.

Opportunities in the non-commodity AC-DC power supply market by power supply type in 2014 are predicted largely to mirror the demand by application. Strongest growth is forecast for power adapters and chargers at 9.6% and open-frame/enclosed power supplies at 9.3%, owing to their use in LED lighting and telecommunication applications. Whereas the market for DIN Rail non-commodity AC-DC power supplies, of which the majority are used in industrial applications, is forecast to grow by just 2.4%.

The DC-DC converter market was the worst hit in 2012 and the market remained almost flat in 2013. It is forecast that overall revenue growth in the DC-DC market in 2014 will be at around 1% although unit shipments will grow by almost 4%. Part of the reason for the slower recovery of the DC-DC converter market is that many of the 'hot' applications that are helping to drive overall market growth at the moment such as LED lighting and tablets are predominately an AC-DC opportunity. The longer-term forecast for DC-DC converters is slightly better, with an average annual growth rate of 2% for the 2014-2017 period but this is still behind the rest of the global power supply market.

www.ihs.com

Power supply failure survey – Part II

By: Dr. Ray Ridley, President, Ridley Engineering

In this second article about power supply failures, the capacitors are examined for their contribution to the failure rate. The causes of failure for different types of capacitors are discussed. In the last part of this article, the question was asked of group members "Why do power supplies fail?" and the results of the survey are repeated in **Figure 1** below.

The survey group saw semiconductors as the main cause of failures, and this was discussed in the last article of this series. Second on the list are capacitors. In this article, we will look at the issues that cause capacitor failures.

Power Capacitor Failures

While semiconductors topped the list of failures, they are usually very well documented components. Avoiding semiconductor failure is usually a matter of keeping voltage, current, and thermal stresses below the published limits in the datasheets. Capacitors have many different failure mechanisms. Overvoltage will cause failure for some types of capacitor, but the current rating is greatly variable. Current-carrying capability is dependent upon the type of capacitor, lifetime required, package, environment, and many other factors. Designing a capacitor into your power system and maintaining reliability over the long term is a challenging task in many applications. It is important to devote proper time and care to the selection of parts.

Figure 2 shows the results for the causes of capacitor failures. These are summarized as follows:

Thermal Stress: 50% Top of the list, perhaps surprisingly, is thermal stress. Many designers have learned over years of experience that capacitors will fail if kept too hot for too long. Since capacitors are usually in the vicinity of hot semiconductors, they are frequently exposed to temperatures well in excess of ambient. In optimizing high-frequency board layout, it is important to keep current loops small and tight. This implies that the capacitors must be kept as close as possible to the power

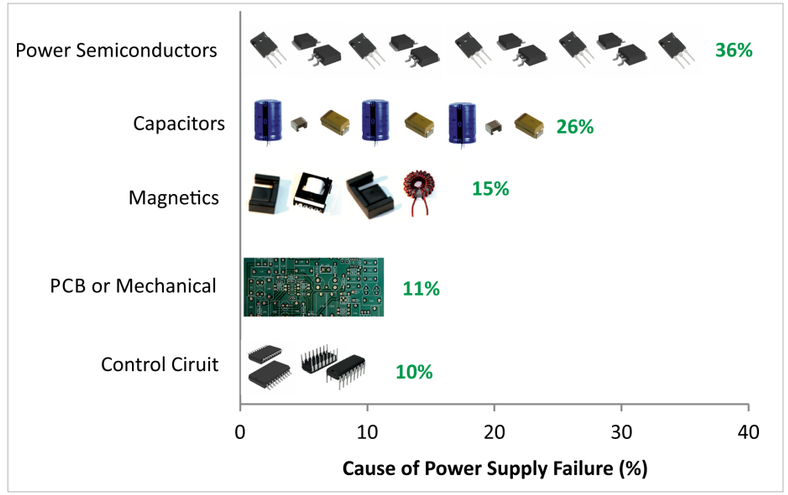


Figure 1: Survey Results for the Cause of Power Supply Failures

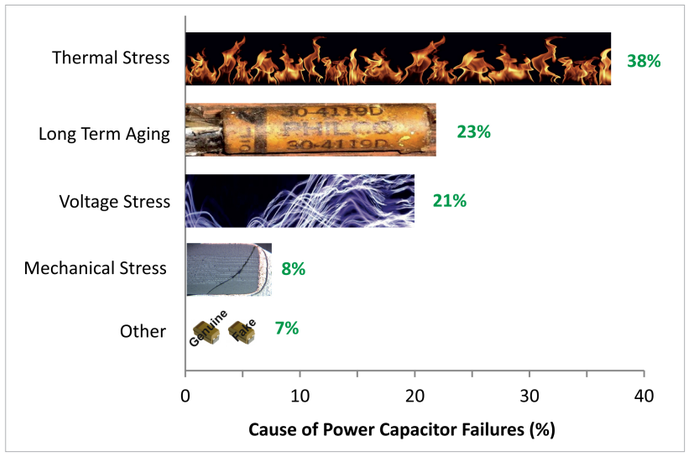


Figure 2: Survey Results for Causes of Capacitor Failures

switches. This also exacerbates the thermal problem.

Long-Term Aging: 23% Second in the list is long-term aging. This comes from experience with predominantly electrolytic capacitors which dry out over time, especially when placed in a hot environment.

Voltage Stress: 21% Depending upon the type of capacitor, they can be relatively tolerant of overvoltage events. Once again, electrolytics have dominated our industry until recently, and they usually come with a surge rating that lets you briefly exceed the voltage rating. Some of them will even recover after a failure. Other capacitor types are usually much less tolerant of overvoltage.

Mechanical Stress: 8% Much lower on the list is mechanical stress. This can apply to any type of capacitor.

Other: 7% A multitude of reasons make up the last category. Included in here is the same problem seen with semiconductors – counterfeit parts.

Power Capacitor Types

To understand the statistics for the failure mechanisms of **Figure 2**, it is important to split the capacitor failure problem into the different types of capacitor technology. A second part of the capacitor failure survey was run to ask which type of capacitors are most likely to fail. The results of this are shown in **Figure 3**.

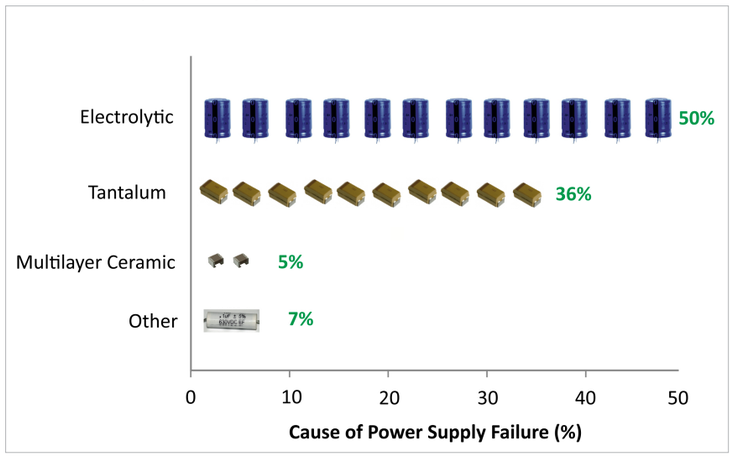


Figure 3: Survey Results for Type of Capacitor Most Likely to Fail

Electrolytics: 50% Electrolytics are used more than any other type of capacitor, so not surprisingly they experience the most failures. The biggest problem with electrolytics is maintaining the electrolyte inside the component. Great advances have been made in technology to provide longer lifetimes and better seals. Ultimately, however, high temperatures inside the capacitor due to ambient temperature or high currents will cause loss of electrolyte over time. When enough loss has occurred, the ESR of the capacitor rises, temperatures climb further, and the part will eventually fail.

Tantalums: 36% Tantalum capacitors are an interesting case study in the power supply industry. Most engineers in our industry have heard the expression that you "need to let the smoke out" of power components—a humorous reference to failed components. One of the LinkedIn group attendees made the wry observation that with tantalum capacitors, you need to "let the fire out". This refers to the rather alarming fact that the failure of a tantalum can be a very dramatic event that will incinerate other components and board material in the vicinity of the failed tantalum part.

What is even more alarming is that most designers feel that tantalums should be heavily voltage derated, as much as 50%, if the parts are to be reliable. Some manufacturers even go as far as derating the nameplate rating deliberately by this amount in order to get ruggedness. Other manufacturers will suggest putting large current-limiting resistors in series with the capacitors, which of course defeats the purpose of using them in a power environment in the first place. Despite this, tantalums continue to be used since they provide low ESR without the problem of electrolyte loss. They provide high values of capacitance that multilayer ceramics do not yet match.

You should be very careful if using tantalums for the first time. A 50% voltage derating is definitely encouraged, and you might want to check with experienced engineers to find out which manufacturers make the most rugged parts. The vagueness of exactly how to use and derate tantalums safely is something that probably would not be tolerated in any other type of component, and certainly not in semiconductors. The data sheets simply do not provide enough information to avoid all the hazards.

Multilayer Ceramics: 5% There are two main reasons for failure of MLC capacitors. First, is overvoltage, for which these capacitors have no tolerance. Always stay below the stated voltage rating. Large MLC capacitors are used frequently these days in high power applications. The big packages suffer from the problem of mechanical stress since they are not flexible. Special mounting techniques have been introduced by manufacturers to relieve stress on the large parts. Anything above a 1210 package must be mechanically designed for its proper mechanical and thermal stresses.

Other Types: 7% There are many other types of capacitors, usually used in high-power or specialist applications that can lead to various types of failure modes. Mechanical stress is often high on the list of causes.

Summary

The survey results in this article highlight the major causes of capacitor failures in switching power supplies. There are no perfect capacitors. Tantalum, electrolytic, and multilayer ceramic capacitors all have their own unique ways of breaking down. Each of them must be carefully considered when they are used in power environments.

Much research continues to be done by capacitor vendors to improve their parts, but failures still continue to be a significant problem. There are many other considerations to capacitor application not mentioned in this article, and it is recommended that you study datasheets and application notes very carefully during your design.

www.ridleyengineering.com

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Boosting output in high-voltage op-amps with a current buffer

Creating a composite op-amp brings its own set of challenges

By: Joe Kyriakakis, Apex Microtechnology

Delivering more than 200mA of output current can be a serious challenge for many high-voltage operational amplifiers. However, when it comes to high-voltage applications requiring as much as 1A of current, it is possible to meet this spec by pairing a current buffer with the op amp. What the current buffer brings to this arrangement is approximate unity voltage gain when it's placed between the output of the high voltage op amp and the load. This means the current buffer is included in the feedback loop of the op amp to create a composite op amp.

But creating such a composite op amp does come with its own set of design challenges. These challenges begin with the current buffer's output stage bias circuit. Usually a Class B output stage is adequate for some applications, but such a solution has a characteristic crossover distortion as the low-side device output current transitions to the high-side device. The preferred scenario is to use a Class AB output stage as the crossover distortion is much lower and the feedback loop remains closed during the transition. But setting the quiescent current of the Class AB output stage is difficult because of output device variations and sensitivities.

The current buffer design approach that we will explore here makes it possible to avoid many of the design difficulties related to output stage biasing by incorporating a depletion mode MOSFET as the high side driver. The benefits of this circuit topology are due to the MOSFET's ability to provide the bias current by using it as a current source. The depletion-mode MOSFET then serves as both the bias current generator and the high side driver.

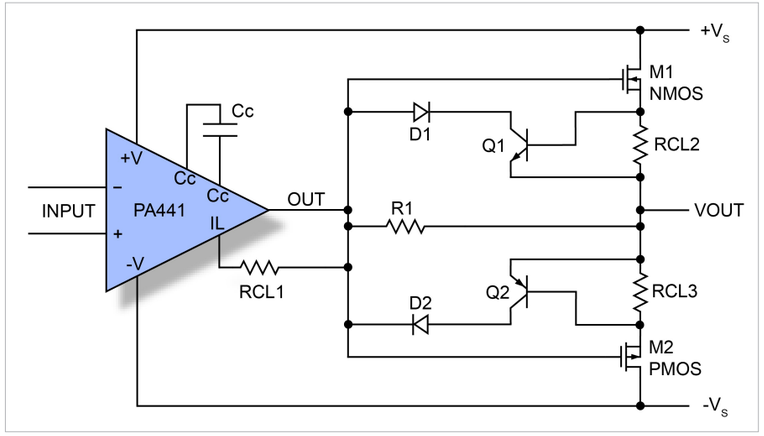


Figure 1: Class B circuit showing one common method of implementing a current buffer

Building A Better Buffer

The Class B circuit shown in **Figure 1** illustrates one common method of implementing a current buffer. In this circuit diagram, the resistor R1 provides

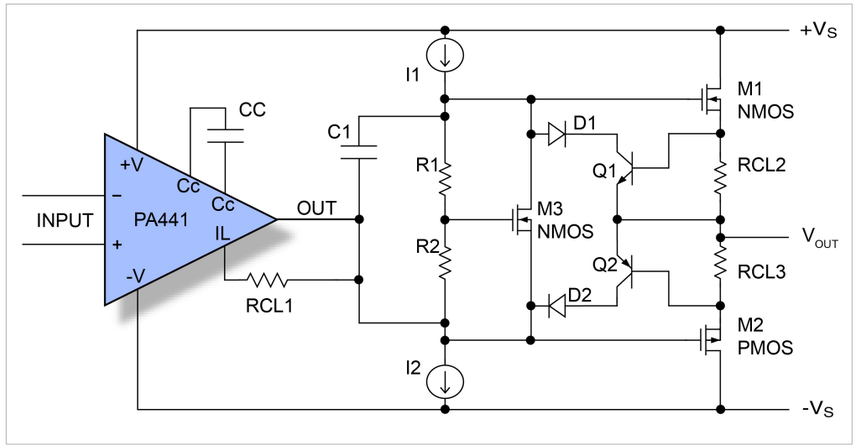


Figure 2: Conventional circuit topology of a Class AB current buffer output stage

a current path to the load from the high voltage op amp (PA441) and is set to limit the maximum gate voltage of the MOSFETs M1 and M2 to 10V. The resistor RCL1 is used to set the current limit value of the PA441 so that the current in R1 creates a voltage drop of 10V.

The op amp current limit value should be set as low as possible to minimize the amount of power dissipation that the op amp is forced to bear. Resistors RCL2 and RCL3 are tasked with providing a level of protection for the output devices by serving to current-limit the output MOSFETs.

The output current flows through RCL2 and RCL3, creating a voltage across the base to the emitter of Q1 and Q2. Once this voltage reaches approximately 0.7V, the transistors Q1 and Q2 begin conducting current to the load, thus clamping the gate drive voltage at M1 and M2 as

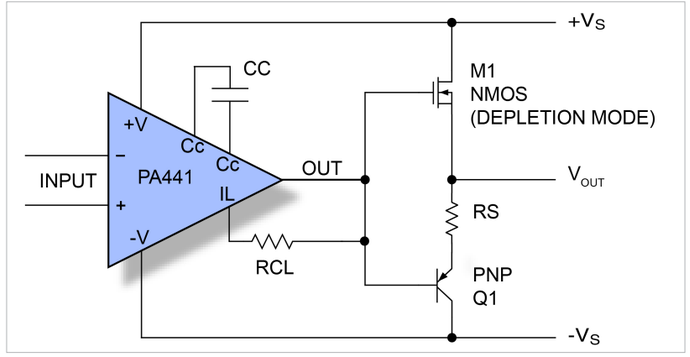


Figure 3: A simplified conceptual circuit diagram of an alternative Class AB topology

the PA441 enters current-limit mode.

The conventional circuit topology of a Class AB current buffer output stage is illustrated in **Figure 2**. This is a simplified schematic diagram using a VGS multiplier composed of M3, R1 and R2 to set the required voltage at the gates of M1 and M2. This provides the desired quiescent current through the output devices M1 and M2. Constant current sources I1 and I2 supply the required current to the VGS multiplier. The transistors Q1 and Q2 are used for current limiting the output MOSFETs, as described in the previous Class B stage example.

This Class AB design approach is much more complex and problematic than the Class B stage design, therefore one must ensure that all of the proper elements are in place. First, additional components are required in order to implement the current sources I1 and I2, and it is important to note that the voltage swing will be less than the voltage swing of the PA441 because of the drive requirements of the output MOSFETs.

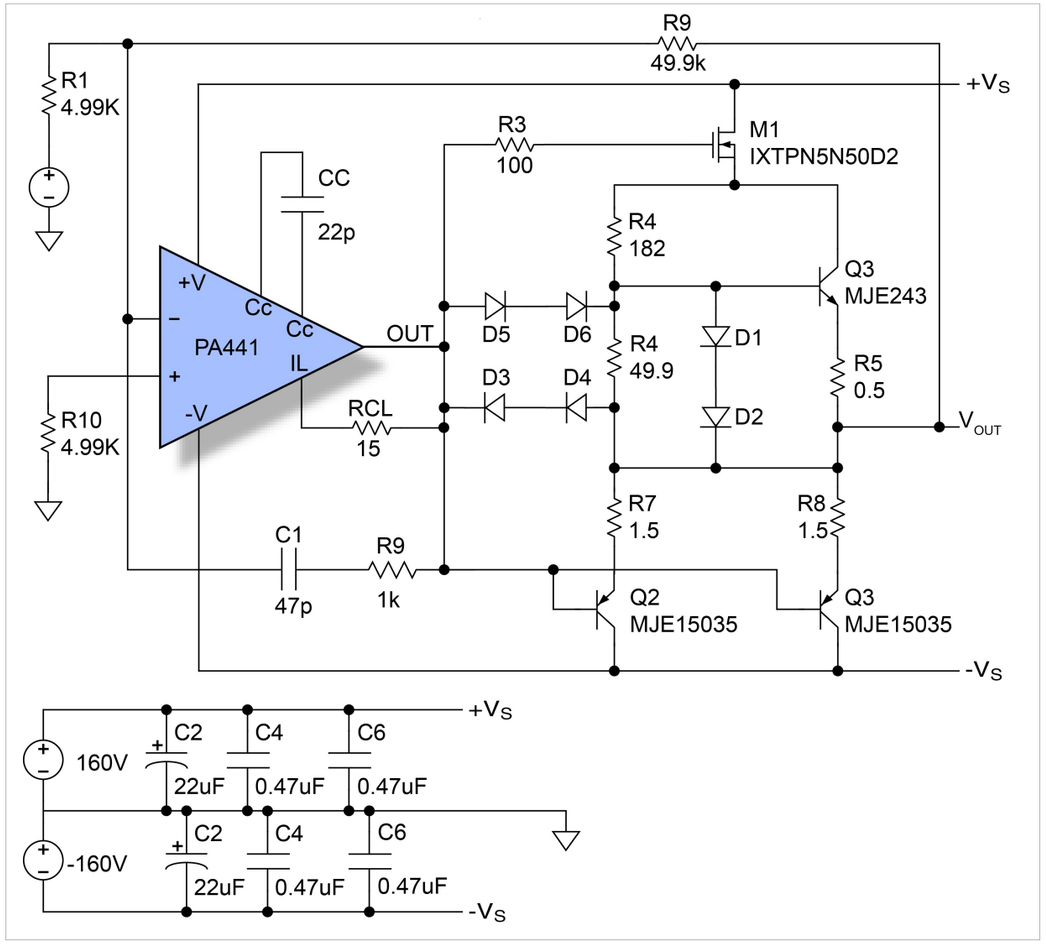


Figure 4: A prototype of the circuit schematic

In addition, setting the quiescent current through M1 and M2 is difficult because of the high sensitivity between VGS and ID. The VGS multiplier, consisting of M3, R1 and R2, must be individually adjusted for every unit. To prevent thermal runaway, the circuit relies on device matching and tight thermal coupling between M1, M2 and M3. Taking these factors into account, along with temperature instability and sensitivity in setting the quiescent current, the actual implementation of this circuit topology is much more challenging than that of the Class B buffer version.

There Is An Alternative

Let's take a look at a simplified conceptual circuit diagram of an alternative Class AB topology, as shown in **Figure 3**. One of the benefits to this approach is that the circuit functions in a self-biasing mode, and does not require the current sources and VGS multiplier of a conventional Class AB stage. In this example, to demonstrate the mechanism for establishing the flow of quiescent current, we will assume that the output voltage is at zero volts, while the base of Q1 must be approximately -0.7V. IN this diagram the gate

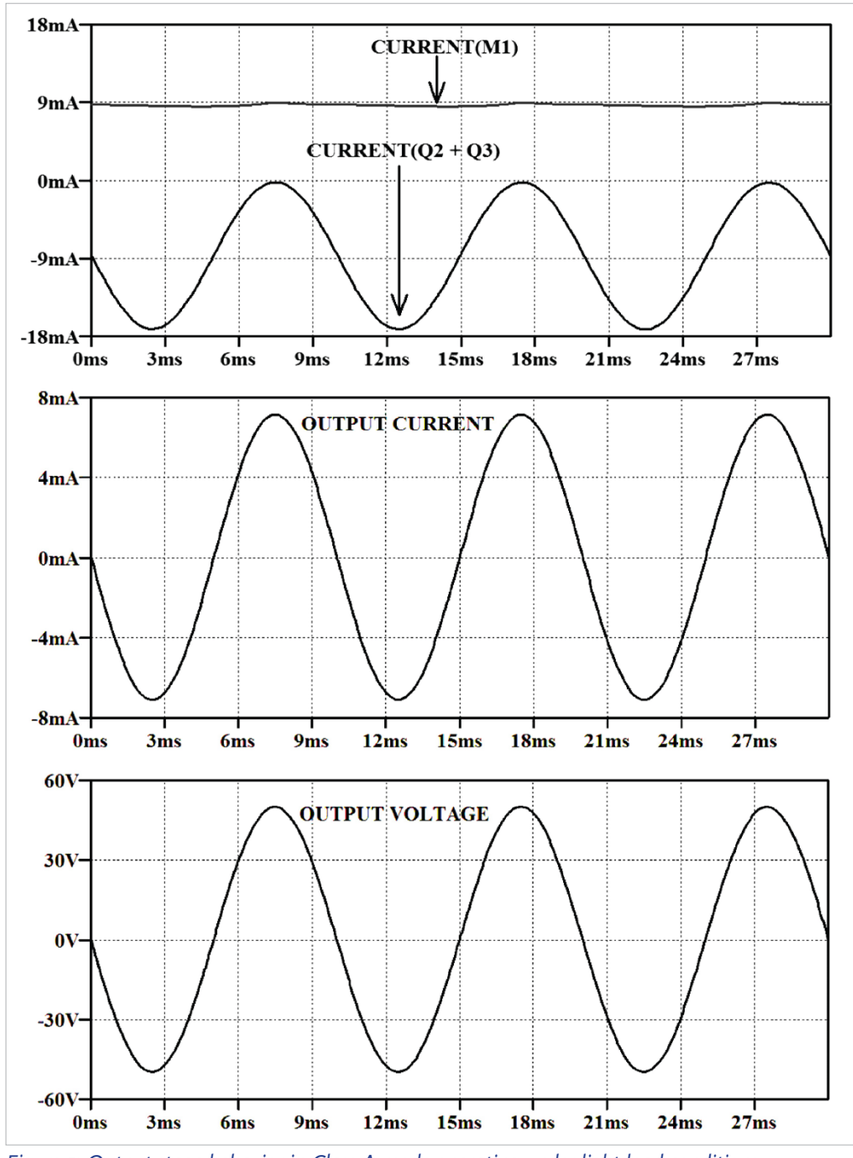


Figure 5: Output stage behavior in Class A mode operating under light load conditions

of M1 is also at -0.7V, forcing the MOSFET to conduct. The resistor RS is selected to adjust the quiescent current to the desired value.

The actual prototype of this circuit schematic is shown in **Figure 4**. The depletion mode MOSFET M1 is biased to provide the quiescent current for the output stage. Resistors R4 and R5 are selected to establish the operating current of M1. The bipolar transistor Q1 acts as a Vbe multiplier to maintain the desired VGS for M1 as the demand for load current increases. That means the Q1 essentially conducts the output current sourced by M1 by bypassing R4 and R5. The bipolar transistors Q2 and Q3 are biased by the quiescent current and provide the load current during the negative half cycle.

In this circuit, two PNP transistors are necessary to accommodate the required power dissipation. The maximum rated power dissipation of each PNP transistor is 50W. The current limit function is implemented through the addition of diodes D1 through D6. The diodes used

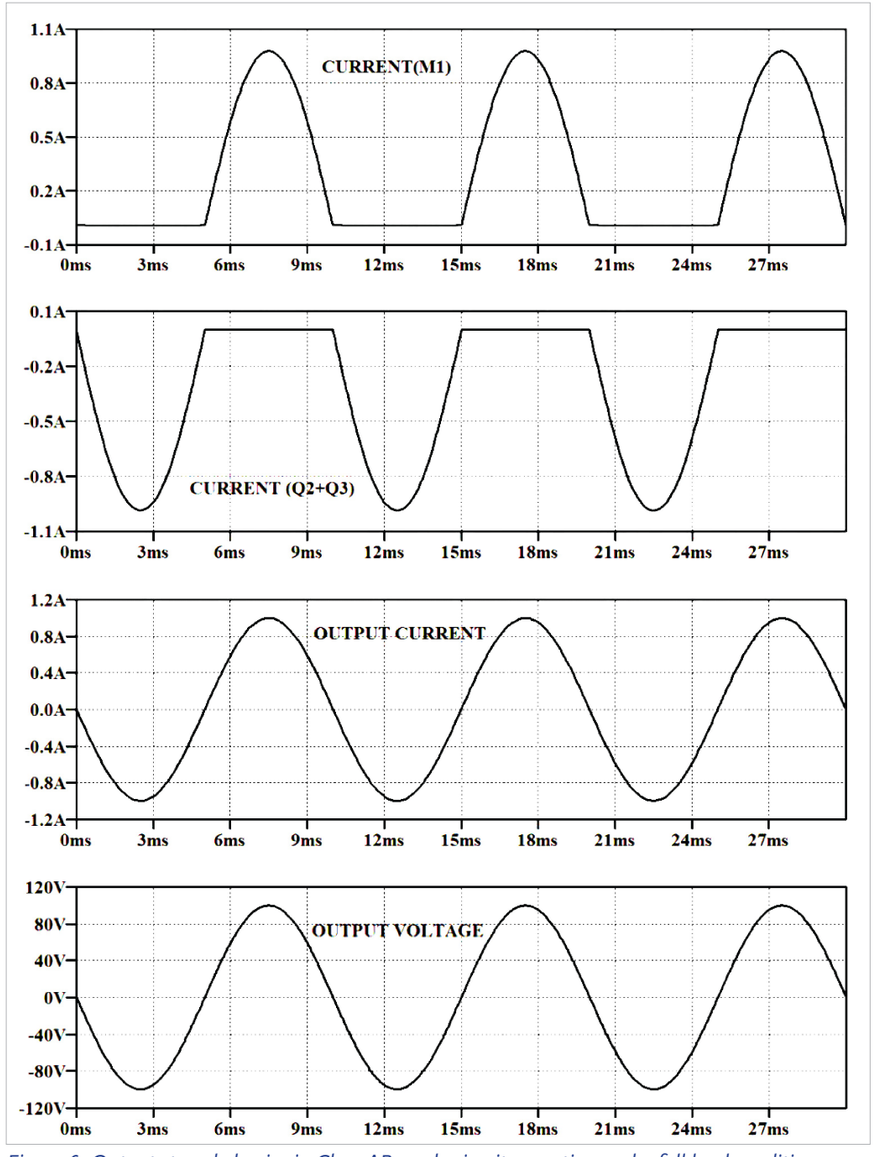
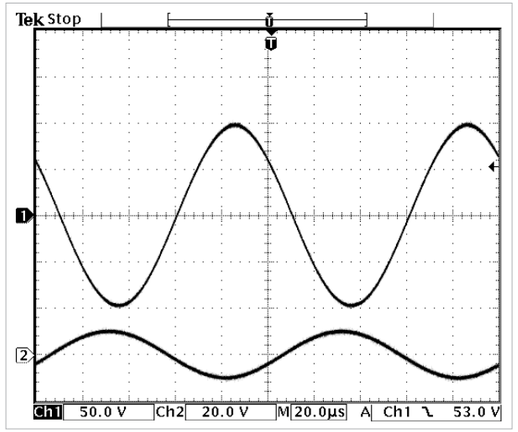


Figure 6: Output stage behavior in Class AB mode circuit operation under full load conditions

in the prototype are 1N4148, but any equivalent small signal switching diode such as 1N914 is suitable. As the output current approaches approximately 1.2A, the voltage across R6 in series with the Vbe of Q1, forces Q1 to limit the output current. Since the diodes D1 and D2 are conducting, a constant current through Q1 is established. In this example the maximum output current delivered by the PA441 is set to approximately 40mA by Rcl.

The diodes D5 and D6 clamp the output of the PA441 to limit the VGS of M1 and still provide sufficient gate drive voltage to support the load current. When the current limit function is engaged, the output current of the PA441 flows through D1, D2, D5 and D6. The current limiting for the negative half cycle functions by forcing the output current from the PA441 through diodes D3 and D4, which establishes a constant current of approximately 1.2A through Q2 and Q3.

This alternative topology does offer several advantages including a high output voltage



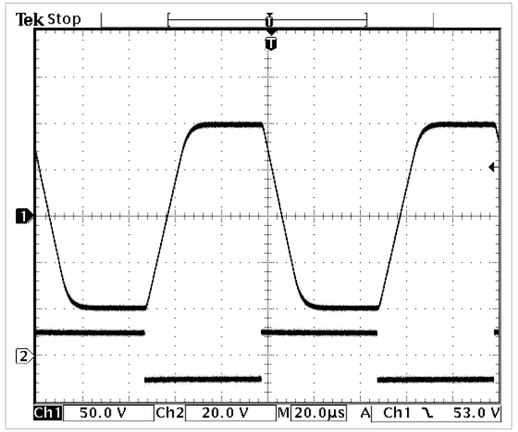
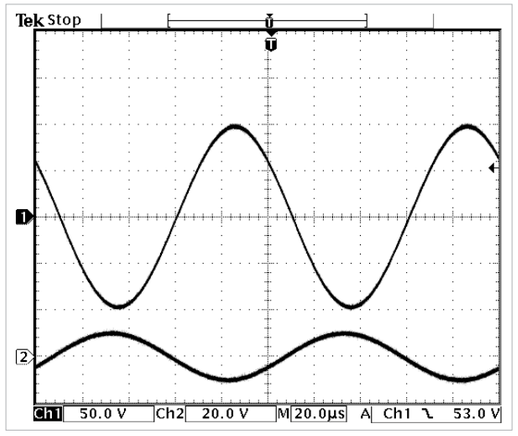


Figure 7: Oscilloscope screen shots taken during bench testing



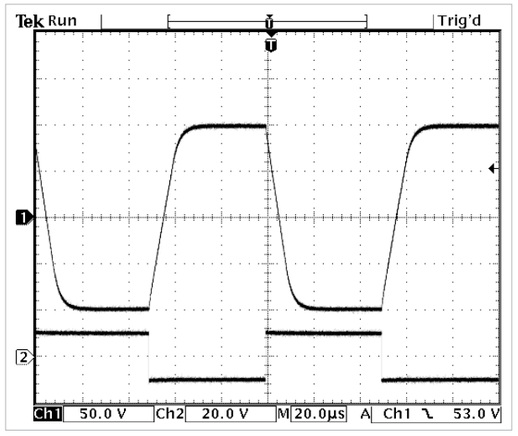
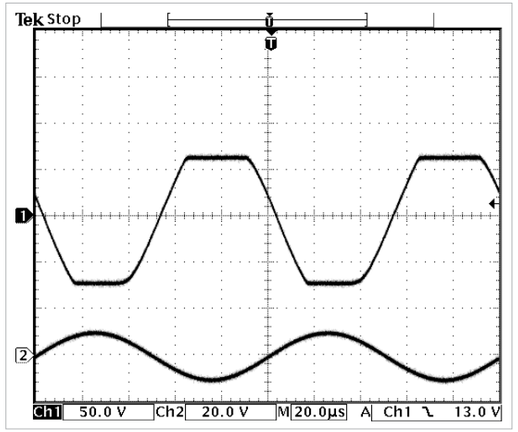


Figure 8: Oscilloscope screen shots taken during bench testing

swing resulting from a limited voltage drop as compared to the typical enhancement mode Class AB output stage; the simplicity of setting quiescent current; and a big plus, a reduced component count.

The best way to demonstrate and underscore just how robust this circuit can be is to look at it in simulation. Let's start by looking at **Figure 5**, which depicts actual simulation plots that demonstrate the circuit is operating in Class A mode under light load conditions. The output voltage is 100V p-p across a load resistor of approximately 7KΩ, and quiescent current is measured at approximately 9mA. Since the current through the transistors M1, Q2 and Q3 is always greater than zero for the entire cycle, the output stage is proven to be clearly operating in Class A mode.

Taking a look at **Figure 6**, we see it demonstrates the current behavior of the same circuit, but now in Class AB mode. Using full load conditions of 100Ω, this series of simulation plots illustrate how current is able to increase with this circuit and that the output stage behavior is in Class AB operation. In this scenario, the power supply voltage is ±160V and the output voltage is 200V p-p.



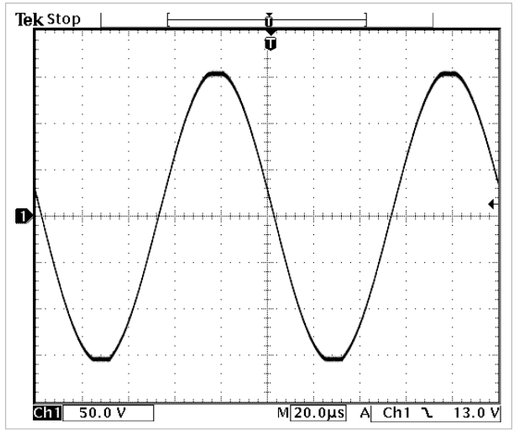


Figure 9: Oscilloscope screen shots taken during bench testing

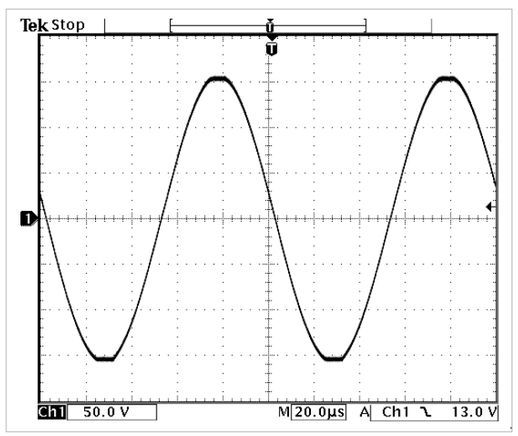


Figure 10: Oscilloscope screen shots taken during bench testing

At this point we should perform some bench testing to see how well this circuit responds in some additional areas of key performance parameters. **Figures 7, 8, 9 and 10** are oscilloscope screen shots taken during a series of real-time test scenarios. The circuit is using a power supply voltage set at ±160V and a signal frequency set at 10KHz with the amplifier configured for an inverting gain of 10. On the screen shots, the "1" indicates channel one, which is the output voltage, and the number "2" is the input voltage via channel two.

The waveforms in **Figure 7** illustrate that with a capacitive load of 0.123µF, the circuit is stable with virtually no distortion. Along the bottom of each screen shot, the voltage supply and slew rate are noted. In **Figure 8**, the circuit is shown now to be operating with a resistive load of 100Ω and again confirms circuit stability.

Figures 9 and 10 test the circuit's current limit levels and voltage swing clipping. Without the enhancement of the AB current buffer, the PA441 would typically current limit just above 60mA, but **Figure 9** shows improvement to slightly above 1A. **Figure 10** illustrates the circuit's higher voltage swing clipping, now just above 150V. So the conclusion here is that the arrangement to pair the amplifier with the new buffer does create a circuit that can deliver performance that can scale up as the output current is increased.

In summary, the circuit we created for our example illustrates that by pairing an op amp with a current buffer, it is possible for the resulting composite amplifier to operate in Class AB mode. Granted, this is only a only a basic approach to achieving Class AB, but certainly this concept can be embellished and expanded to achieve even greater performance.

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Focused ion-beam circuit edit improves power device design

Benefits are especially significant at nanoscale geometries

By: Taqi Mohiuddin, EAG

Designers of power control devices and those that combine control with power FET functionality are finding that FIB circuit edit techniques proven at older process nodes are delivering even greater benefits when used at advanced technology nodes. It is also expected that FIB circuit edit techniques will be important as many power devices move to silicon carbide (SiC), gallium nitride (GaN) and other wide bandgap materials. FIB circuit edit can help designers reduce costs while optimizing performance, increasing functionality, mitigating risk and accelerating development cycles.

FIB systems used for circuit edit enable designers to cut traces or add metal connections inside a chip (see **Figure 1**). These edits can be made quickly and easily, at far lower cost than that required for a typical new wafer lot. Using the latest equipment, it is possible to edit circuits fabricated with 28 nanometer (nm) and smaller technology nodes, including devices that feature multiple-layer metal stacks and those produced in flip chip and other advanced chip scale form factors.

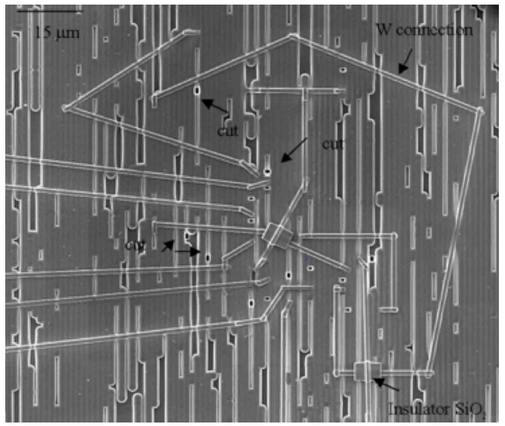

Figure 1: Front-side FIB circuit edit with multiple connections and cuts.

The FIB tool is coupled to a CAD navigation system that enables it to locate each area where edits will be made. A finely focused gallium (Ga+) ion beam with nanoscale resolution is used to image, etch and deposit materials on a device, with an extremely high level of precision. This enables designers to cut and connect circuitry within the live device, and to create probe points for electrical test. The high-energy Ga+ beam can mill through conductors, and uses various types of gases to either improve the precision of the milling process, or the ability to deposit conductive and dielectric materials.

There are numerous applications for FIB circuit edit at every commercially available node. The process can be used to verify design change on the tester, and to validate design change at the system board level.

Typical applications include:

- Debugging and optimizing devices in production
- Exploring and validating design changes
- Prototyping new devices without costly and time-consuming mask set fabrication
- Scaling fixes, so that a fix can be duplicated on a handful or tens of devices that can be provided to internal test, validation, and qualification teams and even to customers as samples
- Accelerating time to market, and/or avoiding late delivery and associated penalties

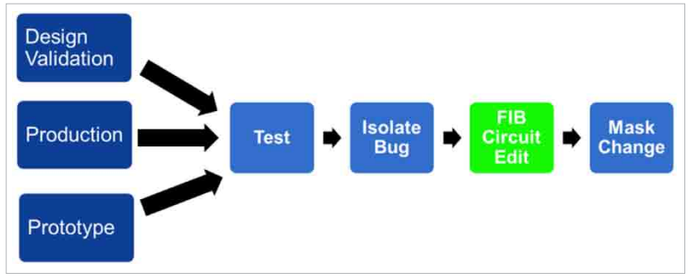

Figure 2: FIB circuit edit process flow.

The FIB circuit edit process can be implemented both at the simulation stage and later during de-bug to optimize success rates during the IC design process (see **Figure 2**).

Most current control products are fabricated using traditional silicon technology, and FIB circuit edit is performed in much the same way with these devices as it is with any other anlog or digital circuit. In the future, there is a strong possibility that drivers will move to wide bandgap materials. FIB circuit edit should offer benefits for these devices, as well. SiC, GaN and other wide bandgap semiconductor materials enable power semiconductor devices to withstand high voltages and temperatures, while providing higher frequency response, increased current density and faster switching speeds. At the same time, however, they present complex challenges related to design and characterization, process monitoring and reliability.

Challenges become even more difficult at advanced process nodes. It is harder to find and fix bugs, and mask costs are significantly higher. Testing becomes more tedious, simulations take longer, and in the case of many designs, it is impossible to achieve 100 percent verification. Additionally, there may not be perfect simulation models for extremely complex designs, and packaging can introduce stresses for sensitive devices. These challenges can be alleviated through the use of FIB circuit edit, which can be used to debug and validate fixes, and to explore design optimization changes before committing to a full mask spin.

Tips and Techniques

While some believe that FIB circuit edit only works well at 90nm and 65nm process nodes, this is inaccurate. Tool and methodology advances have enabled FIB circuit edit to be used for more precise beam guidance. Today's systems also can operate in smaller areas, perform more intricate operations on both the back and front sides of the device, and handle copper layers.

Advances in operator skill have been particularly important. The FIB circuit edit process is not completely automated; for example, endpoint detection continues to require a high level of skill in order to ensure when selected layers of interest have been successfully etched, especially at smaller geometries and during the most challenging FIB operations.

Also important is operator knowledge about IC circuitry and process technology, ion milling patterns, and the basics of FIB tool usage. This can be difficult to achieve within an in-house operation. Larger semiconductor companies will often augment in-house circuit edit resources with external service labs. Small- and mid-sized companies generally can't afford a $1 million FIB tool and wouldn't likely have the staff to operate it, so they tend to go directly to external labs, which can support basic electrical design characterization or verification of redesign parameters, and have a full range of debug tools for solving difficult logic failures and other development anomalies.

Key prerequisites for FIB circuit edit success – especially at advanced nodes -- include a minimum tool resolution (or

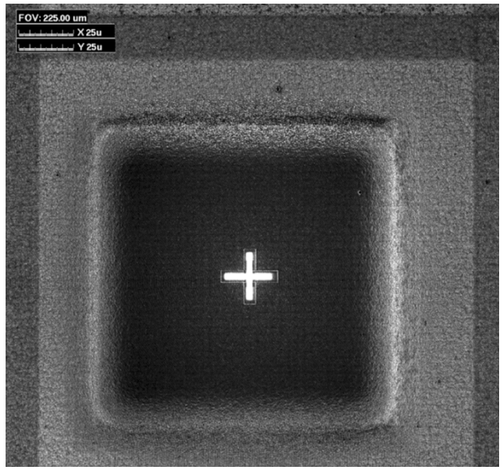

Figure 3: High-resolution trenching enables edits at advanced nodes. [Image courtesy of FIB International Inc.]

aspect ratio) of .1um, and a trenching approach that supports a finer resolution in order to make these edits. Today's equipment can create a hole as small as 0.1x0.1um with an aspect ratio of 1/20. In the case of most 20nm and 28nm designs, it is impossible to make a small enough hole to reach the target. The solution is specialized FIB techniques that shrink the aspect ratio in order to gain access to the target. This also requires the ability to smoothly remove dummy metal above the target metal layer (which, in turn, requires deep and extensive knowledge of IC circuitry and processes, FIB tools and ion milling patterns).

Another important capability is backside and frontside editing. Despite a misperception that flipchip FIB circuit edit can only be performed from the top of a device, the reality is that backside edit is, indeed, possible -- and frequently the most effective approach. Backside edit may be required either because of the substrate material used in flipchip packaging, or because of the increased number of metal circuit layers in today's ICs, which makes it harder to reach a lower layer when editing from the top. **Figure 3** shows a typical back-side FIB circuit edit in which a probe pad is formed for micro probing.

A third area that should be considered is the ability to handle copper layers. Most 28nm and 20nm devices are copper devices that feature a crystal structure. The engineer must have experience in using special methods that ensure metal is removed smoothly with a very high level of quality. Also, accurate beam positioning is more challenging for copper metal devices due to the non-visibility of the circuit patterns. This is also important for aluminum metal devices if there are no unique patterns to recognize on the top level.

Beyond basic FIB circuit-edit expertise it is also important that designers have access to companion failure analysis and test tools, expertise and capabilities. Most devices must ultimately be packaged, and there should be a smooth transition to de-capping or de-lidding the devices and performing micro-probing and other de-bugging tests on FIB-edited parts.

Finally, designers should consider the expertise that is required in the area of front-end processes and materials. Semiconductor advanced technology nodes create challenges related not only to nano-scale geometries, but also new front-end materials. It can be extremely valuable when the FIB circuit edit function is part of a larger lab environment with significant front-end process understanding and materials expertise.

The design verification and validation of power devices will continue to grow more difficult as the industry moves to smaller nano-scale geometries and wide-bandgap materials. FIB circuit edit is becoming increasingly important for improving design success. Thanks to advances in tools, techniques and operator skill, FIB circuit edit can be used to explore design optimization opportunities, and to debug and validate fixes, without the cost or time required for a full mask spin.

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Using the right power semiconductors can increase your power density

The solution must also address regulatory issues while serving system requirements

By: Jifeng Qin, International Rectifier

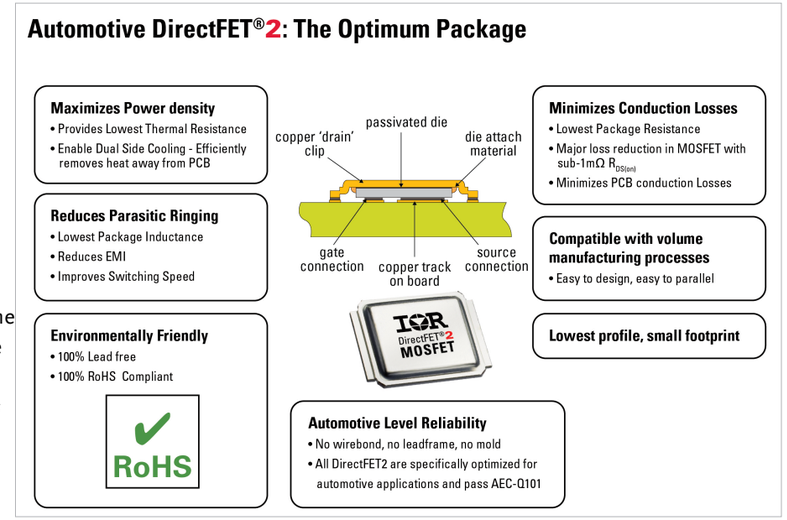

Figure 1: Key Benefits of Automotive DirectFET2

The steady increase in vehicle production, along with increased demand for car electrification is a worldwide phenomena. It is expected that global vehicle production will grow at around 4% over the rest of the decade. On the other hand, mainly driven by stringent fuel economy requirement and cross-functional new features, the power semiconductor usage actually grows at two-digit rate. The dilemma soon rises up between the increased power requirement and limited space in the automotive system. There are fundamental physical limits to how much energy that can be extracted from a given volume/mass of the energy resources (so called "power density"), and this is the key area that many car manufactures are working on nowadays to improve the performance.

Power density is indeed an important phrase in automotive electronics industry. For example, the high power density battery technology is critically needed to ensure the hybrid and electrical car development because nowadays the power density of battery still has significant gap versus gasoline. Similarly, take the steering system as another example, the hydraulic driven steering system always offer good power density compared with an electrical driven motor system, which means replacing the traditional solutions with electric drives requires advance system design with highly efficiency and compact power electronics, especially discrete semiconductor component.

Silicon technology is pretty matured nowadays, and semiconductor industry relies on

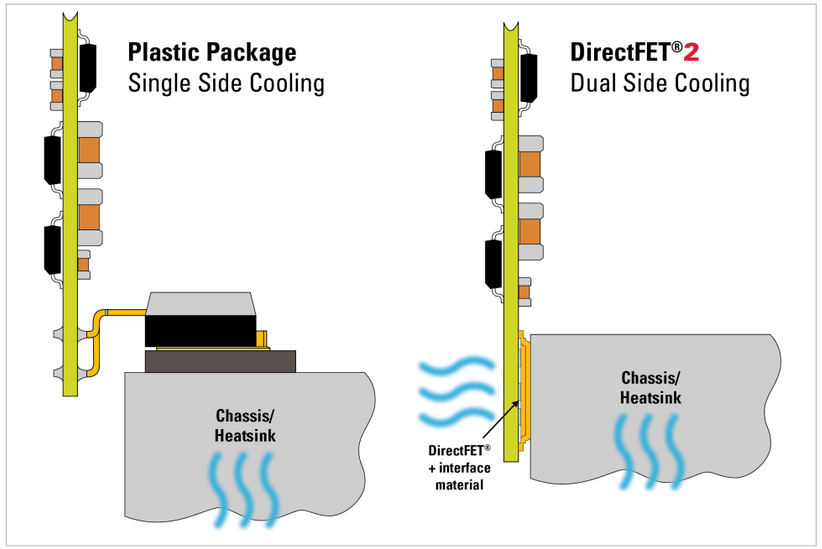

Figure 2: Dual Side Cooling of DirectFET2 significantly improves the power density

two main areas to improve the system power density – either through the innovation of the new material technology, or through the innovative power packaging such as IR's DirectFET2 performance power package. **Figure 1** summarizes the key benefits of the DirectFET2 performance power package. DirectFET2 utilize the Copper Can on top to directly conduct the high current – therefore no wire bonding, no leadframe, and even no mold compound is required. This structure makes the package easy compliance with automotive standard, and all DirectFET2 products are specifically optimized for automotive applications and pass the stringent AEC-Q101 automotive reliability standard. On the other hand, low package inductance reduces parasitic ringing and therefore improves the EMI performance, and low package resistance minimizes conduction loss.

Another important feature for DirectFET2 lies in its superior thermal performance by utilizing the dual-side cooling concept. For traditional plastic surface mount package such as DPAK and D2PAK, package molding is always needed to accommodate the wire bonding, however molding compound have huge thermal resistance therefore prevent the topside cooling, furthermore the bottom side cooling is always limited by the PCB thermal impedance. **Figure 2** shows the comparison of the cooling methodology between plastic package and DirectFET2. For plastic package, cooling through the PCB becomes impractical for many high power applications; therefore complicated and costly mechanical assembly is needed to achieve the good single bottom side cooling. On the contrary, DirectFET2 could take advantage of dual side cooling both from bottom PCB and from top heat sink, the flexibility of topside cooling significantly simplifies the mechanical design, reduces the system cost and improves the system overall power density.

The semiconductor industry is in fast changing mode, as newer technology arrives at an ever increasing rate, consumers are discarding their obsolete products quickly. Motivated by addressing the global issue of consumer electronics waste.

	RoHS 5/6	RoHS 6/6
Pb free package	√	√
Pb free solder	exempt	√

Table 1: RoHS 5/6 vs RoHS 6/6 Comparison

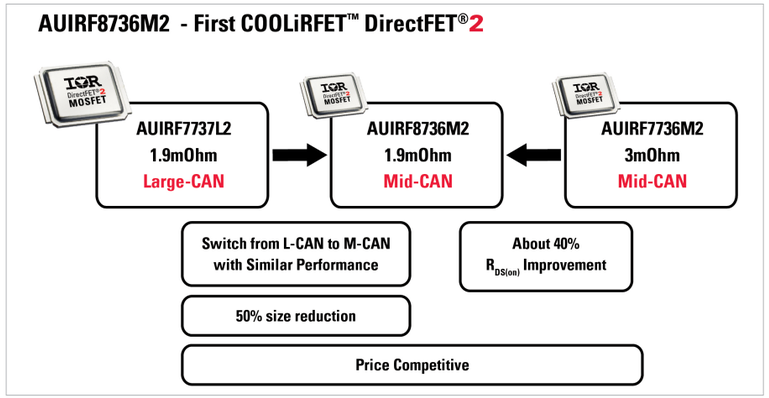

Figure 3: First DirectFET2 package with COOLiRFET™ benchmark silicon platform

The Restriction of Hazardous Substances Directive 2002/95/EC (RoHS) standard was adopted in 2003 by the European Union. Nowadays RoHS has become the benchmark compliance standard for removal of hazardous materials from electronic components. RoHS compliance refers to an EU law to limit the concentration of these substances:

- Cadmium (Cd)
- Hexavalent chromium (Cr [VI])
- Lead (Pb)
- Mercury (Hg)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ethers (PBDE)

As shown above - one of the six banned substances is lead. RoHS 5/6 and RoHS 6/6 are abbreviations commonly used in the industry to designate components or products that comply with the RoHS Directive. RoHS 5/6 refers to products contain lead used in an exempt application, and RoHS 6/6 refers to products below the applicable RoHS Directive limits for all six substances without relying on any exemptions (see **Table 1** below). Many power devices are still allowed to use lead internally, the solder die attached material offers excellent thermal conductivity, very low electric resistance, and high-melting temperature which allows the solder inside the package not to melt when the pacakge is reflowed on the PCB. This exemption is set to expire in 2016 requiring the redesign of systems using non-compliant devices. The new RoHS 6/6 standard requires 100% lead free, even for the internal die attached material.

DirectFET2 is already RoHS 6/6 compliant - It uses epoxy for die attach material - the epoxy is optimized for thermal and electrical conductivity, the performance is comparable to solder yet contain no lead, therefore DirectFET2 package is a completely lead-free power package that meets all present and future RoHS regulations.

For semiconductor discrete components, package innovation always need to in line with benchmark silicon platform to ensure the excellent component level performance.

IR's 40V automotive grade COOLiRFET™ MOSFET platform finds itself a perfect fit for these 12V battery heavy load applications. By utilizing the most advanced trench technology, COOLiRFET platform sets the new industry's benchmark Rds(on) performance, and by combining automotive DirecFET2 performance power package with benchmark COOLiRFET silicon technology, system designers can benefits from significant power density improvement and 100% RoHS compliance.

Figure 3 shows the key benefits of the first COOLiRFET DirectFET2 part. By leveraging IR's benchmark COOLiRFET™ silicon technology with the power performance DirectFET2 package, AUIRF8736M2 brings a 40% Rds(on) improvement in the same footprint or equivalent performance to Large Can device in 50% smaller package reducing overall system size and cost for automotive applications.

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How smart is the Smart Grid when the computer crashes?

Over-reliance on a central computer is an invitation for disaster

By: Edward Herbert, PSMA Energy Efficiency Committee

Software security in the grid is becoming increasingly important. There have been reports of appliances hacked to send SPAM, and The Wall Street Journal claims that the Smart Grid already has been penetrated and infected with potentially disruptive software programs. There are even fears that terrorists may penetrate the SCADA systems in utilities and wreck a generator as revenge for "Stuxnet.". Homeland Security surely is giving this attention.

My concern, however, is more mundane: what happens when the computer crashes? What should happen is "nothing," or at least nothing that does damage or that cannot be managed expediently.

An infrastructure using central computers with multiple sensors overlaying the Grid is a very powerful tool, with great potential for improving Grid performance and reliability. Using real-time measurement, such systems can pinpoint where repair is needed during a crisis, as well as predict problems. Computer-based management systems allow for unprecedented modeling and calibration. For example, the advantages of automated meter reading for billing are well recognized. However, over-reliance on a central computer is an invitation for disaster. A Grid that requires a central computer and communications for stable operation very likely will become unstable when the computer crashes.

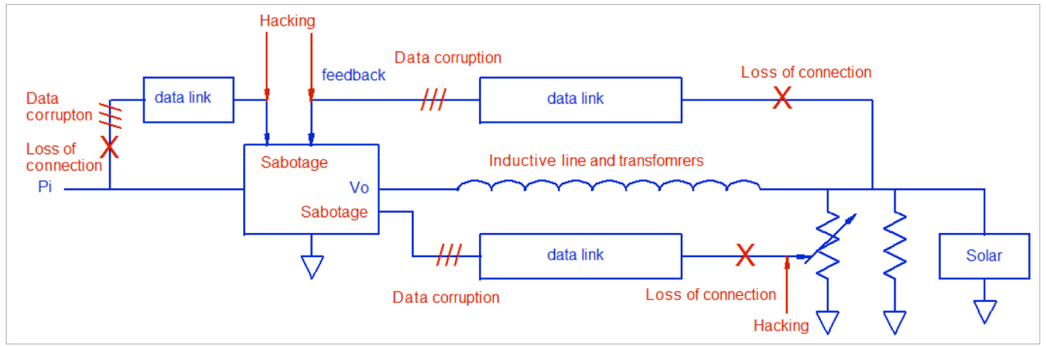

Figure 1: This model of the Smart Grid is based upon a power supply with remote sense. There are many vulnerable points.

Command & control

One of the justifications for the Smart Grid is that we can avoid building more power plants if we can send out commands to reduce the load in times of stress. What happens if you cannot implement those commands? Times of stress are when a central computer is most vulnerable, most likely to be unusable (see **Figure 1**). Power supply designers understand the need for stability

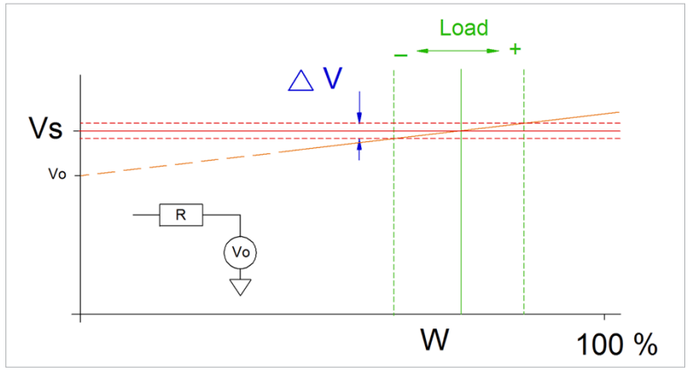

Figure 2: Local control that varies the load in response to line voltage, as an example, is fast and does not rely on a central computer. Other parameters that can be used are frequency and phase angle.

analyses. Loop stability is dependent on response, and lags are a problem. Has the Smart Grid been analyzed to account for lags? What about the time needed to collect and analyze Mega-data, and output the commands to the control devices? A denial-of-service attack could slow the response to a crawl. The lag will make it impossible to respond quickly. Taken together, the inevitability of computer crashes and the slow response make it imperative that local systems have robust default modes and fast response to rapidly changing line conditions. Local controls need to be there. If well done, they mitigate the need for centralized computer control (see **Figure 2**).

The threat of hacking

The conversation needs to include hacking, as it is a sub-set of computer failure. Anything that connects to the Internet has the potential of being hacked. The most effective hack renders the equipment inoperable and non-repairable. Unfortunately, this is much easier than most people realize, partly because of the features that are built in for tight security. Consider a malicious command that turns an appliance off, followed by a firmware update that makes it non-responsive to any command or override. Or a hack that changes the encryption key, so that the appliance responds only to the hacker, or to no one at all.

Contrary to popular perception, the greatest threat of hacking is not the foreign terrorist but disgruntled employees. Regardless of security and encryption, most commands originate with a person or an algorithm. The bookkeeper that notes that a customer is delinquent disconnects him with a click of a mouse, and security won't stop her. She probably cannot update the firmware or change the encryption keys, but if you substitute the consultant

who is hired to upgrade the anti-virus software, he could. He can plant a logic bomb that simultaneously shuts off thousands of customers after he has moved on. Thousands of Smart Meters, shutoff, with corrupted encryption keys, is scary.

The best defense against hacking is having it not do much, the same as the preferred response to computer crashes. If hacking did not do much, it would be no fun and the hackers would stop trying.

So, what can commands from a central computer do that is safe? Often, the concern is "data security," whether a burglar could tell who isn't home by motoring appliance use. While important, that will not threaten the stability of the Grid. So, monitoring and collecting data are OK. But why does a refrigerator need the computer power to send emails? Part of the answer may be limiting function to what really is needed.

Market issues

Much of power management is arbitrage. Arbitrage cannot be managed by detecting line conditions, so it needs to be authorized and commanded from a central authority. However, arbitrage does not require abrupt changes. One way to limit the ability to do damage is to apply power changes due to arbitrage at a very slow rate, slow enough so that errors will be detected and corrected before damage is done.

One function that the utilities would never give up is the ability to shut off the power to delinquent customers. There is no urgency. If shut-off commands were sent but could only decrease the power by 4 % per hour, constrained by hardware, it would take a day to be turned off entirely. That's OK. Mistakes could be caught and corrected, and the customer might even pay his bill.

What if the encryption keys were hacked? The default mode should be "On." Absent commands that maintained the off-state, the Smart Meter should ramp up 4% per hour.

How about power control during heat waves? The same mechanism can apply. The default power allowed by the Smart Meter should be a reduced level, a baseline power that would not overload the system even in times of high demand. Buying more power above the default level is arbitrage, and would require command and response to enable and sustain it. 99.9% of the time, this would be fully functional. When the computer crashes, everyone has enough power to get by and the total load is low enough not to overload the Grid.

Note that in the above scenarios, the Smart Meter is not relaying commands to control specific appliances. It is just enabling a percentage of baseline power, lower or higher. It is up to the customer to turn-off some appliances or buy more power on the spot market when necessary. The sophisticated customer may have a load management computer tied to his smart phone. Others may just unplug what is not needed. The computational power and software needed by the utilities is much less, therefore much less expensive.

Little mention is made of liability, but once it is considered, the utilities may realize that the risk of having explicit control of specific appliances may be unacceptable. What is the liability if a freezer is turned off, but cannot be turned on? Times 10,000?

There was a surge in Smart Meter deployment with large grants, but now the Smart Meter manufacturers are trouble as sales lag. Security concerns may be a significant factor. Utilities may be realizing that getting it wrong could be very expensive.

This article reflects the opinion of the author, not necessarily that of the PSMA

Optimizing Smart Grid Power Connection Functionality

The best solutions combine strong DC current capability with accurate timing functions

By: Chris Siegl and Aung Tu, Fairchild Semiconductor

Advances in system level goals of the Smart Grid to better manage electrical loads during high demand time of use or during a shortage of available resources have created a need for efficient methods of connecting and disconnecting loads from the grid. Load management systems have been available in the commercial and industrial arena for some time. However, with the Smart Grid management systems now advancing on to the stage of controlling devices within the residential and commercial applications, the reliability, efficiency, and cost-effectiveness of such devices become more critical.

The connect/disconnect solutions must be tolerant of the noisy environment of the smart meter as it is directly connected to the incoming feed from the grid and controlled by a micro-controller. The best solutions combine strong DC current capability to open even welded shut contacts with accurate timing functions to filter out noise, relay protection, and the compatibility to optimize the micro-controller clock cycles.

This article reviews both the implementations currently in use and those in development.

Smart Grid system load management proposals, as well as switches needed in various emerging countries are also reviewed. Mechanical dual-coil relays are examined to define optimized driver circuits that provide the needed functionality.
The article concludes with a discussion of the power systems needed to drive the connection relay, as well as the driver trade-offs to meet the proposed performance specifications.

The Impact of Smart Grid

The Smart Grid initiatives have spawned new approaches in load management. The basic technology of remote controller and sequencing of loads in its basic forms has been a function of the industrial market for a long time with complex incentives for businesses to participate. Initially this was done largely through individual device wire telephone connections back to the utility as well as warning and request systems through a mechanism of telephone communications devices.

The cost of this has dropped dramatically with the introduction of wireless and Power Line Carrier (PLC) communication technologies and a healthy competition resulting in improved performance at constantly diminishing costs. Not being dependent on direct hardwire installation and intrinsic safety in the wireless implementations dramatically reduces the cost and complexity of the installation process.

The Residential Meter Market

Another inducement for an economical connect/disconnect requirement comes from the residential meter market. Enabled by the improvements in timely communications to individual meters and local control functions, the ability to remotely open a meter load greatly reduces service costs for a simple service stop or service restoration. There is no longer a need for a service truck when customers request service interruption and re-connects, such as for seasonally occupied vacation and rental properties.

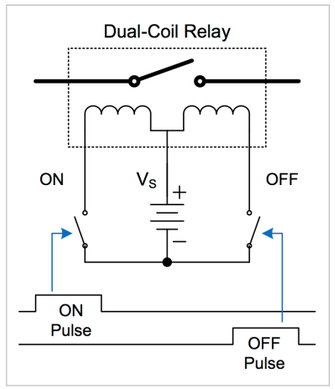

Figure 1: Simplified Diagram of a Relay Drive

Service personal interaction over non-bill payment issues is also minimized. Similar savings apply to temporary construction sites and other venues not needing continuous usage. This remote management capability also reduces power theft in these unoccupied sites and mitigates the associated power losses.

Mitigating meter socket failures

There have been concerns over recent instances of fires starting around newly installed smart meters in older meter sockets. When replacing older meters that have been in place for a long time, the issue has been traced to heating in the meter socket due to corrosion in the contacts to the meter. Heat buildup in the socket is a function of load current and level of corrosion, primarily caused by weather damage and water seepage. Disconnecting the load and reporting the over-temperature condition puts the meter in a position to mitigate the damage safely.

Disconnect after power is lost

Gaining in importance in contactors is the ability to disconnect and re-connect after power has been lost. This is especially important when controlling devices such as compressors, which have high start-up surge currents and are best not cycled without a minimum off time (compressors overheat if cycled over short intervals). Power restoration surges can be reduced by delayed turn on and sequencing of loads, thereby reducing peak surge currents and stresses on delivery equipment as well as loads.

Meter-based and load-based contactors can provide this function with capacitor stored holdup power which is sufficient to pulse the contactor open even in the power-loss event. Smart Grid research is showing significant advantages in equipment reliability and stability using these types of policies.

The Industrial Market

In the industrial market the contactor function has been implemented with a variety of approaches. Motors have been used to drive contactors but these suffer from slow speed during the opening operation with resulting arcing damage. For larger systems, various forms of arc suppression are often used including compressed gasses and spring assisted fast-switching mechanical implementations. These are not economical for the higher volume cost sensitive markets. Therefore the emerging consensus is to use a polarized bi-stable latching relay utilizing two coils with one coil pulsed to move the relay from the closed position to the open position and the second coil to move the relay from the open position to the closed position.

Detailed look at the Driver Configurations

The bi-stable, two coil latching relay is the most common configuration. Some versions include built in springs and other mechanical assistance in the open direction for lower-power operation.

The typical load connection function is implemented with a bi-stable contactor device with two or more poles to disconnect. The contactor is usually wound with two windings; one to close the contactor and the other to open the contactor. A permanent magnetic material or a mechanical latch is used to hold the contactor in place when it is not switching.

To facilitate the mechanical movement, the relay coils need to be energized for a specific time interval. Once the contact(s) have changed position, the voltage should be removed from the winding of the relay. A simplified, typical circuit diagram is shown in **Figure 1** with example waveforms.

Relay Drive Circuit Requirements

As the diagram shows, a dual-coil relay is connected to its supply rail at the center point of the two relay windings. Each winding can be energized by the switches connected

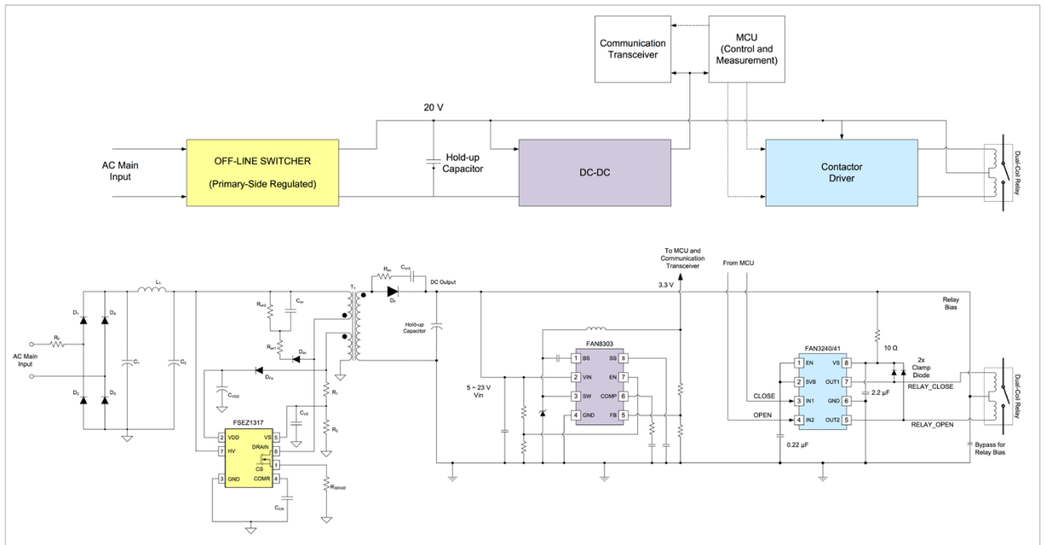

Figure 2: a block diagram of a typical metering system

to the relay coils. The two switches must not be on at the same time, which would cause excessive currents to be drawn from the supply rail, and result in improper operation and damage to the relay.

To accommodate the relatively long time required for the relay contact to travel between its stationary positions (ON and OFF positions), the pulse must be longer than the minimum duration specified in the relay specification. It is also desirable to limit the maximum length of the drive pulse to prevent potential saturation of the relay winding and to avoid over heating the coils and drive electronics. The control signals should also be compatible with latest generation of microcontrollers supporting both CMOS and TTL input levels.

The relay specification also defines the minimum and maximum operating voltages for reliable operation of the contact(s). The voltage requirements of the contactor vary by application, which is driven by tradeoffs in meter requirements. Lower voltages are common in lower-cost low-power applications where the meter and the relay sizes are smaller. Higher voltages are common where higher currents are needed where the larger contacts require more power to switch. Therefore the drive circuit should monitor the relay bias voltage for sufficient voltage level. It is also desirable to have an under voltage lockout for the drive circuit to facilitate smooth startup while circuits initialize.

The preferred integrated solution provides input signal qualification for the control signals, protection against simultaneous activation of the two relay coils, a maximum drive pulse duration limit, and additional basic functions such as bias voltage monitoring, driver enable input, and thermal protection for the driver. The ideal circuit minimizes component count and board space, while increasing the reliability of the system and the noise immunity of the circuitry when driving the coils of the relay.

Practical implementation of power and connect/disconnect

Figure 2 shows a block diagram of a typical metering system. The relay drive voltage is a function of the particular relay used. In general, larger current switching relays (larger contacts) require higher voltages to deliver enough energy to switch fast enough to minimize contact loss due to arching during the switching. Usually this high voltage source is provided by a capacitor to provide maximum power during switching especially in applications where

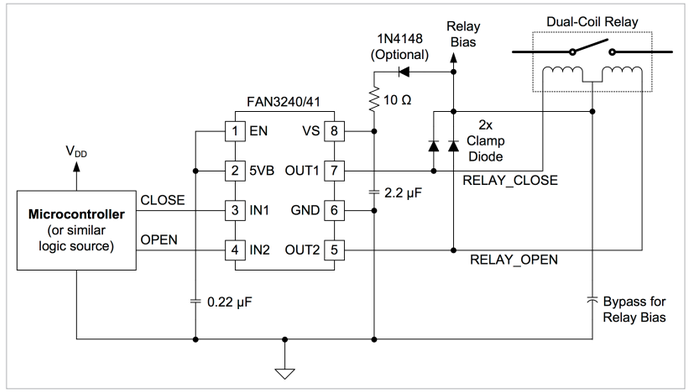

Figure 3: A relay driver such as the FAN3240 or the FAN3241 with a built-in bias supply can be very beneficial

switching occurs after power is lost.

The capacitor has to be sized to provide the energy needed to switch successfully. The capacitor charging supply can be current limited, reducing the power supply cost by taking time to bring the switching voltage to full charge. The disconnect switching is an infrequent event in meters. The typical devices being switched, such as compressors, have a minimum required off time for long life operation. Longer recharge times reduce power supply cost and stresses without impacting performance.

Communications, control and measurement functions are typically implemented with low-voltage (3 to 5 volts) circuits such as micro-controllers and communications circuits. There are a variety of communications technologies that focus on particular market requirements and geographic constraints. Most of these have a burst profile where power consumption is on the order of 5-watt transmission for 100 milliseconds followed by a delay of one second or more before the next transmission. Transmission after power is lost (reporting the status of the network at the time of power loss) is also desirable for times of up to 10 minutes for last transmissions.

The holdup capacitor as described above for the disconnect function applies as well to the communications circuit if a DC-DC stage is included for efficient low- voltage conversion from the high-voltage capacitor. The holdup capacitor can now be shared by the transmission and disconnect functions if sized appropriately.

For a current-limited, off-line switcher supply, a primary side regulated flyback controller with an integrated MOSFET such as the FSEZ1317WA makes for a feature-rich economical solution.

The DC-DC block can be implemented with the minimal-parts-count high-performance solution such as the FAN8303, a step-down regulator with an integrated switch. Finally, the connect/disconnect drive designed to meet the requirements as defined in this article can easily be implemented with the recently introduced FAN3240 and FAN3241 smart dual-coil relay drivers.

When Isolation is required

Sometimes isolation is required in cases such as when there is wire-line communications or where there are a number of circuits on different phases controlled from a common point. A relay driver such as the FAN3240 or the FAN3241 with a built-in bias supply can be very beneficial in reducing parts count and cost as well as circuit simplifications as shown in **Figure 3**.

Conclusion

Variations on the presented solutions can be applied to other smart meter power requirements as well as distributed connect/disconnect functions in a variety of specific applications. As the Smart Grid functionality continues to expand in complexity, new opportunities will emerge for new power management functions. Fairchild Semiconductor has tools, application notes and application pages accessible through the Fairchildsemi.com web page to help you in your design process.

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Advanced packaging critical to power system performance

The last decades have witnessed aggressive advances in semiconductor miniaturization

By: Doug Ping, Vicor

Packaging for power electronics has evolved from simple metal bending to advanced materials and thermo-mechanical design, and from freestanding supply to integrated power management. System-size reductions made possible by higher switching frequencies and semiconductor miniaturization drove the early part of this trend. The more recent improvements, however, have also depended on advances in thermo-mechanical design, particularly of power management components.

Beyond the Box

The last decades have witnessed aggressive advances in semiconductor miniaturization. During the 30 years from 1982 to 2012, commercial processes for fabricating CMOS logic shrank from the 1.5 µm node to the 22 nm node (see **Figure 1**). The resulting increase in functional-density—more than 4,600:1—has altered the course of electronic product design, not just within computational cores or memory subsystems, but throughout the product as well.

At the start of this interval, typical electronic products provided low functional density and presented modest power demands, so power supply designs made use of discrete components and less than optimal cooling methods. Although supply efficiencies were poor by today's standards, they were sufficient given their prod-

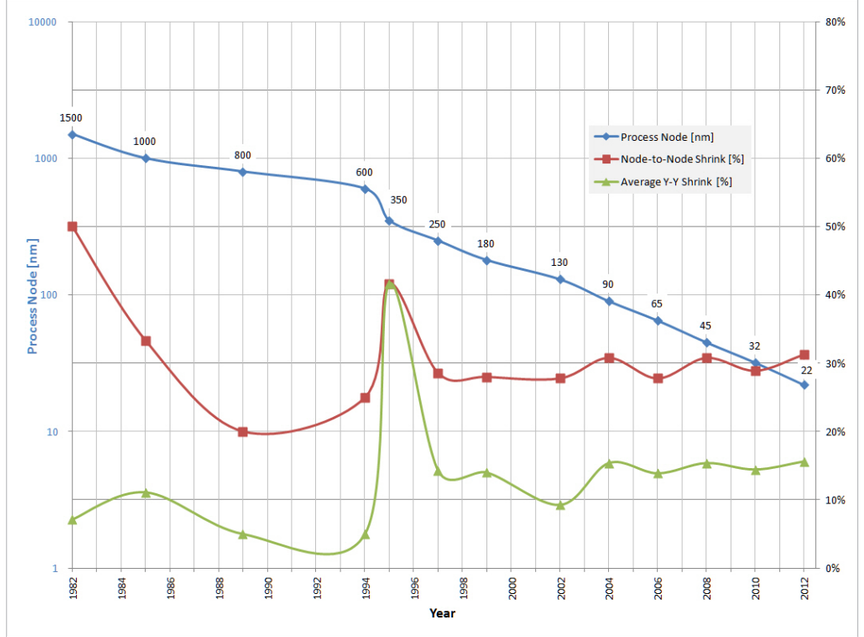

Figure 1: In three decades, commercial semiconductor processes for fabricating digital circuits have moved from the 1.5 µm node to the 22 nm node, shown here on a logarithmic scale (left).

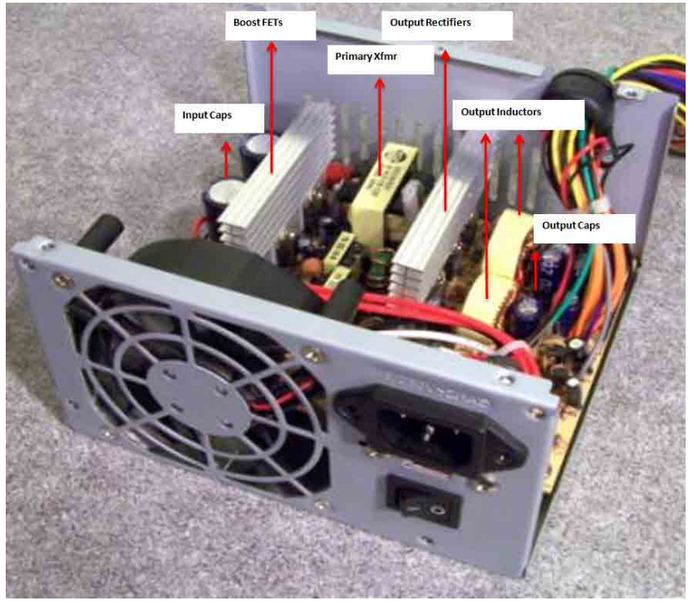

Figure 2: Traditional open- and closed-box power subsystems, including the ATX12V silver box power supply shown here, provide low power density and limited scaling potential.

ucts' low power requirements and large enclosure size.

Among the best-known examples of these designs that remain in use today are the silver-box supplies that power desktop computers. For example, a 400 W ATX12V features a largely discrete design (see **Figure 2**). Individual heatsinks cool power MOSFETs and output rectifiers but the overall thermal design results in large thermal gradients, which are problematic at high ambient temperatures. With a typical efficiency of 80%, the 138 x 86 x 140 mm form factor provides a power density of only 0.24 W/cm^3. ATX supplies meeting the 80-plus platinum criteria can almost double that number to 0.42 W/cm^3 but are still insufficient in power density and not practical for most central office and data center applications.

The progression of semiconductor miniaturization imposed changes to power subsystem architectures. ICs fabricated at smaller process nodes require ever-lower operating voltages and tighter supply-voltage tolerances. Higher functional densities increase supply currents and highly variable resource schedules dramatically increase load-current dynamics. Under these load conditions, designs that separate power sources from their loads by significant lengths of copper cannot provide the performance that these small geometry ICs require.

Slick as a Brick

A number of alternative structures arose in attempts to optimize power subsystems for various physical arrangements of loads. For example, high up-time applications, such as communication line cards, replaced large, inefficient, multi-output supplies with distributed power architectures. These designs begin with redundant single-output AC-DC converters to ensure that the reliability of the distributed voltage, typically 48 V, meets the system's uptime requirements. Line cards usually use on-board brick converters followed by a number of small non-isolated point of load (POL) regulators to power individual resources.

Largely discrete, forced-air-cooled power subsystems present uneven surfaces to the cool-air source resulting in turbulent airflow, which can lead to thermal shadowing and hotspots. Encapsulated brick converters use potting compounds to form essentially isothermal devices. Within the encapsulant, power devices thermally couple to an aluminum baseplate, which provides a single cooling surface. Cooling can proceed by conduction, forced-air convection, or a combination of both.

The baseplate surface provides a large contact area for heat-sink attachment. This thermo-mechanical design allows a 600 W max output power from a 117 x 55.9 x 26 mm package and 12.7 mm heatsink (inclusive) for a power density of 3.5 W/cm3—an order of magnitude

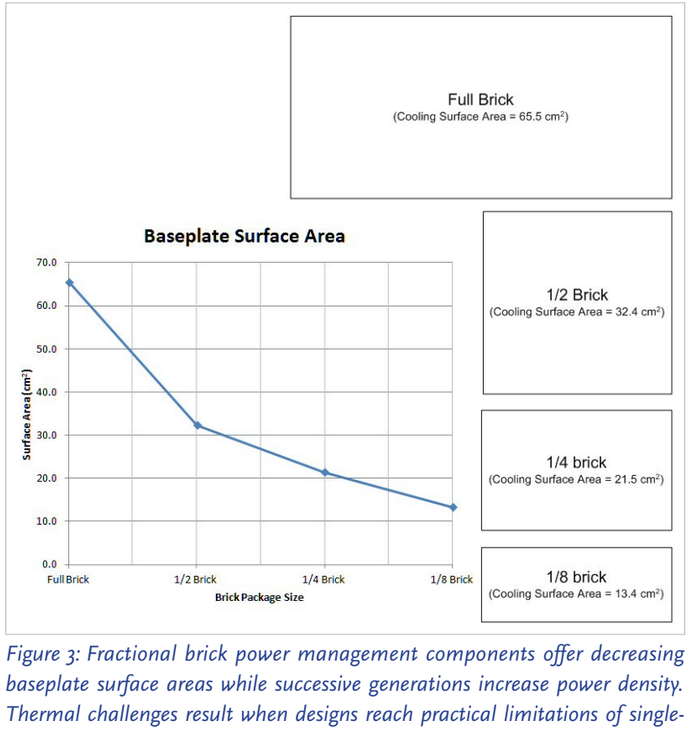

Figure 3: Fractional brick power management components offer decreasing baseplate surface areas while successive generations increase power density. Thermal challenges result when designs reach practical limitations of single-sided cooling methods.

improvement over closed-frame silver-box designs.

As product functional densities continued to increase, the brick form factor quickly gave rise to fractionally sized versions—half, quarter, and eighth-brick—while successive generations provided increasing power capabilities. The fractional-brick's shrinking cooling surfaces constituted a thermal challenge for system designs pushing both functional and power densities (see **Figure 3**). This challenge was exacerbated in applications for which typical ambient temperatures were on the rise as was the case, for example, in server farms and communication hubs.

Most Like it Cool

By now, the functional density of most electronic applications make thermal design an important part of new-product development. The current demands and current dynamics that characterize most products requires embedding the power management subsystem within the functional design—a break from the tradition that held subsystems as freestanding objects.

With electrical loads—heat dissipaters—and power management components (1-η dissipaters) co-locating on system boards, thermal challenges grow with increasing operating temperature: Excess heat reduces the reliability of electronic components. Additionally, designers must derate power components for operation at elevated temperatures so, without effective methods of eliminating heat, power trains become over designed, resulting in larger, heavier, and more expensive systems.

So, as significant an advance as brick packaging technologies were, and while the brick form factors still play a role in terms of simplicity, the industry has grown to need even more dense power management devices beyond what can be accomplished with purely single-sided cooling.

One example of advanced packaging that improves power processing and delivery performance is the Converter housed in Package (ChiP) technology from Vicor. ChiP-based devices exploit symmetrical configurations placing dissipative devices on both sides of a central PCB. A thermally conductive encapsulant transfers heat to both the top and bottom surfaces effectively doubling the cooling surface area relative to the device's PCB footprint (see **Figure 4**). With appropriate system PCB design, additional heat can conduct through the electrical contacts as well.

A combination of high efficiency—97.5% peak for 380 to 12 V bus converters—and symmetrical thermal design with advanced materials can provide 1.5 kW. Including heatsinks and a fan assembly, a 40

Figure 4: Advanced packaging technologies, such as Vicor's ChiP, support symmetrical thermal designs exploiting top- and bottom-side cooling.

x 40 x 100 mm assembly offers a power density of 9.4 W/cm^3 (see **Figure 5**).

Advanced packaging technologies such as this provide 3-D thermal management schemes in either surface mount or through-hole mount form factors. Integrated magnetics promote designs requiring few external components, saving design-cycle time, circuit board area, and product assembly costs.

The encapsulant promotes efficient heat transfer while providing a level of safety insulation commensurate with high-voltage power management requirements and international safety standards.

This allows the same packaging technology to apply to a wide range of power management functions. These include AC-DC conversion with power-factor correction; isolated bus conversion; DC-DC conversion; buck, boost, and buck-boost regulation; and POL current multiplication. A single packaging technology that is applicable to the full menu of power management tasks from power entry to POL can also simplify system thermo-mechanical design by unifying device profiles and thermal characteristics.

Capabilities and scaling vary among various power component manufacturers, so check your vendors' offerings carefully. In the case of Vicor's ChiP-based components, devices can attain thin profiles to 4.7 mm and footprint areas from 6 x 23 mm to 61 x 23 mm, and expanding. Current capabilities extend to 180 A and operating voltages to 430 V, and rising. The company has demonstrated power delivery capabilities in this package technology as great as 1.5 kW, and that number is set to increase as well.

In lower-power applications such as POL converters, small-footprint, low-profile packages provide system designers with additional flexibility to minimize trace lengths from power converter to load. When powering digital resources characterized by high dynamic currents, such as ASICs, processors, or memory subsystems, low loss and low inductance power feeds ensure tight regulation and rapid transient response measured at the load, where it counts.

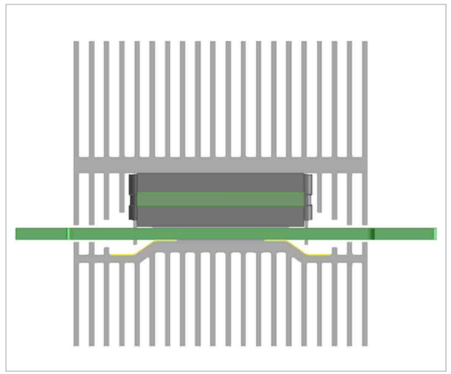

Figure 5: Power management devices taking advantage of advanced packaging can deliver as much as 1.5 kW from cells measuring less than 10 in^3 including heatsinks and fan.

This type of packaging technology also supports high voltage-ratio converters, which in some applications can allow designers to eliminate an entire conversion stage, reducing system cost, increasing the power-train's end-to-end operating efficiency, and increasing reliability.

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Special Report: Powering Industrial Applications

PSSD NORTH AMERICA

Empowering Global Innovation

Inside:

Digital power cuts time-to-market for industrial applications

Power designers have the possibility to tailor power solutions for specific functions

By: Patrick Le Fèvre, Ericsson Power Modules

Given the range of industrial applications is extremely diversified – from very small sensors powered by energy harvesting to mega processors used for process control and huge data computing capabilities required by some industrial equipment – the challenge for power designers remains the selection of the most efficient power architecture across a large variety of applications.

Figure 1: MicroTCA power supply with digital DC/DC and PMBus interface

Unlike the Information and Communication Technology (ICT) industry where boards often combine multiple processors and where the possibility of 3kW per board is moving closer, it is very common in industrial applications to design dedicated embedded computing functions for platforms such as MicroTCA or similar with dedicated boards for specific functions. The use of these cards makes upgrades or repairs easier for a site manager without needing to replace the entire system.
The direct consequence of this type of architecture is that power designers have the possibility to tailor power solutions per board for specific functions, and to quickly implement new technologies such as dynamic energy management and control when upgrading systems' controllers or data processing boards without having to wait for a complete system refresh.

Driving industrial applications

Industrial applications have used analog power modules for decades now, though with the growing demand for higher energy efficiency and tight control of energy, by 2008 the industrial segment had started to implement DC/DC converters and isolated POL (Point-of-Load) regulators with the PMBus. The first commercial application addressed the MicroTCA segment (see **Figure 1**), in which embedded digital PMBus-based DC/DC power modules simplified monitoring and control of the power unit.
In addition, auxiliary boards started being populated with POLs with PMBus, initially being used for monitoring functions such as local temperature, output payload conditions and many other features, but rapidly system designers began to make use of the full performance benefits delivered by the PMBus.

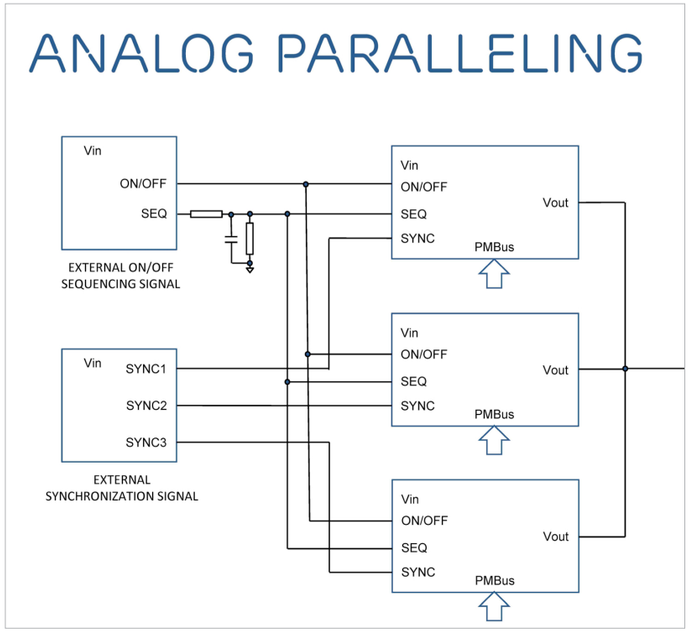

Figure 2: External circuitry required for paralleling and phase spreading when using conventional analog or analog-hybrid POL

As happened in the ICT industry with the growing implementation of more complex ASICs, FPGAs and other processors, by 2012 industrial board power designers were also facing this situation and were having to design flexible power solutions that could meet specific profiles, not only during the design phase but also when the system was up and running.

For many designers used to a conventional power setup, designing a power solution based on relatively complex hardware combining analog, or analog-hybrid POLs and fixed components such as external clocks and multi-gate synchronization ICs (see **Figure 2**), they rapidly understood that the level of flexibility required in new applications made conventional processes significantly more complicated than that of simpler architectures.

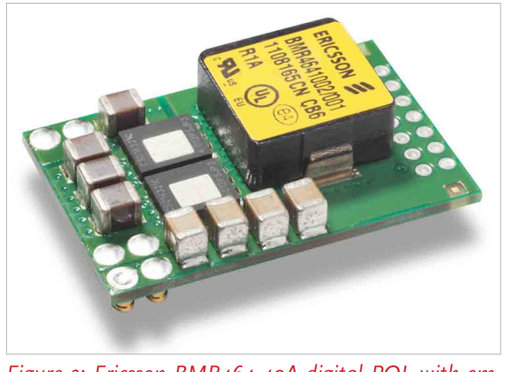

Figure 3: Ericsson BMR464 40A digital POL with embedded and advanced features simplifying paralleling and phase spreading

In addition, a power setup that required hardware modifications to adjust parameters such as sequencing or phase spreading would impact on time-to-market, which is crucial for many applications. It became a question of how best to make complex power architectures simple, efficient and reliable?

Simplicity in complexity

To achieve this required board power architects to explore different ways of working and consider new technologies such as digital power with built-in features. The most recent digital POLs (see **Figure 3**) with embedded features are making it possible to operate each module in a very complex power setup without adding external circuitry (**Figure 4** shows the level of simplicity offered by digital power).

In industrial applications, embedded computing has gained in processing power, often using complex ASICs with multiple cores or quad-core multi-chip-module ICs. Considering that these types of applications require an average of 70A per channel, the embedded computing board could demand up to 300A when at operating at

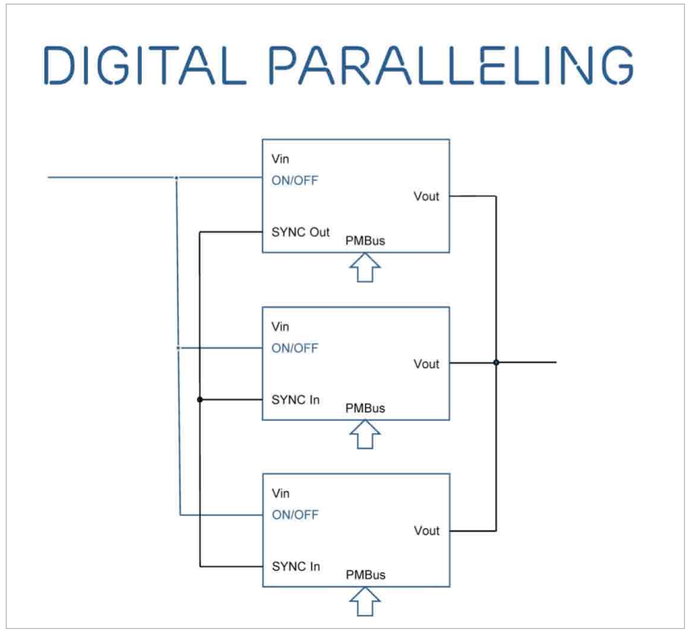

Figure 4: Schematic for paralleling and phase spreading when using full digital POLs

full computational performance. Figure 5 shows this type of application and – despite the power setup requiring a number of features, which will be described later – it is easy to see that very few components related to the power setup are actually required to efficiently power such a demanding application.

While it illustrates the simplicity of the hardware required, the highest benefits reside in the simplicity of the orchestration of different power sequences to optimize energy utilization and reduce ripple and noise, while also retaining a very high level of flexibility such as the ability to change any parameter and at any time without hardware changes.

Silence and flexibility in high current switching

At 300A, noise resulting from the switching stage could have a dramatic effect on performance.

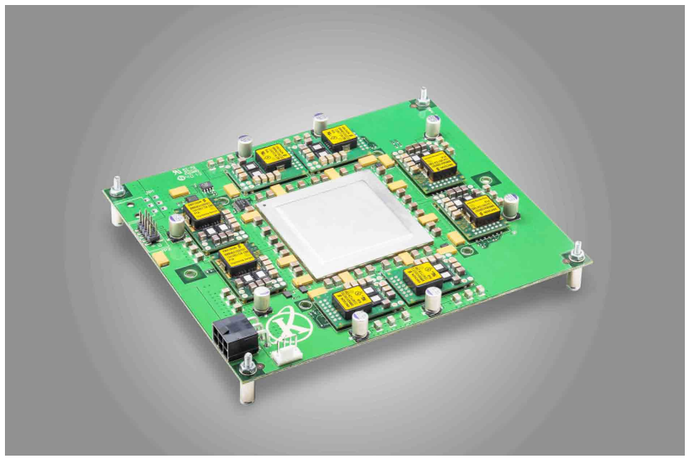

Figure 5: Quad-core industrial embedded computing application requiring up to 300A (average 70A per core)

In conventional PCs, Voltage Regulator Modules (VRM) are built on multiphase topologies; but in the case of the application shown in **Figure 5**, while also enabling the lowest power losses and highest efficiency, each core needs to be powered by a dedicated pair of 40A modules connected in parallel. Phase spreading is implemented to reduce noise and via the use of interleaving, the four pairs of modules switch with the lowest level of ripple that is possible with this technology.

As mentioned previously, using conventional power architectures to implement paralleling with phase spreading requires significant hardware (as in **Figure 2**). However, it can be achieved using software such as the Ericsson Power Designer tool to visualize the phase-spreading effect on ripple and noise in real time.

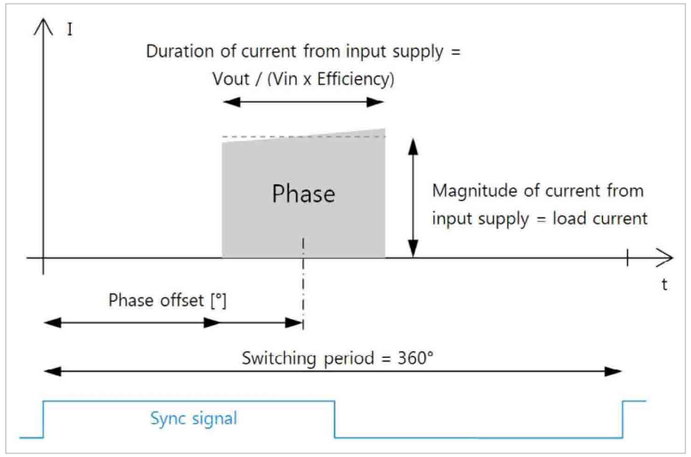

Figure 6: Phase shifting basic principles

The simplest way of phase spreading is allowing the products to operate individually from their own internally generated clock. This randomizes the occurrence of the edges of the switching frequency, which reduces the chances of high peak currents from the input source. However, this method also produces results that are not repeatable. A more controlled and effective way of phase spreading involves distributing the phase edges of each product in a group by operating them from a common switching clock. A single clock source can be used for all products and each product has its phase set to a different value throughout the cycle of the clock.

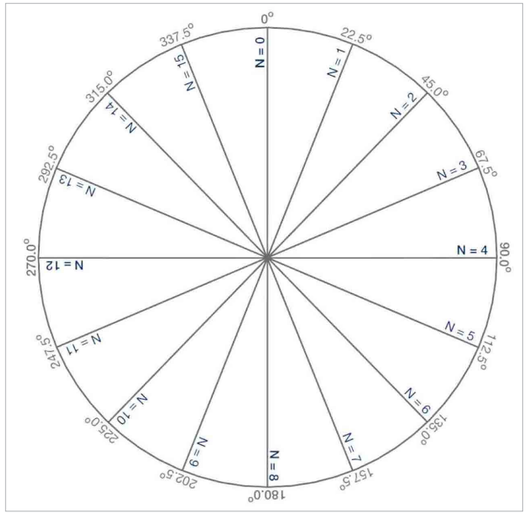

Figure 7: Phase shifting, offset wheel

Phase offset and offset configuration

Assuming the POL regulator is supplied from a common input source, each converter is represented by a phase with a certain magnitude and duration in the switching period, as illustrated in **Figure 6**. The magnitude of the phase is the current drawn from the input supply, which approximately equals the output current of the rail. The duration of the phase as a fraction of the switching period equals the duty cycle of the rail, which in turn depends on the output voltage and actual efficiency of the converter. To achieve a phase spread, each phase needs an offset. The phase offset is defined as the time from the sync signal edge to the beginning of the phase duration.

For non-current-sharing rails, the phase offset is defined by the INTERLEAVE command by the Number In Group value (1-16) together with the Interleave Order value (0-15). The offset can be expressed in degrees or time according to the formula below, where TSW = 1/FSW is the switching period.

$$Offset(°) = 360 \times \frac{Interleave\_Order}{Number\_in\_group}$$

$$Offset(s) = T_{SW} \times \frac{Interleave\_Order}{Number\_in\_group}$$

An example

To demonstrate how simple it can be, consider a configuration based on three rails populated by 3E digital POLs delivering core and auxiliary voltages to a processor. Following the equations and using the values shown in **Table 1**, the ideal phase offsets can be calculated. By using the phase-offset resolution wheel (see **Figure 7**), these are the actual phase offsets to be

Product	Number in Group	Interleave Order	Phase Offset (Ideal)		Phase Offset (Actual)
BMR462	3	0	0	0	0°
BMR463	3	1	120°	1/3 x T_{SW}	112.5°
BMR464	3	2	240°	2/3 x T_{SW}	247.5°

Table 1: Example of the parameters used to calculate the offset

entered into Ericsson Power Designer.

By default, the phase shift is set to zero with the result that all the rails will draw current at the same time, causing noise and uneven input current. To change this, phase spreading can be achieved by configuring specific phase offsets for each rail. The phase offset for each rail is indicated in the right-hand column of the table shown in **Figure 8** and is also shown graphically by the position of colored block. To change the phase offset of a rail, power designers simply have to left-click and drag the

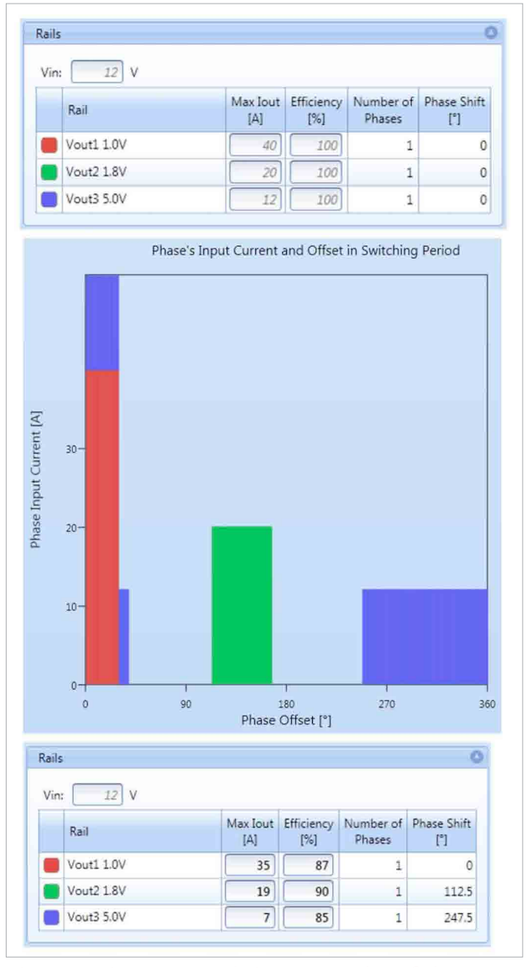

Figure 8: Ericsson Power designer screenshot of phase spreading interface

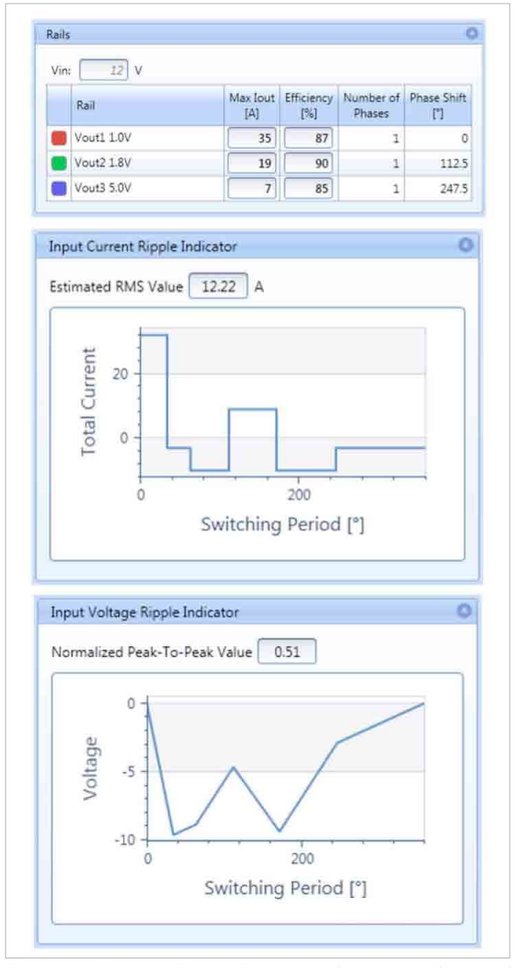

Figure 9: Ericsson Power Designer phase spreading and input current and input voltage ripple indicators

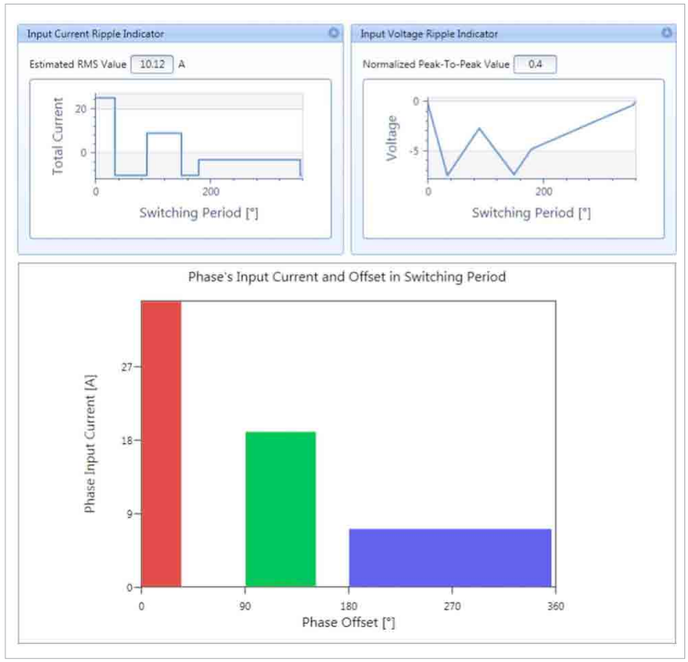

Figure 10: Automatic phase spreading representation

corresponding colored block to the desired phase offset position. In this example, phase offsets are distributed equally across the period at 0°, 112.5° and 247.5°.

Another interesting possibility offered by digital power and simulation tools is the visualization of input current and voltage ripple with the optimization of phase spreading (see **Figure 9**), making it possible to reduce the amount of filtering.

The Input Current Ripple Indicator provides an estimated RMS value of the total input current ripple of the rails, as well as a graph showing the variation of the total input current along the switching period. The target is a minimized RMS value, which means a 'smoothed' out input current. The Input Voltage Ripple Indicator provides a normalized peak-to-peak value of the total input voltage ripple of the rails, in addition to a graph showing the variation of the input voltage along the switching period. The normalized peak-to-peak value will be 1 in the case where all phases have zero phase offset. As offsets are introduced the peak-to-peak value will be reduced. The target is a minimized peak-to-peak value.

Optimizing phase spreading

Power designers have two possibilities: manual or automated optimization. In the case of a simple system without current-sharing rails, most of power designers will likely use the manual optimization, which follows the previously described sequence (left click and drag phases to the desired offsets) and visualize the result with the adjustment.

For more complex systems with current-sharing rails or a larger amount of rails, finding the optimized phase offsets manually may not be an easy task. With a single click on the 'Optimize' button, Ericsson Power Designer will automatically find an optimized configuration of phase offsets. Trying this on the example, a spread can be achieved with the same input current RMS value as in the manual optimization, but with a lower peak-to-peak input voltage ripple (see **Figure 10**). The increased offset difference between the higher current 1.0V and 1.8V rails affects the input voltage waveform, so that the normalized peak-to-peak value is reduced from 0.5 to 0.4.

Saving time-to-market

The example presented above clearly demonstrates the benefits that can be delivered by digital power when implemented in industrial applications, such as simplified design and shorter time-to-market. What is more, in demanding applications such as that shown in Figure 5, employing know-how and expertise in the field and implementing digital power at its best can result in a five-fold reduction in time-to-market.

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Digital power management without code qualification

There are many different styles of digital power management available

By: Frederik Dostal, Analog Devices

Digital power management has become more popular year over year, for multiple reasons. There are more semiconductors available to support digital power management, helping reduce the cost for such solutions. Another important reason for today's success of digital power management however, is the increased trust and better understanding of digital power management by power supply design engineers.

There are many different styles of digital power management available today, defined by how the digital functionality is implemented. Microcontrollers, microprocessors, DSPs and even FPGAs can be used. Within each 'style' there are products available which suit themselves to do digital power management. Devices are suitable if they have enough data crunching power and the right analog interfaces. Data crunching power is usually not difficult to find, analog interface ability however needs to be dedicated for the purpose of power supplies.

These interfaces include analog to digital converters (ADCs) as well as PWM generators. These have to be fast and accurate enough so that the power supply can operate with a stable control loop and so that it has an acceptable line and load transient response. Adding such analog interfaces to a digital core product with external, discrete ADCs is possible but usually quite expensive, space intensive and challenging to implement.

The difficulty lies in the fact that the selection of suitable components is difficult and requires power supply system knowledge as well as a good understanding of ADCs. A much simpler and often more optimized path is to select an integrated circuit dedicated for digital power management. Today a broad selection of such devices exists in the market.

Solutions with coding and code qualification

The group of available solutions requires the digital circuitry to be programmed by code. Often C code is used. Such coding allows for the greatest flexibility. Every possibility a designer would want to do can be implemented as long as the processing power of the digital circuitry and the analog interface permits it. This enormous flexibility comes at a certain cost. Programming knowledge is necessary. Usually power supply experts are not very experienced in programming code. Sometimes development teams consist of analog power supply experts as well as software experts. While such a development team setup may work well, very often there are difficulties with communication within the team. Often the software programmers do not know power management well enough to find suitable solutions quickly.

After code programming is completed, a rigorous testing procedure needs to be run. A stuck software routine or undefined states can be catastrophic in power supplies. Verification and also qualification of such software is time consuming, costly and requires experience. In many engineering fields such as automotive, military but also in industrial applications, any code modification will start a new cumbersome qualification process. These disadvantages limit such digital power management solutions to special cases where a highest degree of freedom is necessary and no standard solution is available

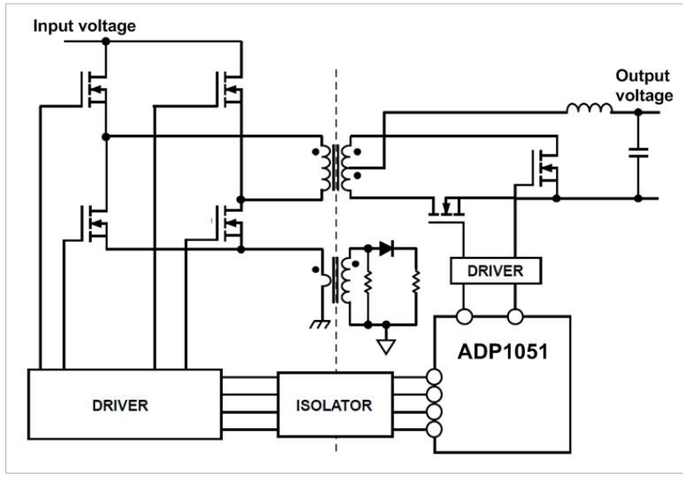

Figure 1: ADP1051 in a zero voltage switched isolated DC to DC conversion topology with synchronous rectification

Solutions without coding but with code qualification

Some vendors of digital power management integrated circuits help their customers in the design process by offering pre-programmed software tools. This can be coded IP generated specifically for power supply functions which is provided to the power supply design engineer. The designer can then combine some of these program modules and configure the complete solution. Such software support may also consist of graphical user interfaces (GUIs) that can be quite easy to use. These significantly help power supply designers to set the digital power supply to do what it needs to do. They perform the translation from the way power supply engineers think to how digital circuitry needs to be told what to do. While this is a valuable support vehicle, the outcome of such tools is software code after all.

With this approach the flexibility of the design engineer is somewhat limited. If the pre-programmed software tool does not allow a certain function, it cannot very easily be implemented. While the generation of the code has been simplified, still extensive tests need to be performed to make sure that the power supply will work reliably. Also the final code needs to undergo the rigorous qualification process as mentioned above.

Solution without coding and without code qualification

The third style of how digital power supplies can be build is a hardware-coded system based on a state machine controller IC. Such a system comes pre-configured. The influence a power supply designer has on the controller is reduced to setting registers in the state machine. While this limits the flexibility somewhat, most possible use cases have been considered, when the controller IC was designed so that most applications will work very well with such an integrated approach. Also these natural limits make it much easier and safer to work with this controller. If only a limited amount of 'adjust knobs' are available, checking for errors becomes simple.

Figure 1 shows a typical circuit with the ADP1051 fully integrated digital switching DC-to-DC controller IC based on a state machine. It is used in a full bridge topology intended for isolated DC-to-DC conversion of a few hundred Watts.

Graphical user interface and generated register settings

Figure 2 shows a screenshot of the graphical user interface (GUI) of the ADP1051. While an I^2C data stream may set the register settings of the state machine, such a GUI significantly simplifies the process. On different screens,

Figure 2: Screenshot of graphical user interface for digital DC to DC controller based on state machine

all the possible settings can easily be made. In a spy window the user has full visibility of the data flow in between the GUI and the controller chip. The specific screenshot in **Figure 2** shows the setting of the compensation of the control loop as an example. Poles and zeros can be relocated by the click of a mouse button. Different compensation schemes for different operating conditions are possible.

Details about typical designs

The circuit shown in **Figure 1** uses an ADP1051 controller from Analog Devices for a full bridge DC-to-DC conversion. Other typical applications are half bridge, two switch forward, and active clamp forward topologies. Even LLC resonant mode is supported by these controllers. For non-isolated power supplies, the new ADP1055 can be used in interleaved synchronous buck regulators for highest flexibility.

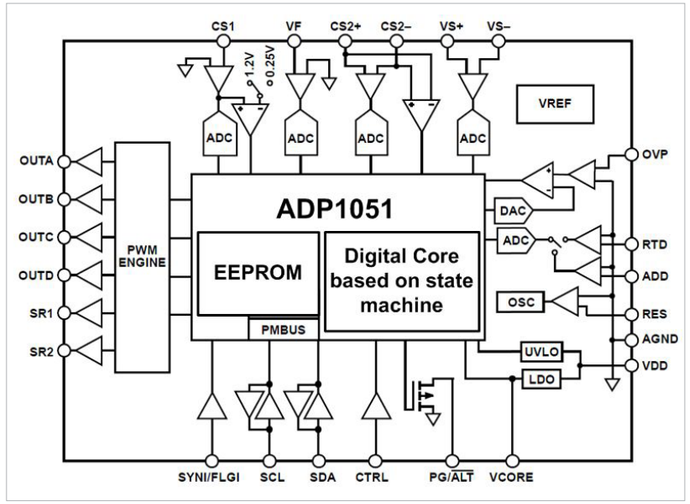

Figure 3: Integration of the analog interfaces with the digital controller core

Further available controllers using the same concept are the ADP1047 / ADP1048 for power factor correction (PFC) applications.

All these solutions offer I²C or even PM-bus interfaces. These are used to dynamically read information about fault states or real time information about voltages and currents in the system. The digital interface is also used to set and reset certain register values. For easy design, all of the state machine controllers include an EEPROM that stores the register values. This enables simple start-up of the circuitry. A few of the EEPROM bytes can even be used for external data such as a system operation hour counters. An external flash memory or additional EEPROM is not necessary.

The integrated ADC and PWM generators are optimized for the usage in power supplies. The output voltage is sensed with both, a very fast ADC for best regulation loop bandwidth but also a very accurate ADC for good DC accuracy. The result of both ADCs is then combined in the digital domain. The power supply designer does not have to worry about these functional blocks. **Figure 3** shows the integration of carefully selected analog circuitry and how it is combined with an EEPROM and digital control circuitry based on a state machine.

Specific advantages in industrial power supplies

Digital power supplies are especially common in telecommunications infrastructure applications. Already years ago, the many unique functions and features of digital power supplies offered clear system value. In Industrial power supplies, we are still at the beginning of the deployment curve. The drivers are machine-to-machine communication and the desire to communicate the status and conditions of the power supply itself as well as the quality of the generated bus voltages and the quality of incoming AC or DC voltages. Efficiency demands and reliability concerns are also a strong driver for digital power management in industrial applications. Digital power controllers based on a state machine offer ease of use and a low investment threshold to make it all happen.

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Optimizing Rack Power Distribution with Advanced PDUs

Peak operating efficiency and reliability are necessities

By: Joe Skorjanec, Eaton

In today's information-driven business landscape, enterprises across the globe have become increasingly dependent on data centers as the foundation for successful operations. For mission critical environments, peak operating efficiency and reliability are necessities; if the data center falters, the business suffers as a result.

Figure 1: Advanced rack power distribution units (PDUs) can monitor every aspect of power

Maintaining data center uptime is more vital to businesses today than ever before, and operators need to monitor every piece of power-drawing equipment in the data center with high accuracy and preciseness. For enterprise and multi-tenant data centers alike, the ability to stay up and running requires advanced rack power distribution units (PDUs) that can monitor every aspect of power and enable the management of power distribution (see **Figure 1**). Without these technologies, data centers are at risk of being unable to keep up with the ever-expanding business requirements.

What Influences Modern Data Centers?

Today's data center is under intense pressure in many regards. While information is increasingly important to organizations across every industry, which is reflected by an exponential growth in data volume, data center operating budgets aren't keeping pace. With more demands and stagnant budgets, data centers must operate more efficiently. In this environment, data centers face the burden of operating with energy efficiency and reducing downtime as much as possible.

At the same time, virtualization – with its promise to deliver better utilization – is creating a heightened need for flexibility throughout and among data centers. This requirement is further reinforced by the rising use of cloud-based solutions and co-located data centers, which in turn is driving the need for higher accuracy in billing – often down to the single-outlet level in a rack.

In addition, data centers are increasingly implementing converged infrastructure environments, which include integrated storage, server and networking technologies all made possible by virtualization. With converged infrastructure platforms, data centers are equipped to meet the on-demand computing challenges of today's businesses – providing they can manage the fluctuating power distribution requirements that such challenges entail. Altogether, these demands are motivating data centers to closely manage every facet of operations to ensure efficiency.

Figure 2: Rack capacity is used to select the appropriate input plug for the rack PDU

In effect, today's data centers function much like utilities, providing computing capacity in response to changing demands. Certainly, high-level power distribution strategies are needed for peak efficiency, yet data centers must go beyond a big-picture view of operations. Facilities that are contending with a variety of pressure-inducing factors must keep a watchful eye on all aspects of power distribution. A new generation of advanced rack PDUs – devices with monitoring and management capabilities – offer data centers comprehensive functionality that addresses their most pressing operational needs.

How to Plan for Capacity

The process of selecting a rack PDU should begin with the power rating of the unit and the technologies the data center requires. When designing a data center, operators typically take into account the planned capacity of the rack to calculate power and cooling requirements. Rack capacity is then used to select the appropriate input plug for the rack PDU (see **Figure 2**).

Data centers today often want a unit capable of carrying the full power load as well as accommodating the possibility for expansion, so they allow for extra capacity. When such future-proofing is pursued, any excess capacity that is being provisioned can be handled seamlessly by simply implementing a larger capacity PDU.

On a high level, data centers can also implement environmental technologies such as airflow management solutions, including aisle containment doors and ceilings, blanking panels and data center cages for secure partitioning. Additionally, data centers can deploy UPS solutions to improve efficiency and reduce power costs without compromising protection. Busways with plug-in configurations can flexibly connect power to server cabinets with the capacity to meet high power demands as well.

Evaluating Advanced Technologies

Once the power rating and capacity of the unit is considered, data centers should next assess technology and applications. Typically, rack PDUs come in three categories: basic distribution, metered distribution and managed or switched distribution. Moving up the stack from basic to metered will allow data centers the ability to locally measure current and load balance – not to mention the capability to remotely monitor branch circuits and facilitate capacity planning.

With advanced meters, data centers gain the capability to meter power at the outlet level. Outlet-level metering also provides a level of detail in reporting power usage that is often required in multi-tenant racks at co-located data centers. In addition, managed

PDUs facilitate outlet switching, an ideal capability for lights-out data centers or in situations where fast response to remotely cycle power in the rack is needed.

With outlet switching, data centers can also turn off outlets when not in use, thereby preventing accidental overloading of the rack PDU. Finally, outlet switching enables data centers to sequence power up and perform load shedding – both innovative features that can be important elements of an overall power strategy.

Data center operators can further enhance power distribution with the use of cables and accessories that deliver outlet and section current information, thereby improving both management and troubleshooting. With the addition of power management software, data centers can keep operations efficiently running with comprehensive services that include technical expertise for all products that are designed to improve costs, uptime, reliability, power quality and an expansive, 24 /7 support network.

As computing demands continue to increase, modern data center mangers must examine power distribution at a granular level with enhanced capabilities in mind. With virtualization and converged infrastructure, computing capacity is dynamic – workloads, applications and storage are moved around both within and among data centers as business needs dictate.

Advanced rack PDUs have the features and reliability today's data centers need to maintain their own operations, but more importantly to support the changing and accelerating demands of the business. Businesses would be wise to develop their power strategy by understanding the current rack environment and workload demands, followed by choosing an optimized rack PDU.

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SPECIAL REPORT : POWERING INDUSTRIAL APPLICATIONS

HV underground cable aids substation expansions with space constraints

The turnkey approach can be ideal for ensuring a successful project

By: Peter Ebersold, Marmon Utility

Substation expansions can become extremely complicated when space is limited. That's when use of high voltage underground cable comes into its own as a viable option. What makes the option even more favorable is a turnkey approach, in which the high voltage underground cable provider provides the cable, terminations, and testing and documentation.

Figure 1: Big Tree Substation

At a recent substation expansion project located near Buffalo, NY, where expansion of a substation yard and extension of an overhead 115 kV bus was impracticable and relocating facilities within the substation was impractical, Seymour, CT-based Kerite Company provided turnkey underground cable installation services that allowed new capacitor banks to be installed and energized in a reasonable amount of time and for reasonable cost.

Buffalo area project required novel solution

NYSEG, a subsidiary of Iberdrola USA, needed to add capacitor banks to improve the electrical system to handle load growth in the Buffalo NY area. The utility, which serves 877,000 electricity customers and 261,000 natural gas customers across more than 40 percent of upstate New York, chose to install two new 115 kV, 25 MVAR switched capacitor banks at Big Tree Substation, an older facility constructed in the 1940s. The substation feeds the Ralph Wilson Stadium, home of the Buffalo Bills, and new capacitor banks were important for ensuring overall system improvements and supporting system voltage in the area (see **Figure 1**).

Consulting engineers Laramore, Douglass and Popham were brought in to design the project. The company provides engineering for investor-owned and cooperative utilities, and works on everything from wind farms to industrial clients. Senior substation engineer Stan Bail

Figure 2: Underground cable transmission lines

explains that, while the Big Tree Substation seemed large, it was actually impossible to add both banks above ground as is commonly done with substation expansions. There was a wide-open space on the south side, but the north side was very close to a fence, with a house just outside the fence. "We came to the conclusion that the banks had to be underground because transmission lines were in the way," said Bail. "We couldn't place the capacitor banks off the existing bus, because it was 35 feet in the air and there was no room to place the capacitor banks under the existing structure."

According to Bail, they had room within the substation fence if they could have gotten the overhead wire bus extended to the area where the capacitor banks would fit. The issue was that NYSEG needed two capacitor banks and two breakers. Since the bus was split, with one on the north end and one on the south end, the best solution would be taking the two locations from overhead to underground. They then ran the underground cable, coming up at one central location, terminating the underground cable and connecting to two different circuit breakers and two different capacitor banks. The solution was an uncommon one for a substation; underground cable transmission lines are more frequently used when an airport is nearby and it is important to keep circuits from interfering with airport operations (see **Figure 2**).

After deciding on the engineering approach, Bail began looking for a company that could supply the cable, terminations, and testing components. He consulted with the client about their existing relationships with suppliers of high voltage underground cable, and then began discussions with Kerite, a Seymour, CT-based firm that had a reputation for high quality high voltage underground cable and a great deal of recent installation experience. After talking with Ed Sleight, Northeast Sales VP for Kerite, he decided that Kerite was a good fit. "I explained the substation project and found it was a perfect match – we needed high voltage underground cable and they had services to provide."

Turnkey approach selected for cable runs

The design included a conduit system to facilitate cable pulling from the bus area to the capacitor bank, including a conduit plan showing how and where to place the 6-inch PVC conduit, with one conduit per cable per phase. After the conduit system was installed, Kerite brought the cable to the site for electrical subcontractor Northline Utilities to do the cable pulls. Instead of working with one large 1300 foot reel, Kerite cut each run individually to length on smaller reels, which are easier to store and make pulling the individual runs much faster and simpler. This allowed the subcontractor the flexibility of pulling one phase and leaving it if necessary, then returning the next morning to pull the next phase.

The north end connection cable was about 275 feet, while the south bus connection underground cable link was approximately 150 feet. Each end of the connections requires three terminations (one for each phase), so there were a total of 12 terminations at the substation. The terminations for the end of the Kerite cable are 6.5 feet tall and each termination takes approximately eight hours to complete. Because of the complexity of the project, Bail was especially attracted by the turnkey installation services Kerite offered, including supplying the cable, doing the terminations, and conducting the testing. The testing included both high voltage DC high potential testing at the factory to ensure that there were no defects, and additional lower voltage field-testing.

"There was a great deal of cooperation between Kerite and Northline Utilities onsite," said Bail. "When you are terminating cables it is extremely important to avoid any wet conditions. Each one of the terminations took hours of sanding and dressing the cable after it was pulled, and Kerite needed a shelter to keep the wind, mist and rain off while doing the terminations. Northline built a shelter to keep them dry so they could keep working through whatever conditions the weather threw out there."

He adds that he plans to use Kerite for another capacitor bank in the Rochester, NY area, where underground cable is needed because there is no space to expand the substation. "When you are limited by space, underground high voltage cable is a viable option when compared to other more expensive substation expansion alternatives."

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Powering low-voltage devices from an intermediate-bus voltage

Take care creating your overvoltage risk mitigation plan

By: Willie Chan & Jason Sekanina, Linear Technology

Intermediate bus voltages from 24V to 28V (nominal) are commonplace in industrial, aerospace and defense systems, where series-connected batteries may be a backup power source and 12V bus architectures tend to be impractical due to distribution losses. The widening voltage gap between the system bus and the power inputs of digital processors present design challenges relating to power delivery, safety and solution size.

If a single-stage non-isolated step-down DC/DC converter is used, it must operate with extremely accurate PFM/PWM timing. Input surge events put further stress on the DC/DC converter, presenting another overvoltage risk to the load. Erroneous or counterfeit capacitors introduced in manufacturing may cause output voltage excursions exceeding the load's ratings potentially causing the FPGA, ASIC or microprocessor to ignite. Depending on the extent of the damage, the root cause may be quite challenging to determine and the resulting high repair costs, downtime and harm to reputation extremely frustrating.

Therefore, an overvoltage risk mitigation plan should be given careful consideration to minimize cost and inconvenience to customers. Traditional overvoltage protection schemes involving a fuse are not suitable for protecting modern FPGAs, ASICs and microprocessors, particularly when the upstream voltage rail is 24V or 28V nominal. A new solution has been created, combining a 38V-rated, 10A DC/DC switching regulator with circuitry to defend against many faults, including output overvoltage. Power and protection for today's most advanced digital logic devices are now available in one compact device.

Importance of accurate switcher timing

When a wide differential exists between the input voltage and the desired output voltage, switching DC/DC regulators are favored for their high efficiency. To achieve a small solution size, a non-isolated step-down switching converter is an obvious choice, operating at high enough frequency to shrink the size requirements of its power magnetics and filter capacitors. However, such a DC/DC switching converter must operate at narrow duty-cycles as low as 3%, which demands accurate PWM/PFM timing. Furthermore, tight voltage regulation is required by digital processors and fast transient response is needed to keep the voltage within safe limits. At higher input voltages, the margin for error in the on-time of the top side switch of the DC/DC regulator is reduced.

Bus voltage surges, which are often present in aerospace and defense applications, pose a danger not only to the DC/DC converter but to the load, as well. The DC/DC converter must be rated to regulate through the overvoltage surge with a fast control loop, so that sufficient line rejection is achieved. If the DC/DC converter fails to regulate or survive the bus surge, an overvoltage will be presented to the load. Overvoltage faults may also be introduced as the load's bypass capacitors degrade with age and temperature, which results in looser transient load response over the course of the end product's life.

If the capacitors degrade beyond the limits of the control loop's design, the load can be exposed to overvoltage by two possible mechanisms. First, even if the control loop remains stable, heavy transient load-step events will demonstrate higher voltage excursions than were expected at the onset of design. Second, if the control loop becomes conditionally stable (or, worse yet, unstable), the output voltage can oscillate with peaks exceeding acceptable limits. Capacitors can also degrade unexpectedly or prematurely when an incorrect dielectric material is used, or when fake components enter the manufacturing flow.

Cheap counterfeits can cause costly headaches

Gray market or black market, the attractive cost of counterfeit components can prove to be too enticing for some to resist, even though they don't meet the standards of the genuine article (e.g., they may be recycled, reclaimed from electronic waste, or built from inferior materials). A short-term savings becomes a huge expense when a counterfeit product fails. Counterfeit capacitors, for example, can fail in a number of ways. Counterfeit tantalum capacitors have been seen to suffer internal self-heating with a positive-feedback mechanism to the point of reaching thermal runaway. Counterfeit ceramic capacitors may contain compromised or inferior dielectric material, resulting in an accelerated loss of capacitance with age or at elevated operating temperatures. When capacitors fail catastrophically or degrade in value to induce control loop instability, the voltage waveforms can become much greater in amplitude than originally designed, endangering the load.

Risk mitigation planning

Any risk mitigation plan should consider how the system would respond to and recover from an overvoltage condition. Is the possibility of smoke or fire resulting from an overvoltage fault acceptable? Would efforts to determine root cause and implement corrective actions be hampered by damage resulting from an overvoltage fault? If a local operator were to power-cycle (reboot) a compromised system, would even greater harm to the system result further hindering recovery efforts? What is the process and time required to determine the cause of the fault and resume normal system operation?

Inadequacies of traditional protection circuits

A traditional overvoltage protection scheme consists of a fuse, silicon controlled rectifier (SCR), and Zener diode. This circuit (Figure 1) protects the load in the following manner. If the input supply voltage exceeds the Zener breakdown voltage, the SCR activates, drawing sufficient current to blow open the upstream fuse. It is relatively simple and inexpensive, however drawbacks of this approach include accuracy of the Zener diode breakdown voltage, SCR gate trigger threshold variation, varying response time of the SCR and fuse and the level of effort required to recover from a fault (i.e. physically servicing the fuse and restarting the system).

If the voltage rail under consideration powers the digital core, the SCR's protection capability is limited since the forward drop at high currents

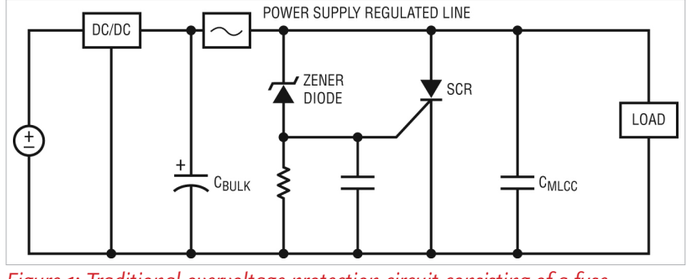


Figure 1: Traditional overvoltage protection circuit consisting of a fuse, SCR and Zener diode.

is comparable to or above the core voltage of the latest digital processors. Because of these drawbacks, the traditional overvoltage protection scheme is not suitable for high voltage to low voltage DC/DC conversion powering loads such as ASICs or FPGAs that could be valued in the hundreds if not thousands dollars.

While inexpensive, this circuit's response time is insufficient to reliably protect the latest digital circuits particularly when the upstream supply rail is an intermediate voltage bus. Moreover, even the simplest recovery from an overvoltage fault is invasive and time consuming (see **Figure 1**).

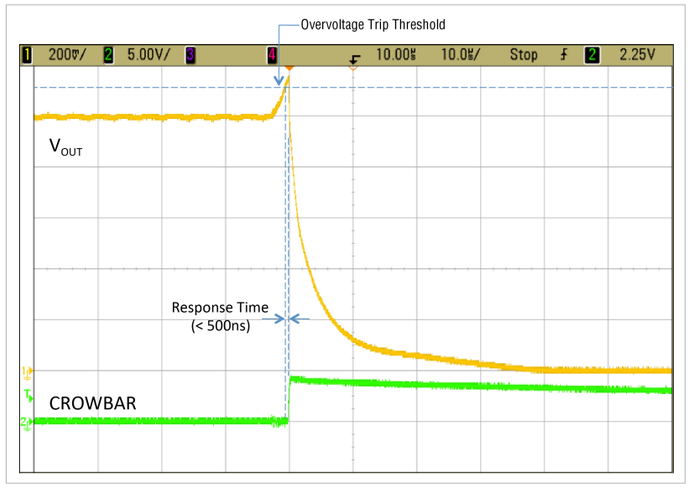


Figure 2: The LTM4641 responds to an overvoltage condition within 500ns protecting the load from voltage stress. (VIN = 38V, VOUT = 1.0V, adjustable overvoltage trip threshold set at +11%)

An innovation combining power & protection

A better solution would be to accurately detect an imminent overvoltage condition and respond by quickly disconnecting the input supply while discharging excess voltage at the load with a low impedance path, like the protection features included within the LTM4641 step-down µModule regulator. At the heart of the device is a 38V-rated, 10A step-down regulator with the inductor, control IC, power switches and compensation all contained in one surface mount package.

To add a level of protection for high value loads such as ASICs, FPGAs and microprocessors, an extensive level of monitoring and protection circuitry is included. The LTM4641 maintains a constant watch for input undervoltage, input overvoltage, overtemperature and output overvoltage and overcurrent conditions and acts appropriately to protect the load. To avoid false or premature execution of the protection features, each of these monitored parameters has built-in glitch immunity and user adjustable trigger thresholds with the exception of overcurrent protection, which is implemented reliably, cycle-by-cycle with current-mode control. In the case of an output overvoltage condition, the LTM4641 reacts within 500ns of fault detection (see **Figure 2**).

Not only does the internal architecture of the LTM4641 allow it to respond nimbly and reliably, it can even automatically reset and rearm itself after fault conditions have subsided. A differential sense amplifier is employed to regulate the voltage at the load's power terminals, minimizing errors stemming from common-mode noise and PCB trace voltage drops between the LTM4641 and the load. The DC voltage at the load is regulated to better than ±1.5% accuracy over line, load and temperature. This accurate output voltage measurement is also fed to the fast output overvoltage comparator, which triggers the LTM4641's protection features.

When an overvoltage condition is detected, the µModule regulator rapidly takes multiple courses of action, simultaneously. An external MOSFET (MSP in **Figure 3**) disconnects the input supply, removing the high voltage path from the regulator and the high-value load. Another external MOSFET (MCB in **Figure 3**) implements a low impedance crowbar function, quickly discharging the load's bypass capacitors (C in **Figure 3**).

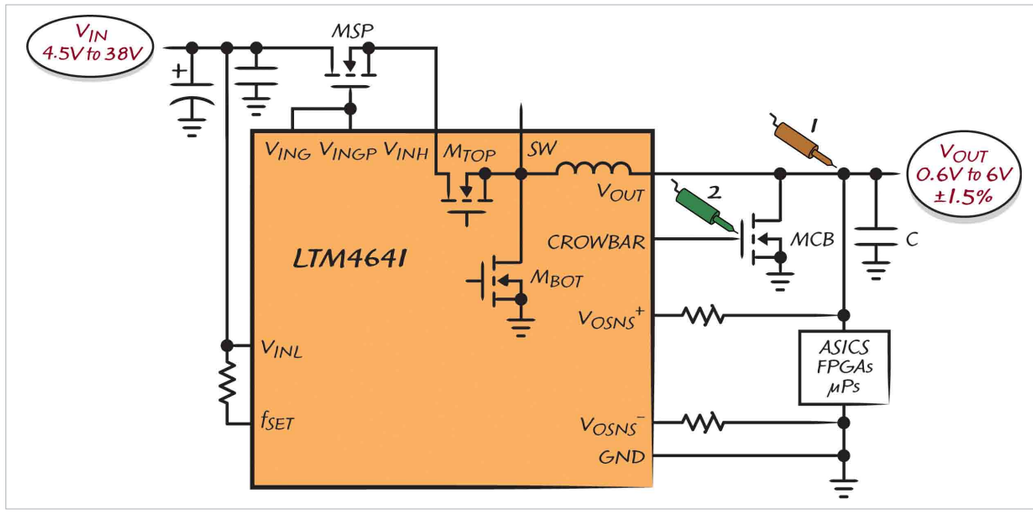


Figure 3: LTM4641 output overvoltage protection plan. The two probe icons correspond with the waveforms in Figure 2.

The DC/DC step-down regulator within the LTM4641 enters a latched-off shutdown state and issues a fault signal indicated by the HYST pin which can be used by the system to initiate a well managed shutdown sequence and/or system reset. A dedicated voltage reference independent of the control loop's reference voltage is used to detect fault conditions. This provides

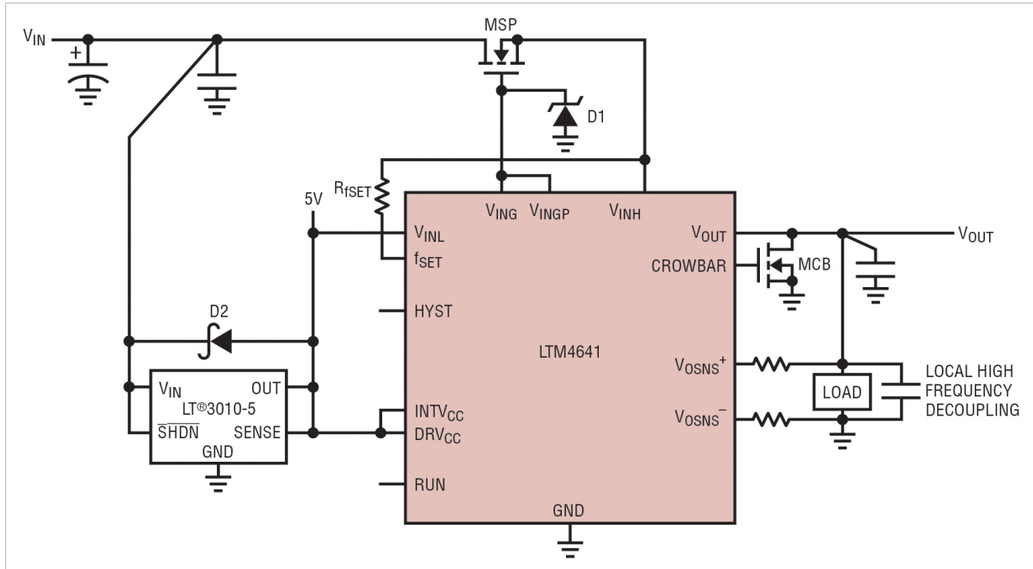


Figure 4: Input surge protection up to 80V, using the LTM4641 & external LDO

resilience against a single-point failure, should the control loop's reference happen to fail.

The improvement in protection offered by the LTM4641 over the traditional fuse/SCR protection scheme is further bolstered by how the system recovers from a fault. In the traditional overvoltage protection scheme, a fuse is relied upon to separate the power supply from the high value load. Therefore, someone must physically be present to remove and replace the fuse in order for the system to resume normal operation after a fault has occurred. In contrast, the LTM4641 can resume normal operation quickly once the fault condition has cleared either by toggling a logic level control pin or by configuring the LTM4641 for autonomous restart after a user specified timeout period expires. No components need to be physically replaced, which is a critical requirement for systems with high uptime requirements and/or operating in remote locations. If fault conditions reappear after the LTM4641 resumes operation, the aforementioned protections immediately engage to again protect the load.

Input Surge Protection

In some cases, output overvoltage protection alone is insufficient, and input overvoltage protection is desired. The LTM4641's protection circuitry can monitor the input voltage and activate its protection features, should a user-configured voltage threshold be exceeded. If the anticipated maximum input voltage exceeds the 38V rating of the module, input surge protection can be extended up to 80V with the LTM4641 still fully operational by adding an external high voltage LDO, which keeps control and protection circuitry alive (**see Figure 4**).

Conclusion

With market requirements for higher system performance and uptime coupled with the tremendous expense of the latest digital processors, engineers must consider risk mitigation strategies, particularly when a distributed power bus in range of 12V-28V or those with surges are involved. The latest and often very costly FPGAs, ASICs, and microprocessors have supply voltages with a maximum limit as low as 3% - 10% of the intermediate voltage rail, which makes them extremely susceptible to damage, potentially even igniting from an overvoltage fault. Such faults might be caused by timing errors in the switching regulator, an input voltage surge or improper components introduced during manufacture.

www.linear.com

Acknowledgements:
Afshin Odabaee & Yan Liang, Linear Technology

Don't forget the main reason to migrate to green tech is a green planet

By: Alix Paultre, Editorial Director, PSD

With all the debate about the development of green and renewable tech and its integration into the marketplace, we often forget the primary reason we do this: to save our ecosystems and ourselves. Green technology isn't just a novel way to generate power and save money; it is a vital development to save humanity from itself.

Big blue marble

Most of us, regardless of ideology or faith, can agree that this planet is the only one we will ever have to live on. Even if we develop colonies in other star systems in the far future, 99.9% of humanity will still have to live here. This planet is a closed environment that we cannot replace for another copy if something goes wrong. Pollution and environmental destruction due to fossil-fuel extraction, processing, transport, storage, and use is a daily reality.

This is not to say that alternate energy and green tech will ever completely replace fossil fuels in power systems, however these technologies and processes do expand the palette of system solutions, leaving fossil fuels to the applications requiring that level of energy density. The number of devices and applications that can be served by systems driven by renewable or harvested power systems are growing daily.

Green also means money

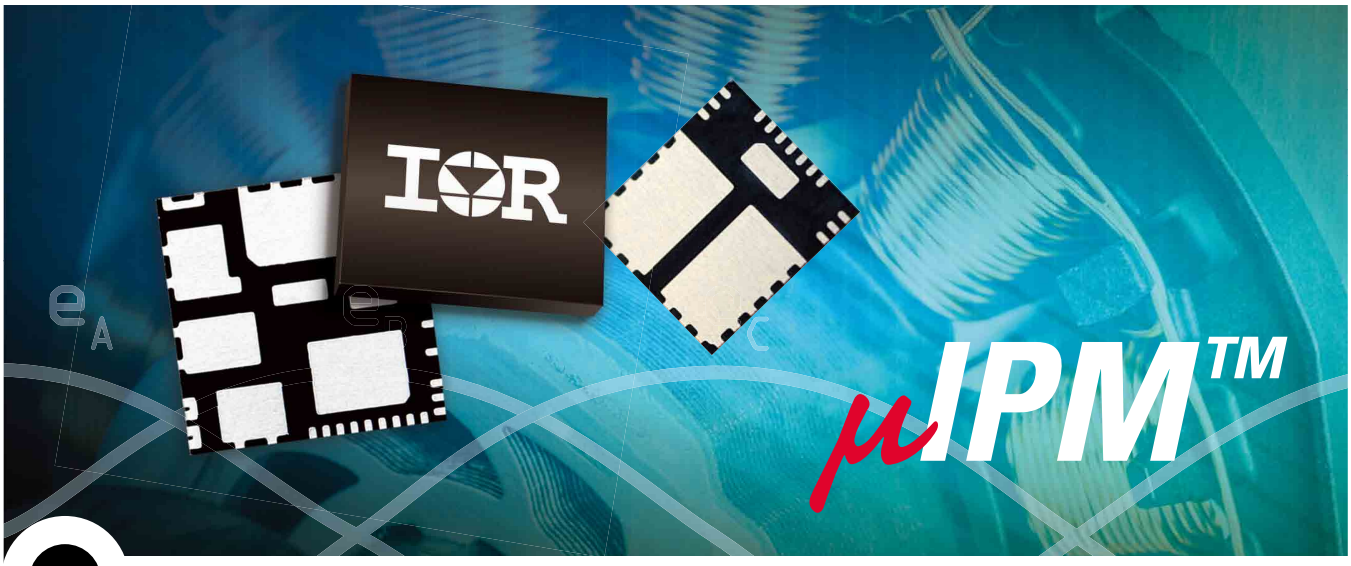
Hybrid industrial systems using harvested energy for sensors and controllers with fossil-fuel energy saved for the process itself can not only save energy, they can economically extend the utility of legacy systems by integrating advanced oversight and command for significantly improved efficiency. Not only do such systems save energy and money, more efficient industrial processes have less waste and impact on their environment.

These savings propagate throughout society. The factory that uses less power reduces the load on the municipal grid, and one that uses fewer raw materials frees up capital for investment in the company. In addition, a facility that is more efficient in its daily business can direct more energy toward R&D efforts. A cost-effective company can compete in the marketplace and provide its community with jobs and taxes.

Next –gen tech saves

Not only does every advance in system efficiency and process technology reduce the environmental impact of the product created, solid-state technologies tend to use significantly fewer materials than the analog devices they replace. For example, 32-inch flatscreen TV uses a fraction of the materials a 32-inch CRT did, reducing component inventory, shipping requirements, and eventual cost as the technology matured. This applies to the manufacturing floor in things like smaller pick-and-place machines, control terminals, inspection stations, and robots.

www.powersystemsdesign.com



Innovative Power Module Reduces System Size

µIPM™ Power Modules Deliver up to 60% Smaller Footprint

Specifications:

Part Number	Size (mm)	Voltage	IO (DC@ 25°C)	Motor Current**		Motor Power VO=150/75VRMS	Topology
				w/o HS	w/HS		
IRSM836-024MA	12x12	250V	2A	470mA	550mA	60W/72W	3P Open Source
IRSM836-044MA	12x12	250V	4A	750mA	850mA	95W/110W	3P Open Source
IRSM836-025MA	12x12	500V	2A	360mA	440mA	93W/114W	3P Open Source
IRSM836-035MB	12x12	500V	3A	420mA	510mA	108W/135W	3P Common Source
IRSM836-035MA	12x12	500V	3A	420mA	510mA	100W/130W	3P Open Source
IRSM836-045MA	12x12	500V	4A	550mA	750mA	145W/195W	3P Open Source
IRSM808-105MH	8x9	500V	10A	1.1A	1.3A	285W/390W	Half-Bridge
IRSM807-105MH	8x9	500V	10A	1.1A	1.3A	285W/390W	Half-Bridge

Features:

- Integrated Gate Driver IC
- Compact PQFN package offers up to 60% smaller footprint
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- DC current ratings from 2A to 10A
- Voltage range of 250V – 500V

***µIPM*™ Advantages:**

- Shortens design time
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- Simplicity - Eliminates Heat Sink
- Replaces more than 20 discrete parts to deliver a complete motor drive stage
- Slashes assembly time and cost
- Simplifies procurement and inventory management
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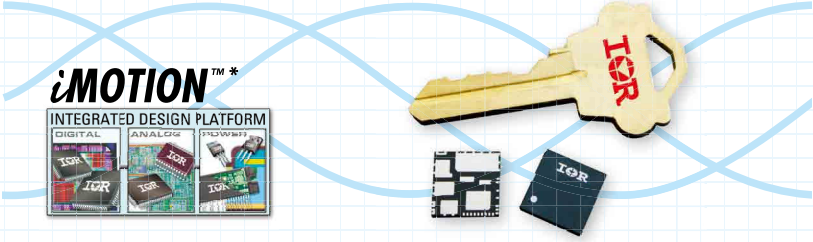

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