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May 2018



Special Report: High Bandwidth Semiconductors + Packaging Technologies (pg 19)



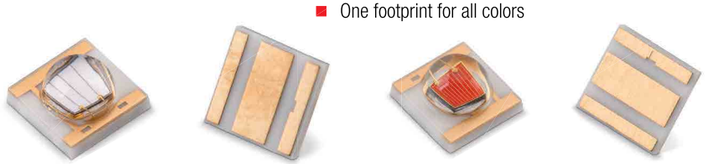
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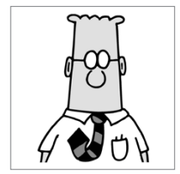


COVER STORY
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Volume 15, Issue 4



It's All About Materials

Welcome to the May edition of PSD. This year seems to be constantly busy and the time is flying in. Maybe it is because the industry is on the crest of a wave at the moment, or it may be that the number of important events is increasing and we are constantly in the lead up to another one. This month, we start to look at the premier European event for the power industry, PCIM.

As legislation demands products become even more efficient, more industries are looking to power designers to provide the solution. This has led to power being showcased in vertical events more frequently. Exhibitions, such as Medtech now feature power supply manufacturers extensively, and Europe's largest industrial fair, Hannover Messe, even has it's own power technical stream. SPS IPC Drives Expo in Nuremberg last November also had a large amount of power supply manufacturers exhibiting.

Even events that focus on other areas of electronics often have a growing list of power manufacturers attending. For example, Embedded World had a noticeable jump in the number of power manufacturers taking up stands. No matter how important other shows become, PCIM is the one place where power companies come to show off their true innovation in the field, months and years before those innovations find their way into the product halls at Embedded World or Hanover. Much like the APEC exhibition earlier this year in Texas, PCIM's innovation will include a huge focus on wide-bandgap materials and packaging technologies.

That is one reason we have chosen those topics to be the main theme of the magazine this month. Materials such as GaN and SiC have started a revolution in the power industry. The original theory behind those materials' properties had been discovered decades ago. Putting that theory into practice started much more recently, around 15 years ago. That research and development is now coming to fruition as techniques are refined and we tease every drop of performance out of wide-bandgap materials. Patrick Le Fevre of Powerbox was working on advanced materials at the start of the practical development and was also at APEC in March. In the issue he talks about how the technologies have developed over the last decade and a half to get to where we are today.

Another article on the topic this month is from UnitedSiC. There's no doubt of the benefits offered by SiC technology, especially in power conversion circuits. However, to gain these benefits usually requires a full redesign of the product, which is not practical be for many companies. UnitedSiC takes a different approach, offering designers drop-in SiC replacements that allow access to many of the benefits of the material. Read more about that technology inside.

And if you do attend PCIM this year, don't forget that PSD will be running a round table at the event on 12 pm on Tuesday. The discussion will focus on the future of the industry. It would be great if you could join us there.

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Best Regards,

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ROHM Semiconductor Opens Test Lab for Power Components

ROHM Semiconductor has opened its new European Power Lab in the company's European Headquarter facilities at Willich-Münchheide, near Dusseldorf. The investment in the new facility demonstrates Rohm's commitment to the region it sees as one of the most important areas globally for power devices. The state-of-the-art lab will also assure customers of Rohm's commitment to quality and high standards and provide a higher level of support.



The lab is intended to analyze the capabilities to Rohm's power components and systems and provide the company's customers with application-level support. Measuring 300m², the lab contains several bespoke test benches and a separate test area for high-voltage testing. Due to a lack of suitable test benches on the open market, Rohm specified, developed and designed the benches to its own requirements. Developing the test benches internally also has the benefit of being inherently flexible and scalable to cope with the changing demands of the market.

The lab is equipped with the latest technologies, which feature a strong emphasis on safety. This equipment allows Rohm to electrically characterize all of its semiconductor components, including SiC MOSFET transistors, SiC diodes, IGBTs, Si power MOSFET transistors and gate drivers.

Currently installed in the lab are a power bench, a calorimetric bench and a high voltage bench. The power test bench is intended to facilitate the testing of AC/DC, DC/DC, DC/AC and AC/AC converters under real application conditions up to 15kVA. Power analyzers take high precision measurements of the efficiencies and losses of the objects under test. The test bench's features include an AC power supply that can emulate different power grid conditions, and both AC and DC electronic loads. The power bench can test voltages up to 1500VDC and 400VAC.

The calorimetric test bench analyzes the thermal behaviour of discrete power devices, modules, electronic boards and complete power systems. This test bench can test at currents of up to hundreds of Amps and has a climatic chamber for tests under temperature conditions ranging from -40°C to +180°C and humidity between 10 and 98%.

The high voltage test bench can produce voltages up to 8000V and is located in a separate room for safety. The bench can also be used to investigate and test insulation clearance and creepage distances on boards and systems using voltages of up to 6000V.

Christian André, President ROHM Europe, said, "This investment shows our determination to be one of the major suppliers in SiC and Si Power discrete and integrated device technologies, and to play an important role in the growing power market. The new Power Lab is the centrepiece of our quality and reliability scheme".

ROHM Europe
http://www.rohm.com/eu



Wide Bandgap Semiconductors and Packaging

By: Kevin Parmenter, PSD Contributor

It's forward thinking and necessary to have the terms "wide bandgap semiconductors" and "packaging" in the same sentence. Several years ago, I was involved in the emerging stages of wide bandgap semiconductor devices. In a meeting I mentioned that device success in the marketplace required a focus on building a supporting ecology and innovation in packaging technology. This of course did not fit the belief that we could put next century technology in 1980's packages without optimized drivers or controller schemes and expect quick success and returns in a single quarter.

Fast forward to where we are today, and what was needed is now occurring. The GaN and Silicon Carbide suppliers are innovating from the pins in, providing incredible technologies that inch us closer to the ideal switch. Frequencies and performance can be increased to unheard of levels. The parasitic capacitances inherent in all semiconductor switches are drastically lowered, making devices easier to drive. Early manufacturing issues have largely been solved – reliability promises to meet, if not exceed, that of silicon semiconductor devices, and every day semiconductor devices are made better and better - including competing silicon devices. The rate of improvement is just getting started, so watch for phenomenal innovations.

In addition to lower capacitances, GaN has no parasitic BJT and no body diode with zero reverse recovery. Increasing switching frequencies, better efficiency, lower losses, fewer parts – smaller filters, smaller heat sinks and enabling new topologies can translate into smaller, faster and lower total system cost. Silicon Carbide devices enable much of the same; however, higher voltages are routinely possible vs. silicon IGBT's and MOSFETS. It seems obvious that e-mode GaN devices are going to eclipse cascode devices based on customer preference and what's being used in new designs. Essentially, if you don't have e-mode, you better get it before it's too late.

From the pins out, packaging innovation and progress has been astounding – we see that power electronics design is now like RF power design so that the interconnections and PC Board become part of the circuit. We are now at chipscale levels, eliminating wire bonds and increasing performance and reliability with better EMI performance, improving thermal performance. It's clear this innovation was needed for the potential of wide bandgap semiconductors to be realized.

Regarding packaging, we're seeing the enviable of the needed drivers with impedance matching to the unique capabilities of wide bandgap devices, as well as the programmable digital control IC's needed to take advantage of switches. We'll see more co-packaging of these into modules with 3D packaging used, building out the ecology. We're also seeing the reference designs from semiconductor companies as required to accelerate the designs.

These are exciting times in the wide bandgap and power electronics industry for those embracing the challenges and can face the realities of the market needs by adapting, innovating and delivering on promises. It might even take some collaboration and investment in magnetics design.

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Active Bridge Rectifiers Reduce Heat Dissipation within PoE Security Cameras

By: Ryan Huff, PoE Applications Engineer, Analog Devices, Inc.

Power over Ethernet (PoE) has been embraced by the video surveillance industry as a solution to an age-old problem: complicated cabling. For instance, a basic, traditional fixed-view security camera requires two cables: one for power (10W to 15W from a 24V AC or 12V DC), and a separate, coax cable for the video signal. With PoE, a single Ethernet cable carries both video data and power. Everything is simplified. Right?

Not quite. To meet compatibility with existing systems, camera manufacturers must produce PoE-enabled cameras that are also compatible with legacy power sources—they must accept PoE 37V to 57V DC from an RJ-45 jack or 24V AC, +12V DC, or –12V DC from an auxiliary power connector.

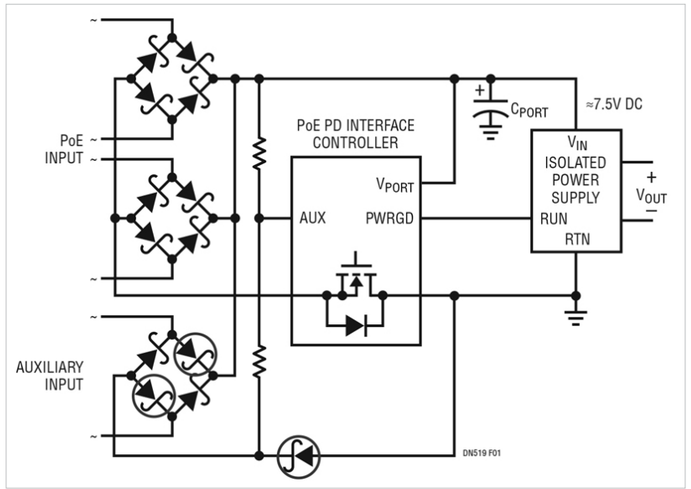


Figure 1: Auxiliary Input and PoE Power Architecture

The Old Way Loses Power

Figure 1 shows the power architecture used by many PoE camera manufacturers to solve this problem. A full-bridge diode rectifier after the auxiliary (old-school) input produces positive DC power from either 24V AC, +12V DC or –12V DC. The resulting DC power and the PoE inputs are diode-ORed with the winning supply fed to a wide input voltage isolated switching power supply, which in turn powers the camera electronics.

This power architecture presents a few challenges. When the camera is powered from the auxiliary input, three diodes (circled in Figure 1) fall into the power path. In addition to the inefficiency of this design and possible heat problems from the power dissipated by the diodes, the three diodes lead to a significant voltage drop at the input to the switching power supply. With a 10W to 15W camera, these challenges are easily surmountable, but the latest security cameras have doubled this power consumption. Features like pan/ tilt/zoom (PTZ) and camera lens heaters for outdoor operation have made this power architecture unsuitable for this new wave of cameras.

To illustrate the architecture's deficiencies, consider a 26W camera. For a 12V DC auxiliary input (assumed to actually be 9V DC due to use of unregulated wall warts/ AC adapters) and three 0.5V drop Schottky diodes, the input voltage of the switching power supply is 7.5V (9V – 3 • 0.5V). The input current for this camera is approximately 3.5A (26W/7.5V). The resultant power dissipation of the three Schottky diodes in the power path is 5.2W (3.5A • 3 • 0.5V). This power dissipation leads to higher temperature within the camera, which is difficult, time consuming and expensive to mitigate.

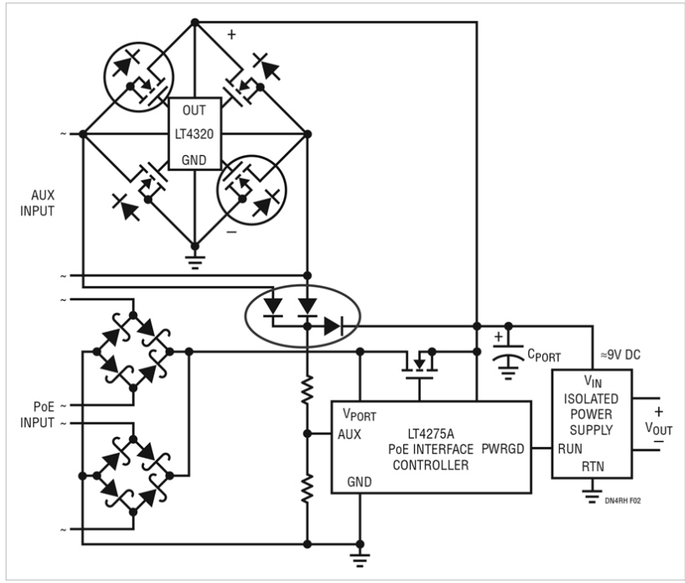


Figure 2: Improved Power Architecture with No Diode Drops in Power Path

Improve Performance with Ideal Diodes

Figure 2 shows a way to counter this shortcoming. Here, the two diodes of the full-bridge rectifier are replaced by ideal diodes, circled (black) in Figure 2. Ideal diodes are simply MOSFETs controlled to behave like regular diodes. The advantage of an ideal diode is that one can use MOSFETs with low channel resistance (RDS(ON)), thus reducing the forward voltage drop (IDS • RDS(ON)) to much less than a Schottky diode drop. The LT4320 ideal diode bridge controller enables the control of four MOSFETs in a full-bridge configuration. The third diode drop due to the diode-OR in Figure 1 is eliminated by the LT4275 LTPoE++™/PoE+/PoE PD controller. Its topology allows the use of a few small-signal diodes, circled together (red) in Figure 2, for auxiliary input sensing. These diodes are not in the power path as in the traditional architecture, so they do not contribute any additional voltage drop or heat issues.

Results

The power architecture shown in Figure 2 significantly reduces overall power losses when compared to that of Figure 1. To quantify, the LT4320 combined with low channel resistance MOSFETs results in a 20mV drop across each ideal diode bridge MOSFET. This produces an input at the isolated supply of 8.96V (9V – 2 • 20mV). The higher input voltage drops the required input current to only 2.9A (26W/8.96V) versus the original 3.5A.

The resulting power dissipation of the improved architecture is now a scant 116mW (2.9A • 2 • 20mV), versus 5.2W for the original architecture—a 45× reduction! Additionally, the lower input current further reduces power dissipation in the isolated power supply's power components (i.e., input filter inductor, power transformer and switching MOSFETs) due to the reduction of their I2R power losses. A simple calculation puts this reduction at 31% (100% – 2.9A2/3.5A2).

Conclusion

Adding the LT4320 and LT4275 to the auxiliary and PoE inputs of a PoE-enabled security camera recovers more than 5W (5.2W – 116mW) of power dissipation over traditional full-bridge/diode-OR designs. This reduction of power eases the thermal design time and complexity of PoE security cameras.

Analog Devices
www.analog.com

Advanced Packaging Methods for Modern Power Supplies

Innovative packaging improves cooling and thermal management

By: Stefan Preimel, Concept and Application Engineer, Infineon Technologies

No matter the technical innovation or application, all modern technologies have one thing in common; they rely on a reliable, small and high performance power supply to be able to function and meet their specification. As end products become more complex, the design parameters for the power supply become more challenging, generally requiring more power and more efficiency in an ever smaller space – and with rising energy costs, efficiency is on the agenda of every power supply designer.

Power supply topologies have been developed and improved over many years, and now the focus is turning to the semiconductor devices that are so fundamental to the operation and performance of modern switch-mode power supplies (SMPS). Significant investment has been made to develop devices that switch more efficiently and faster, allowing SMPS design engineers to meet their goals.

However, packaging of switching MOSFETs has continued to lag behind mainstream technologies with many devices remaining through-hole devices (THD), which brings advantages and disadvantages.

In this technical article, Infineon will delve into the topic of semiconductor packaging for SMPS applications and look at how improvements in thermal management and packaging are making a significant contribution to achieving the performance required for modern SMPS.

In order to meet the common goals of modern SMPS designers including fast switching, high efficiency, reduced size and weight and minimized total cost of ownership (TCO), semiconductor materials have been the subject of significant development activity. By driving down on state resistance, improving gate charge and reducing switching losses, the latest superjunction (SJ) MOSFET technologies in combination with the improved CoolSiC™ Schottky diode technologies address these challenges in modern hard- and soft-switching applications.

Despite the advances in semiconductor materials, until relatively recently, the most common packages used for power switching devices were THD types such as TO-220 and TO-247. However, these package types had some significant drawbacks, especially in modern SMPS. The long leads led to parasitic inductance that reduced switching speeds, meaning that associated magnetic components were larger and more expensive. And, with almost all other components on the printed circuit board (PCB) being surface mount devices (SMD), these THD components required a special process step to fit them into the PCB and solder them, increasing production complexity and cost.

Despite all the advantages of currently available SMD devices, such as shorter leads and easier handling in production, they still have some drawbacks with respect to cooling. Currently, SMD devices are generally cooled by contact with the PCB, either through their body or the component leads. This remains one of the major challenges for applications such as power factor correction (PFC) circuits, and is the main reason that TO-220 and TO-247 remain the most common package types used for high power SMPS applications.

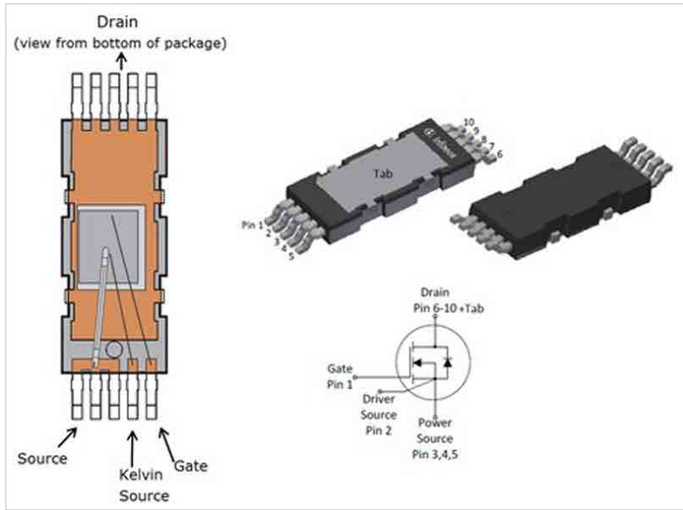


Figure 1: DDPAK technology incorporates top-side cooling in an SMD package

Top-side cooling of SMD

Heat rises and, while conventional SMD packages that disperse heat down into the PCB have some merit, definitely a package that can disperse heat towards its top surface will have better performance as it is working with physics and not against them.

The new Double DPAK (DDPAK) package from Infineon Technologies is a recent example of a surface mountable package for power devices that delivers top-side cooling. The packaging concept is optimized for high power, high voltage and high reliability applications and is suitable for both MOSFETs and SiC diodes, bringing a new direction in terms of power system integration.

Most commonly, the DDPAK offers five connections for the drain current, three source connections and one source sense connection for the gate reference potential, as well as a single connection for the standard gate drive. Although this 4-pin approach is possible with conventional THD packages and would allow for electrically cleaner driving signals that reduce switching losses in the application, THD device space constraints still remain an issue.

Parameter	TO220	DDPAK	Comparison
Height [mm]	19.40 mm	2.53 mm	86% height reduction
Thickness	4.75mm	2.53mm	46% thickness reduction
Cooling area [mm²]	118 mm²	56 mm²	50% less cooling area
Rthjc* [°C/W]	1.83 °C/W	1.65 °C/W	10% less Rthjc
Inductance	8nH	4nH	50% less inductance

*for Rthjc IPP60R180C7 and IPDD60R190G7 are compared

Figure 2: DDPAK offers vast size and performance improvements over TO-220

This is further improved by the lead inductance being reduced by 50% of the SMD package size.

The DDPAK is smaller than the TO-220 package, thereby saving space and allowing greater power densities to be achieved. This is further helped by the 18% improvement in thermal coupling between the semiconductor junction and the case.

The thinner form factor is also highly compatible with modern product designs, allowing for thinner end products to be designed.

As the body of the DDPAK is not in direct contact with the surface of the PCB (with approximately 150 µm between the two) further benefits and flexibilities are delivered to the designer.

Many product safety standards, especially those for power supplies, such as standards from Underwriters Laboratories (UL) stipulate the maximum temperature that a FR4-based PCB can reach during operation. When the semiconductor device (e.g. MOSFET, SiC Diode) is in direct contact with the PCB this rule limits the temperature of the semiconductor, thereby constraining the performance of the SMPS.

One challenge with conventional SMD packages that are mounted on PCBs is the different rate of thermal expansion of the device / package and the PCB itself, due to the different Coefficients of Thermal Expansion (CTE) of the two materials. A specific test (known as Temperature Cycling On Board

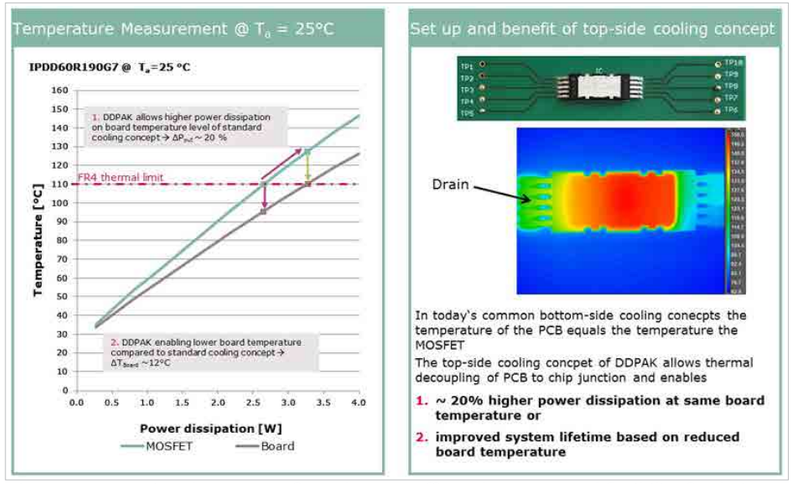


Figure 3: Separating the DDPAK from the PCB offers advantages and flexibility for designers

(TCOB)) is defined by IPC9701 to address this issue.

As the leads on a DDPAK are compliant, they have a certain spring-like quality and act as a buffer between the body of the DDPAK and the PCB. This innovation completely eliminates CTE-related failure modes including solder joint fatigue and internal package defects due to the stress. In fact, when a TCOB test with over 2000 cycles was performed on a DDPAK there were no failures – indicating a quality level that will meet automotive standards even though it is an industrial product.

Heatsinking the DDPAK

While the DDPAK is thermally very efficient, for almost all practical applications some form of heatsinking is required to be attached to the top-side to assist the movement of thermal energy away from the semiconductor junction and into the ambient surroundings. Selection of the actual heatsink to be used will depend on several factors, although the thermal energy to be dissipated and the available space within the design are generally two of the most important. The design of the DDPAK gives several options for affixing the heatsink to the package including the use of clips, push pins, adhesives or even direct soldering. The final choice will be made depending upon the needs of the design and what suits the production process. As no heatsink face or package surface can ever be 100% flat, it is good practice to include some form of thermal pad or thermal paste to ensure a good thermal contact between the DDPAK and the heatsink.

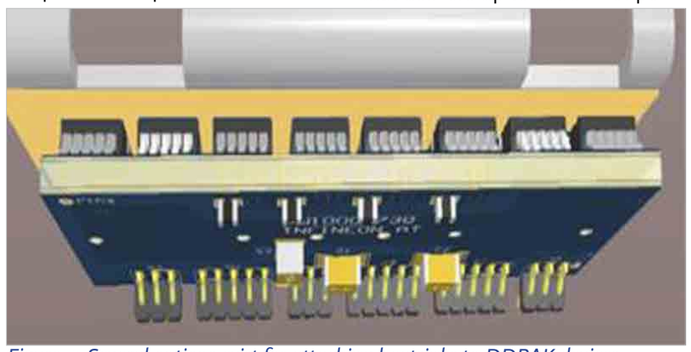


Figure 4: Several options exist for attaching heatsinks to DDPAK devices

A real world example: 1600 W Titanium server power supply

To illustrate the performance of DDPAK devices we shall consider a 1600 W Titanium server power supply which is a demanding real world application.

The basic hardware construction consists of an input filter, AC/DC conversion stage, control / bias board and DC/DC stage. As is typical for server power supplies, forced air cooling is provided via an inbuilt fan. This directs airflow over the power board that contains the DDPAK devices.

The daughter card contains a full PFC and a half-bridge LLC stage that delivers up to 1600 W of power with an input of 230 VAC. Figure 6 shows the overall design that meets the efficiency 80 PLUS® Titanium standard requirements at 50% load and exceeds them at the other critical load points of 10%, 20% and 100%.

Description	Specification
Low Line	90 V_{AC}, 500 W / 1250 W
High Line	230 V_{AC}, 500 W /2500 W
Choke	600µH
Shunt	5/10mΩ
Frequency	65kHz
Used parts	IPDD60R190G7 & IDDD04G65C6 IPDD60R050G7 & IDDD20G65C6
Accuracy	0.1%
Board dimension L x W x H [mm]	200x140x70

Figure 5: The challenging Titanium server power supply specification

Summary

Designing SMPS is a challenging business and the requirements continue to get tougher as applications demand ever-higher levels of power density and efficiency with each iteration. While the semiconductor materials have advanced dramatically, the package has not kept pace with THD packages remaining the most common in power-related applications.

However, the advent of the DDPAK from Infineon Technologies brings a new packaging concept to the market that meets the needs of even the most demanding applications. Thermal performance is improved due to top-side cooling and switching speed is increased due to a 50% reduction in parasitic inductance.

Furthermore, the innovative mechanical design not only separates the module from the PCB, it also includes compliant legs that remove any of the potential failures associated with CTE.

When combined with the latest silicon technologies, such as CoolMOS™ G7 and CoolSiC™ G6, DDPAK delivers a significant step forward in switching devices for market-leading SMPS.

More detailed technical data on the DDPAK top-side cooled package, along with a dedicated application note, will be available on the Infineon website.

Infineon Technologies
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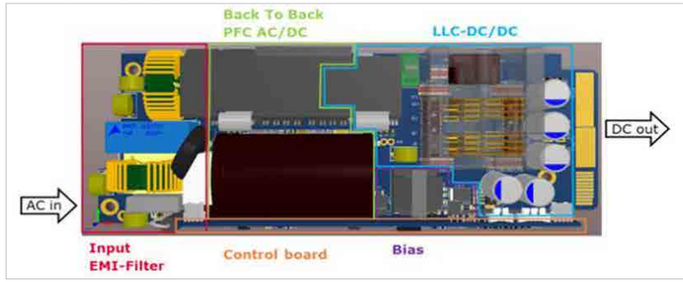


Figure 6: Basic layout of the 1600 W server power supply demo setup

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The Renesas RZ/N1 family, offer high-precision time sync and time-controlled transmission using TDMA

By: Arno Stock, Renesas Electronics Europe

Extensions to the IEEE 802.1Q standard for Ethernet switching, listed under the generic term "Time Sensitive Networking" (TSN), allow automation solutions with homogeneous network architecture from sensors to the cloud. In contrast to this, traditional solutions using proprietary network standards at the field level to ensure hard real-time always mean a certain discontinuity in the network architecture. The TSN technology resolves this discontinuity, facilitating the flow of information between the field level and higher levels of automation hierarchy. In addition, users and equipment manufacturers also benefit from a unified hardware that offers flexibility and cost savings. Another plus point is a better utilisation of installed equipment and cables through common use for a wide variety of applications without risking mutual interference.

Due to the apparent benefits mentioned above, the introduction of TSN technology into the automation world is no longer questioned today. Strategy variations are found mostly regarding timing and sequence of steps only. Individual manufacturers already have the first TSN capable products on the market today, more are committed, and others will follow step by step.

A key question while introducing new technologies is the broad availability of suitable hardware. The TSN standards are still relatively new, and the implementation into corresponding semiconductor devices requires time. On the other hand, only a small however essential part of the TSN standards requires dedicated hardware support. Many TSN-related functions, e.g. for network management, are purely software-based and can easily be implemented on any hardware.

Today, equipment manufacturers have two main options at their disposal to map TSN functionality in their equipment. On the one hand, FPGA-based network interfaces offer a flexible approach to incorporate latest functions into products promptly. The price for this cumulates over three factors, i.e., the relatively high product costs, the development efforts for the FPGA logic including testing, certification and eventually the IP licensing costs.

On the other hand, the market offers standard semiconductors that provide verified TSN functions at low cost. This is feasible because instead of reinventing the wheel, the TSN standards, which are largely based on proven concepts, develop and generalise these concepts further. Depending on the specific application requirements, using these TSN precursor devices, it is already possible and common practice today to implement the TSN functionality in automation solutions based on off-the-shelf standard components.

TSN technology for an automation system

The demands on network elements, in particular on end nodes and switches, vary depending on their function and configuration in the network. The network interface of a PLC or in an edge computer must be more efficient than that of simple field device. Likewise, the switches at this level must also cope with a much higher network load than their counterparts in a line at the lower end of the field level. This is reflected in the minimum requirements for the corresponding components so that especially in the area of simple field components, simplified solutions for line or ring topologies are feasible with only two external Ethernet ports.

The TSN sub-standard family offers two main methods for chronologically deterministic transmission: Prioritisation and frame pre-emption (asynchronous) and time-controlled transmission in reserved time slots (TDMA method, synchronous). Both can also be used in combination. Currently, in the field of industrial automation, the focus is on the time-controlled transmission of hard real-time data via TSN. This principle has already proven itself in established standards such as Profinet IRT, SERCOS III, EtherCAT or Powerlink. The TSN standard IEEE802.1Qbv extends and generalises the existing proprietary mechanisms to extend their scope of application and enable the coexistence of different real-time systems in a common network domain without mutual interaction. The time-controlled transmission to Qbv avoids undesired collisions between different data streams leaving the switch at a common port. If the component under discussion is only an end node with a single Ethernet port, i. e. without integrated switch functionality for forwarding, then a sufficiently precise control of the transmission time of individual Ethernet frames

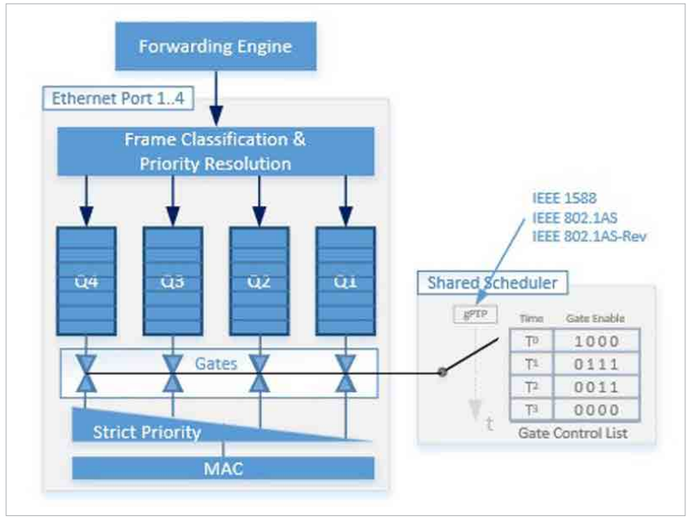


Figure 1: Structure of the TDMA function

time synchronisation messages. The frequency and phase of the PTP timer must be adjustable by time synchronisation.

TSN in existing devices

Some of the currently available semiconductor devices, such as those of the Renesas RZ/N1 family, already offer mechanisms like high-precision time synchronisation and time-controlled transmission using the TDMA method.

TSN will utilize the new IEEE 802.1AS-Rev protocol which is based on IEEE 1588 and does not impose any additional requirements on the hardware. As an alternative today either its precursor, the IEEE 802.1AS or the IEEE 1588, which was being used hitherto, is deployed. Differences between the implementation of the two lie exclusively in the software layers.

The TDMA technique has also

Figure 1 shows the structure of the TDMA function in the RZ/N1 blocks. At the top end, the incoming Ethernet frames are relayed to their destination ports by the forwarding engine. There, each frame is classified according to configurable criteria and placed in one of the four output queues (Queues). The gPTP hardware timer is synchronised with the network time of the TSN domain. All time slots of the TDMA mechanism are derived from it. The time slots with individually configurable length are specified centrally for all Ethernet ports of the device in a Gate Control List with four entries.

Controlled via Bitmasks, arbitrary output port queues can be opened in each time slot. In this context, “opened” means that Ethernet frames, which are in a queue, can reach the MAC and thus the cable via priority control. The priority control always selects the Ether-

Feature	IEEE 802.1Qbv	IEEE 802.1Qav + TDMA
Traffic Queues	8	4
Time Slots	> 8	4
Scheduler	Individual per egress port	Global for all ports
Classification criteria	VLAN PCP, default for untagged frames	VLAN PCP Destination MAC IPv4 (DiffServ) Ipv6 (Class of Service) Programmable Pattern Matcher Ethernet frame type default Queue for untagged frames
Congestion Control	Guard Window	None

Table 1: Comparison between Qbv and Qav +TDMA

net frame of the highest priority open queue for forwarding. However, the Ethernet frames in the "closed" queues are not forwarded in the relevant time slot.

The differences in Qbv-capable hardware lie primarily in the number of different queues and time slots, i. e. the diversification in the handling of individual Ethernet frames. **Table 1** shows a detailed comparison. For example, the Renesas RZ/N1 family chips support four queues and four time slots. For comparison: the TSN standard Qbv defines eight queues and leaves the number of time slots undefined. Apart from that, though a Qbv-standard switch has a central gPTP timer, the Gate Control List is port specific so that each port of the switch can have an individual schedule.

For a field device with a single Ethernet port and field devices in a simple line or ring topology using the embedded switch, the above limitations are often acceptable. This is so because only a few different real-time streams have to be transmitted, and the transmission schedule for all ports is identical to allow an unobstructed flow of the Ethernet frames through the component and thus through the line or ring.

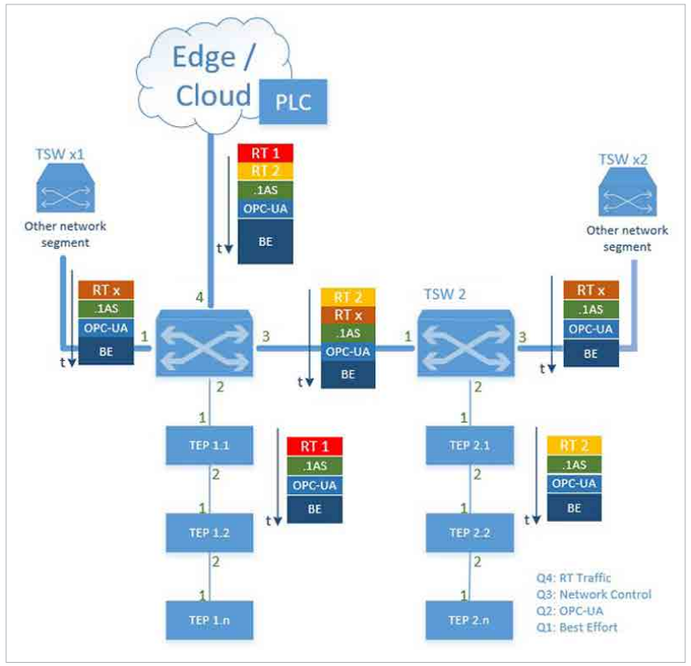


Figure 2: TSN sample system

The following TSN application example illustrates this.

TSN application example

The sample configuration in **figure 2** illustrates how a TSN-based automation solution can be built using the features of the available RZ/N1 devices.

A TSN-capable PLC, existent physically in the plant or virtually in an edge computer, controls a large number of I/O components (TEP n.m) that are organised in two lines. As an alternative, a ring structure would also be possible here. The network traffic is time-controlled and synchronised with the PLC's operational cycles. The PLC operational cycles consist of three phases: Reading the actual values from the I/O devices, calculating new output values through the PLC program and output the new output values to the terminal devices. Over the time, phase 1 and phase 3 overlap. The TSN backbone consisting of TSN switches TSW 1 and TSW 2 must handle all network traffic between PLC and sub-rings and, if necessary, also as indicated by the TSW x1 and TSW x2 switches, further cross-traffic between network components connected to the segment under review. This calls for full support of the TSN standards Qbv and, if required, Qbu by the TSW 1 and TSW 2 backbone switches.

Priority	Class	Example	Queue	T_0	T_1	T_2	T_3
7	Real-time data	I/O data	4	1	0	0	0
5	Network control	Time synchronisation	3	0	1	0	0
3	Prioritised	OPC-UA	2	0	1	1	0
1	Others	http, Status, Diagnosis	1	0	1	1	0

T_0: Time slot for real-time data only. Avoidance of collision with other classes.
T_1: Time slot for all remaining classes
T_2: Time slot for low-priority data only, to ensure minimum throughput.
T_3: Guard band, guarantees a free output port immediately at the beginning of T0 of the next cycle

Table 2: Communication classes of the sample network

The requirements in the sub-lines are much more relaxed. The TEP n.m components there must only forward network traffic to and from the neighbouring components. Their role as a TSN endpoint is limited to a single real-time stream in the transmitting and receiving direction for communication with the PLC and other non-time-critical communication, e. g. for time synchronisation or as an OPC-UA server. **Table 2** in this example shows the different classes and their mapping to the available hardware of the RZ/N1 family devices which fulfil all requirements of the TSN function required in this constellation.

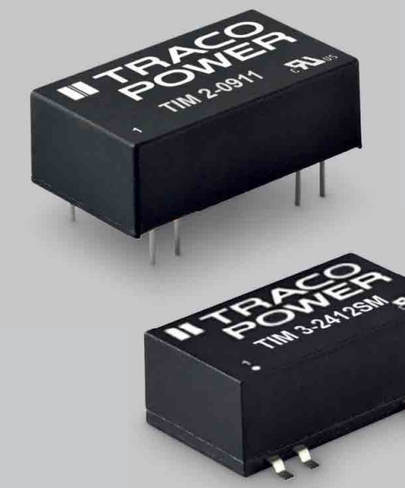
In the example, all network components, switches, and end nodes are synchronised with each other via the IEEE 802.1AS time synchronisation protocol and use the time-controlled transmission to avoid undesired collisions. Communication takes place in a fixed time raster which repeats cyclically. The assignment of the classes to the time slots of this raster for devices in the sub-lines is also shown in table 2. The cycle time and the length of the individual time slots depend on the application. The time slot T3 is always empty, i. e. no queue may send during this time, and should have the length of the longest occurring Ethernet frame. This guarantees that the output ports at the beginning of the real-time window To are always free and are not occupied by the previous frame, which would have led to an undesired delay while sending the real-time frame.

Communication scheme

All TEP n.m endpoints send their actual values as input variables to

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			Cycle	Cn				Cn+1				Cn+2
			SPS State	Data I/O		Computing RT.out for tn+1		Data I/O		Computing RT.out for tn+1		...
Link (Port to Port)												
SPS/Cloud	E	TSW1	4.I	RT.out.2.tn	RT.out.1.tn	Net Ctrl	OPC-UA & Best effrt	RT.out.2.tn+1	RT.out.1.tn+1	Net Ctrl	OPC-UA & Best effrt	...
	I		4.E	RT.in.2.tn	RT.in.1.tn	Net Ctrl	OPC-UA & Best effrt	RT.in.2.tn+1	RT.in.1.tn+1	Net Ctrl	OPC-UA & Best effrt	...
TSW 1	1.E	TSWx1			Net Ctrl	other RT	OPC-UA & Best effrt		Net Ctrl	other RT	OPC-UA & Best effrt	...
	1.I				Net Ctrl	other RT	OPC-UA & Best effrt		Net Ctrl	other RT	OPC-UA & Best effrt	...
	2.E	TEP 1.n	1.I		RT.out.1.tn	Net Ctrl	OPC-UA & Best effrt		RT.out.1.tn+1	Net Ctrl	OPC-UA & Best effrt	...
	2.I		1.E	RT.in.1.tn		Net Ctrl	OPC-UA & Best effrt	RT.in.1.tn+1		Net Ctrl	OPC-UA & Best effrt	...
	3.E	TSW 2	1.I	RT.out.2.tn		other RT	Net Ctrl OPC-UA & Best effrt	RT.out.2.tn+1		other RT	Net Ctrl OPC-UA & Best effrt	...
	3.I		1.E	RT.in.2.tn		other RT	Net Ctrl OPC-UA & Best effrt	RT.in.2.tn+1		other RT	Net Ctrl OPC-UA & Best effrt	...
TSW 2	2.E	TEP 2.n	1.I		RT.out.2.tn	Net Ctrl	OPC-UA & Best effrt		RT.out.2.tn+1	Net Ctrl	OPC-UA & Best effrt	...
	2.I		1.E	RT.in.2.tn		Net Ctrl	OPC-UA & Best effrt	RT.in.2.tn+1		Net Ctrl	OPC-UA & Best effrt	...
	3.E	TSWx2			Net Ctrl	other RT	OPC-UA & Best effrt		Net Ctrl	other RT	OPC-UA & Best effrt	...
	3.I				Net Ctrl	other RT	OPC-UA & Best effrt		Net Ctrl	other RT	OPC-UA & Best effrt	...
TEP 1.n	2.E	TEP 1.n+1	1.I	RT.in.1.tn		Net Ctrl	OPC-UA & Best effrt	RT.in.1.tn+1		Net Ctrl	OPC-UA & Best effrt	...
	2.I		1.E		RT.out.1.tn	Net Ctrl	OPC-UA & Best effrt		RT.out.1.tn+1	Net Ctrl	OPC-UA & Best effrt	...
TEP 2.n	2.E	TEP 2.n+1	1.I	RT.in.2.tn		Net Ctrl	OPC-UA & Best effrt	RT.in.2.tn+1		Net Ctrl	OPC-UA & Best effrt	...
	2.I		1.E		RT.out.2.tn	Net Ctrl	OPC-UA & Best effrt		RT.out.2.tn+1	Net Ctrl	OPC-UA & Best effrt	...
		TEP Scheduler		T0		T1	T2 T3	T0		T1	T2 T3	...

Figure 3: TSN Schedule

the PLC at the beginning of each network cycle. The PLC for its part sends the new output values computed in the last cycle to the endpoints.

For this purpose, on each line and the backbone, a time slot To is reserved during which only real-time data is transferred between the endpoints TEP n.m and the PLC. Collisions with other network traffic are impossible so that the maximum transmission time to and from each endpoint is guaranteed. The end nodes transmit their actual values to their superordinate backbone switches TSW1 and TSW 2 in both lines simultaneously. These collect the data and send it to the PLC. Also here, collisions between the line frames are excluded because the backbone switches transmit the data of each line in a separate time slot. This necessitates appropriate resources in the backbone switches.

The output values are transmitted in two steps to achieve utmost simultaneous arrival of the PLC output values at each of the TEP n.m end node; first, to the line 2, which is one switch away, then to line 1. The time slot To in the sub-lines must be selected long enough to provide sufficient time for forwarding all output variables. The simultaneous exchange of actual and new output values runs collision free and doesn't require any additional measures because the data flow in opposite directions.

After all actual values have reached the PLC within their defined transmission window, and the new output values have arrived at all end nodes, the PLC starts to process its user program which computes new output values from the current values. The output nodes process their new set-points synchronously based on the network-wide synchronised time so that all components change their output states simultaneously.

After the PLC has completed its computations, the next network cycle follows seamlessly.

Additional data can be transferred beyond the reserved time slots on the TSN backbone and in the lines one and two without having to worry about any effect on the real-time system in operation. For example, real-time data RT x can be encapsulated between adjacent network segments in individual time slots as long as the total data throughput of the individual network strands provides sufficient remaining bandwidth. Additional important data streams are used for time synchronisation or to query OPC-UA objects.

Conclusion

TSN is still a young standard, and the establishment of the necessary hardware support is in progress now. But even with off-the-shelf standard components such as those of the Renesas RZ/N1 product family, which are based on extended predecessor standards, the benefits of TSN technology can already be reaped today as long as the differences are acceptable in the actual application.

Renesas Electronics Europe
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Lighting the Way for the Automobile Industry

High power LEDs are an efficient and reliable source of light

By: Steve Subiry, Global Product Manager, Eaton

Light Emitting Diodes (LEDs) are semiconductor devices which provide an efficient and reliable source of light and contain no moving parts, making them very reliable in environments with elevated vibration and shock, such as automobiles. Other desirable properties include high efficiency, long life and brightness. LEDs are ideally suited to a variety of automotive applications, including backlighting, instrument panels, liquid crystal displays and general lighting, such as head and tail lamps. With the latest technical advancements in high power LEDs, auto manufacturers are expected to phase in LED lighting across all their vehicles by 2020.

High power LEDs are an efficient and reliable source of light in multiple areas within an automobile, including headlights, running lights, rear vehicle brake lights and passenger compartment lighting. Until recently, however, LED drivers, which supply power to the LEDs and protect them from voltage or current fluctuation, were unable to support the high lumens required for headlights and running lights, as well as the higher ambient temperatures that exceeded +125 °C.

Today, advanced LED driver designs are being developed with electronics components that result in a higher luminescence, better energy efficiency, and lower cost. These products enable manufacturers to develop higher power LED headlight clusters that perform well at higher currents in a smaller footprint. Specific inductors support a more advanced LED driver design that handles higher voltages and a wider array of high power LEDs that can operate "bend light" and dimming functions to improve roadway safety.

Excelling in Versatile and Rugged Conditions

It is critical for manufacturers to work with suppliers who can deliver automotive-grade, high power inductors that offer low electromagnetic interference (EMI) and higher operating temperature, which are essential requirements for obtaining efficient DC/DC conversion. These robust inductors are designed to withstand harsh environmental, electrical and mechanical conditions. Many of the more recent applications demand that the inductors perform at temperatures from -40 °C to +155 °C, representing the same inductance roll-off characteristics across the entire temperature range. Tight thermal coupling can ensure effective heat dissipation under high current conditions. Utilizing a variety of sizes and higher inductance values allows automotive designers to operate at higher voltages needed to drive multiple high-power LED arrays for headlights and daytime running lights.

With the rapid increase of automotive electronics content in vehicles, maintaining a low EMI is required. Inductors are recommended to be magnetically shielded, making them suitable for virtually all applications throughout the vehicle. This gives automotive engineers design flexibility. Additionally, these inductors should be AEC-Q200 Grade-1 qualified and appropriate to operate in temperatures of up to +165 °C, making them popular for engine compartment applications including electric motors, pumps, and engine control modules, as well as for lighting body and security systems.

Selecting a circuit topology

LEDs must be properly driven to ensure peak performance and maxi-

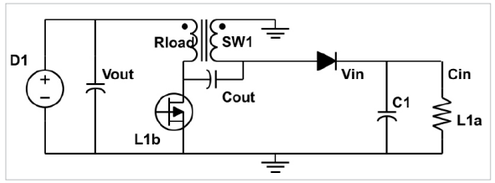


Figure 1: SEPIC circuit

mum useful life. The key to successful lighting circuits is designing and implementing an effective driver with a suitable circuit topology. Two topologies are described here:

SEPIC Circuit

A Single-Ended Primary Inductor Converter (SEPIC) allows the output voltage to be greater than, less than, or equal to the input voltage in DC-DC conversion (**Figure 1**). Typical vehicular applications include daytime running lights (DRLs) and, more recently, full LED headlights, which supports all of the lighting options of low-beam, high-beam, fog and turning indicator lights using a single SEPIC driver circuit. This single circuit is able to output the optimal LED driver voltage and currents based on the actual number of light features turned on. Eaton's off-the-shelf AECQ Grade1 coupled inductors (DRAQ series) may power SEPIC drives up to 40W, which is sufficient for a standard LED headlamp. SEPIC drives make complete LED headlights affordable to the general public, not just luxury car drivers.

Boost and Buck Circuit

Boost and Buck circuits are used for the most sophisticated LED headlights (See **Figure 2**), providing sufficient power to drive multiple light features all the way up to 120W per lamp. This type of circuit topology includes a powerful boost converter which normally boosts the battery voltage to a maximum 60V. This elevated voltage is then bucked down to the required voltage level to power different LED strings of the headlight. The different light strings may be composed of a matrix of uniform LEDs (normally 32-1024 pixels) or strings of power LEDs and some standalone power LEDs. These complex headlight units can control the light intensity based on the road conditions, driving speed, steering wheel position and upcoming traffic sensed by the Advanced Driver Assistance System (ADAS). The complex LED drivers adjust the light intensity and focus automatically for ride enhancing safety on the road, whether day or night. Some laser LED diodes may illuminate all the way up to 600 meters, allowing high speed driving during the evening. These drivers require robust inductors with high power density and 10-20pcs per lamp to properly manage the various voltage and current requirements. When selecting components, it is important to choose those with high efficiency, high temperature capability, high heat dissipation capability and stable operation at all temperatures ranging from -40 °C to +125 °C ambient. Eaton's HCM1A inductor product line is designed specifically to take this challenge with various number of inductances and size options.

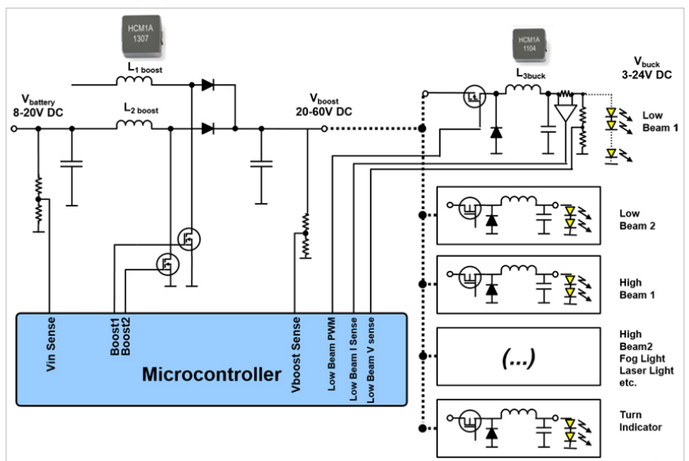


Figure 2: Boost-Buck circuit

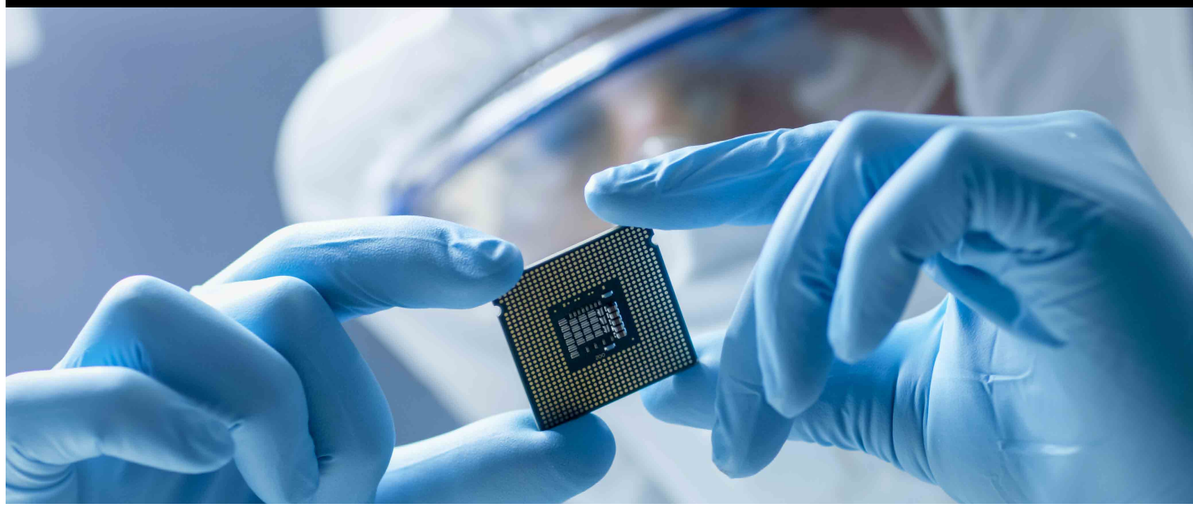
Summary

Advanced automotive-grade electronics are versatile, affordable, and provide the automotive engineer with more innovative solutions – adding flexibility to their designs, enabling new vehicle features, and enhanced driving experience.

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Special Report: High Bandwidth Semiconductors + Packaging Technologies

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Powering the Future with Intelligence and Efficiency

GaN HEMT transistors deliver unprecedented levels of performance compared to conventional MOSFETs

By: Patrick Le Fèvre, Powerbox

In March 2018 the Applied Power Electronics Conference (APEC) took place in San Antonio (Texas). APEC is the world's largest convention dedicated to applied power electronics, and the place where research laboratories, universities, market analysts and companies showcase the latest and often 'industry first' technologies that make power supplies more efficient, reliable and safer. This year's event was definitely the real 'kick-off' point for wide bandgap semiconductors, especially the ones based on Gallium Nitride (GaN) technology.

The event was also a symbolic milestone for 'digital power', which initially emerged in 2003 as a promising technology. GaN started its journey five years ago, and is following a similar path to digital power by moving gradually from a 'technical curiosity' to a 'commercial product'. Digital power and GaN are both technologies that have been highly debated and challenged when introduced to the market and it is interesting to link both of them in this way, especially when the outcome of combining the best of the two technologies will result in truly outstanding commercial products.

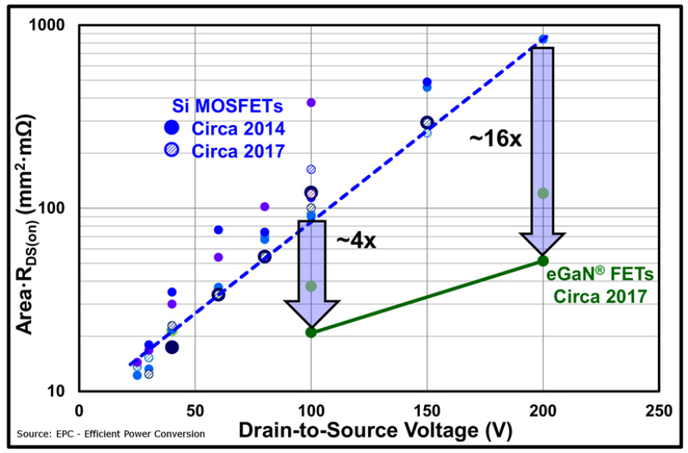


Figure 1: Comparison of the normalized area of a chip versus the voltage rating of the best MOSFETs, in blue, with the latest generation of GaN FET (Source Efficient Power Conversion (EPC))

From skepticism to game changer

Ten years ago when GaN pioneers presented the concept of offering a more efficient Gallium Nitride based alternative to super-junction MOSFETs, it attracted a lot of opinions and strong statements, "It will never fly"! As it has been for the digital power, the journey from 'garage development' to commercial products has been full of frustration, tears and deceptions, and only perseverance and a strong belief in the technology have brought it to a successful state.

GaN high-electron mobility transistors (HEMT) have very interesting intrinsic behavior patterns, delivering unprecedented levels of performance compared to conventional MOSFETs. In terms of intrinsic performance, having a very low charge gate, zero reverse recovery and flat output capacitance, GaN has everything that power designers dreamed of for decades to improve performance, decrease size and to reach the mythical 99.99 % efficiency.

One example of the benefit of GaN transistors is the die size, which is much smaller than conventional MOSFETs (**Figure 1**). The graph compares the normalized area of a chip versus the voltage rating of the best MOSFETs with the latest generation of GaN FETs. The separation in the die size 'Figure Of Merit' between silicon and GaN FETs is growing rapidly - now sitting at 16 times better at 200V and four times at 100V - and we may not have reached the limits yet. This opens the door for power designers to create products that will amaze us with their performance levels.

Step by step to maturity

As it is for any new technology, especially when disruptive, moving from research to high volume production is a long process, and one that includes an education for electronic engineers. In the case of GaN, the implementation of zero-voltage switching topologies requires very specific drivers and new methods of control. Despite the huge benefits of GaN transistors, for many years the shortage of efficient drivers has limited the interest level from industrial designers. However, the increased number of semiconductors players investing in GaN in the last two years has made this technology simpler to implement.

Many technical barriers have been removed. Manufacturing processes have gradually been optimized to increase yield and reduce cost, quality processes specific to this technology have been implemented, and in November 2017 the JEDEC organization announced the formation of a new committee to set standards for Wide Bandgap Power Semiconductors (JC-70), which is a sign of readiness for mass implementation.

Step by step, the puzzle is going to be completed and if GaN has been widely used in LED and RF applications, it is now starting its journey into DC/DC converters and AC/DC power supply segments. There is not a week without a new product announcement and for sure a lot of things will happen during the next coming months.

Have you ever imagined?

Starting my career as a power supply designer in 1982, I have been through many technology shifts and I still remember the debates about the risks of moving from linear power supplies to switching ones. I was lucky enough to work for a large telecommunications company that began research into digital power when many considered it to be anecdotal, and I was happy to be among the pioneers exploring new ways to manage power conversion and to improve efficiency. Today, the combination of digital control and the unprecedented benefits of GaN are realizing a dream for all ICT board power designers - to manage the conversion from 48V to 12V in a footprint exceeding 1200W per cubic inch with an efficiency of 96 percent, and we haven't seen the end of the GaN evolution.

Celebrating 15 years of digital innovation

Today, digital power is part of most power engineers' educational program and is implemented in a wide variety of applications. It is important to remember the origins of digital power, and how from early research work conducted in the mid-seventies by Trey Burns, N.R. Miller and others, digital power gradually took its place in the power industry to reach its current level of maturity. In the seventies, at a time when the power industry was slowly considering the migration from linear-power to switching-power, Trey Burns researched and explored the use of state-trajectory control law in step-up DC/DC converters and compared two methods of practical implementation, one employing a digital processor and the other using analogue

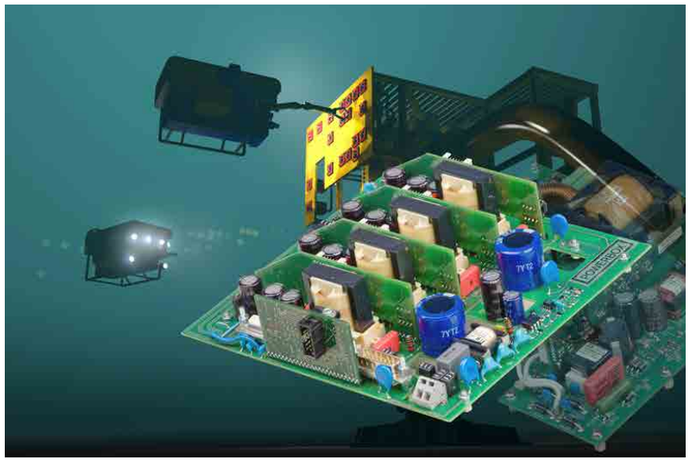


Figure 2: PRBX VB410-384 - Subsea power supply with full digital control power management, monitoring and intelligent redundancy.



Figure 3: PRBX GB350 – Coreless power supply operating in high magnetic field applications (MRI) fully digitally controlled and monitored

computational circuits. It is anecdotal but interesting to note that at that time, an experimental product built by Trey Burns was a boost converter operating at a switching frequency of 100Hz - which sounds slow - but it had to be slow because it took up to 450 micro-seconds to execute the digital program per sample.

After more than 40 years from the initial research to APEC 2018, and 15 years on from the first commercial digital DC/DC converter presented in 2003, the technology is now widely adopted by almost all segments of the industry. From monitoring and controlling deep sea power systems with the highest level of reliability (**Figure 2**) to guaranteeing stable voltages to critical medical equipment exposed to the high magnetic radiation of a Magneto Resonant Imagery system (**Figure 3**), digital power is almost everywhere, and soon to be embedded in equipment installed on the International Space Station. For all the pioneers who have been engaged in this journey, this is an amazing situation and we are now seeing the same level of excitement with the development of Gallium Nitride devices.

5000W Per Cubic inch and 99.99% efficiency

What makes power designers' lives exciting is the ever-present level of innovation making it possible to improve performance levels, contributing to reducing our environmental impact and to build a sustainable society. We are flooded with news every day – the Internet of Things (IoT), autonomous and electrical vehicles, and many technical innovations – they will all require very efficient and compact power sources. 5000W per cubic inch and 99.99 percent efficiency might sound impossible to reach, but who in the mid-seventies would have imagined what we already achieved today when combining new topologies, digital control, new components such as GaN, and the passion to innovate?

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SPECIAL REPORT : HIGH BANDWIDTH SEMICONDUCTORS + PACKAGING TECHNOLOGIES

Advanced Cooling and Efficient Semiconductor Technology

Solving the thermal challenge for new designs no longer needs to be a significant challenge

By: Dongsup Eom and Dennis Kim, ON Semiconductor

Power engineers often face seemingly conflicting and almost impossible challenges. As system designers add more features and functionality to newer product generations, so the system requires more power, but has less space available to generate it. While there are many techniques available to manage heat, forced air cooling is often unreliable and draws in dust that can lead to premature failure. Passive cooling using heatsinks meanwhile is reliable, but requires space and adds weight that is often just not acceptable in modern equipment that is designed to be portable. As such, solving the thermal challenge is often a significant challenge on new designs.

The best approach to thermal management is not dealing with the waste heat, it is to find more efficient approaches so that the heat is not generated in the first instance. Correct selection of the topology and, more importantly, the power switching components, is critical to achieving this. However, all power circuits generate some heat, no matter how efficient they are.

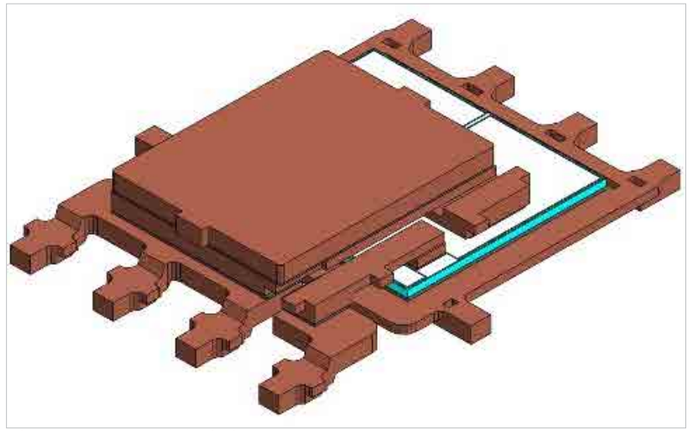


Figure 1: 3D model depicting Dual Cool technology

As designs get smaller, the opportunities for passive convection cooling are reduced and designers have to find innovative ways to thermally connect semiconductor junctions heat spreading surfaces and ultimately to the ambient environment where the heat can dissipate.

However, the impact of package selection is not limited to thermal performance - packages with longer leads introduce parasitic elements into the circuit that can affect both the speed of operation and efficiency.

A novel approach to cooling small packages

ON Semiconductor is one company that has developed a power-specific packaging technology to address the need for improved thermal performance in today's electronic designs. 'Dual Cool' technology is based on Power Quad Flat No-Lead (PQFN) packaging and creates a direct heat path from the drain and source sides of the vertical MOSFET die structure. This structure facilitates adding a heatsink alongside direct thermal conduction into the printed circuit

board (PCB).

Dual Cool has evolved from the popular and established PQFN packaging. While implementing new features, the Power33 and Power56 lead geometries and pinouts are retained, allowing designers to improve thermal performance without having to change the PCB layout, thereby facilitating an easy transition.

By replacing wire bonds with copper clips that are similar to leadframes, Dual Cool improves the thermal conductivity and current handling of the package. As a result, higher power densities are possible.

A standard PQFN package with clip technology offers a 13.9% improvement over a traditional wire bond-based PQFN package. Adding Dual Cool technology increases the performance differential to 57.5%.

Dual Cool uses four mils thin silicon, which is half the normal MOSFET thickness, thereby improving thermal and electrical performance. The top and bottom surfaces of the die are plated to permit solder attachment of the drain lead frame on the bottom, and the source and gate clips on the top. To improve the heat transfer path from the die to the top of the package, a heat slug is soldered to the source clip. Solder attachment of the silicon to the lead frames, with optimized copper clips additionally reduces electrical and thermal parasitics.

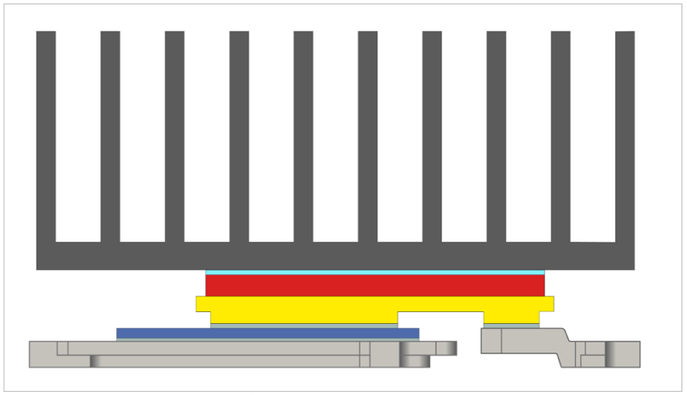


Figure 2: Dual Cool is ideal for use with a heatsink

The θ_{JC} (thermal resistance from the junction to the case) has two important aspects: the junction to case thermal resistance to the drain tab as well as the top heat slug. The datasheet contains these values for each specific product type, giving a measure of the two most efficient heat paths out of the component, allowing the designer various options for managing the thermal energy created by high power density designs.

Dual Cool and PowerTrench MOSFETs

ON Semiconductor's PowerTrench MOSFETs offer excellent electrical properties including very low levels of RDS(on) making them a good choice to benefit from the new Dual Cool packaging concept. The integrated monolithic SyncFET Schottky body diode is ideal for power applications. The combination of Dual Cool and PowerTrench occupies the same land pattern as PQFN-JEDEC standard parts, yet allows for >60% better thermal performance as shown in **Figure 3**.

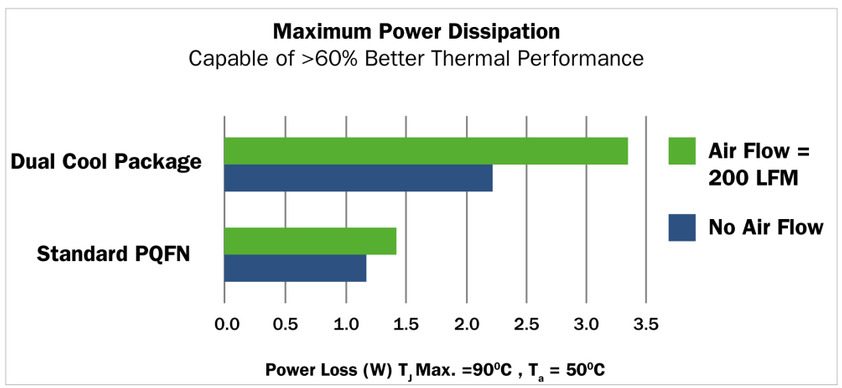


Figure 3: Users can achieve a 60% performance improvement

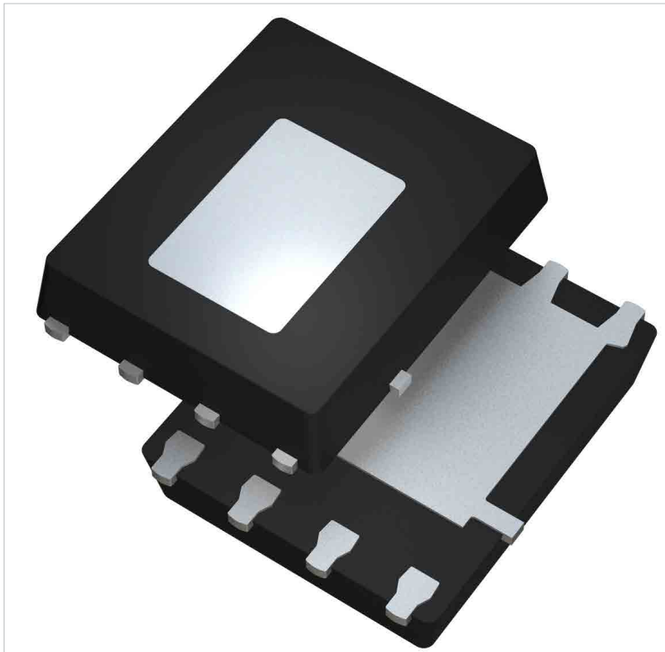


Figure 4: Dual cool technology embedded in a PQFN package

Dual Cool PowerTrench MOSFETs with top-side cooling have a far better thermal coupling to the top of the device. In many cases, they can be used without an additional heatsink thereby reducing size, cost and weight. With enhanced dual-path thermal performance and improved parasitics over its wire-bonded predecessors, the use of a heatsink provides even more impressive results.

Laboratory testing has shown that when a heatsink is used with Dual Cool package technology, synchronous buck converters deliver higher output current and increased power density. With ON Semiconductor's trench silicon technology, Dual Cool packaging gives excellent results in terms of both power density and thermal performance.

The Dual Cool product portfolio from ON Semiconductor offers more than 20 products with BVDSS values from 25 V to 150V and multiple choices for RDS(on) and package size. All Dual Cool solutions are lead-free, RoHS-compliant, and available in 3.3 mm x 3.3 mm, 5 mm x 6 mm, and 8 mm x 8 mm PQFN packages.

Dual Cool and heatsinks

Heatsinks are a very effective method of further improving thermal performance, especially if there is airflow across their surfaces.

Many styles and shapes of heatsinks are available and selection of the appropriate solution will depend on the application, available space and heat to be dissipated. Attachment methods include solder anchoring, push pin, thermal tape, screwing, or glue / adhesive – the selected method will depend on the products selected end use criteria, and any available processes at the manufacturing site.

Thermal interface materials (TIM) such as those listed below can be used to improve the contact between the Dual Cool package and the heatsink and eliminate any possibility of air gaps in the interface that will limit heat dissipation.

- Thermal Grease
- Insulating Pad
- Phase-change Materials
- Thermal Tape
- Gap Filler Sheet or Gel
- Thermally Conductive Glue or Adhesives

Testing and evaluation by On Semiconductor demonstrated

that thermal grease provides an improvement over gap filler sheets primarily due to the thin interface. Wire bonded packages showed a 10% improvement over gap pad, which rose to 12% for clip bonded packages. For Dual Cool, performance was shown to be improved by 21% over the Gap Pad.

The result is that a device that can dissipate 5.8 W with a thermal Gap Pad, can dissipate 7.0 W with grease, with no other changes. However, grease may be the best performance-wise, but is more difficult to dispense, rework and does not have the electrical isolation properties of the pad. The application will dictate if these trade-offs are worth making.

In applications where tightening a screw, a push pin, or a solder anchor is used to secure the heatsink, a compression load is placed on the component. The PQFN 8 x 8 Dual Cool package has been tested and simulated to withstand high compression loads. Results show that the package can withstand up to 1500 N of load without causing any electrical or mechanical failure.

Board layout and production
Due to their small size and low profile, PQFN packages are an ideal space-saving alternative to leaded options. Additionally, the Dual Cool PQFN offers a size advantage over the industry standard D2PAK SMD package.

Looking in more detail, the source and gate pads are larger than the package lead to allow toe filleting of the solder. The pads are also wider than the leads, to account for variation in board fabrication and component placement during assembly. Combined, these tolerances can stack up to 0.10 mm.

The PCB pad for the exposed thermal pads is the same as the size of the exposed pad allowing the surface tension of the molten solder to pull the component so that it perfectly aligns with the land pad. This process ensures that the Dual Cool packages are consistently and correctly aligned during production.

In power applications where significant heat is generated, the PCB pads act as a local heatsink, transferring thermal energy into the board itself.

When performing thermal characterization of PQFN 8 x 8 Dual Cool packages, it was demonstrated that there is a significant improvement in the thermal resistance from junction to ambient if the copper on the PCB is increased to a larger (say 1in2) copper pad connected to the solder-mask-defined land pad. This approach is recommended for the drain pad.

Summary
By combining innovative Dual Cool packaging with high performance PowerTrench technology, engineers are now able to access products that firstly minimize heat generation by operating very efficiently and, secondly, have the ability to move any excess heat to the edge of the package.

In fact, in many applications, due to the efficient performance the Dual Cool / PowerTrench, devices can be used without additional heatsinking reducing size, weight and cost of the system solution.

On Semiconductor
www.onsemi.com



SiC Cascodes: Fast-Track to Wide-Bandgap Performance

Benefits of wide-bandgap semis aren't out of reach if not committed to a complete redesign

By: Anup Bhalla, VP Engineering at UnitedSiC

SiC MOSFETs can deliver impressive performance and efficiency gains in power-conversion circuits, but a clean-sheet design is needed for best results. SiC cascodes offer a drop-in replacement bringing instant access to many of the advantages of wide-bandgap devices.

Drop In, Turn On
Silicon carbide diodes, and MOSFETs in 600 V or 1200 V ratings, are now readily available in the market and enable power-systems designers to leverage the advantages of wide-bandgap (WBG) semiconductors in power-conversion circuits like H-bridges to increase energy efficiency, temperature capability and power density. To maximize the benefits of these devices, the circuit ideally should be designed from the ground up, using optimized gate-drive circuitry to provide the asymmetrical turn-on/turn-off voltages required by SiC FETs, and smaller magnetic components made possible by SiC's high-frequency capability.

Such a clean-sheet approach is practicable when designing advanced new equipment such as inverters for electric vehicles and power conditioning for wind or solar microgenerators, where ultimate performance is critical for success. However, there are numerous established applications that could benefit from valuable performance and efficiency improvements if upgrading to WBG devices such as SiC FETs could be made faster, less complicated and cost-neutral. Ideally, the industry needs drop-in replacements for existing silicon devices, to allow products to be upgraded at a suitable juncture in the model's history. This could be when a significantly revised version is to be launched in the market, or when a current component becomes obsolete.

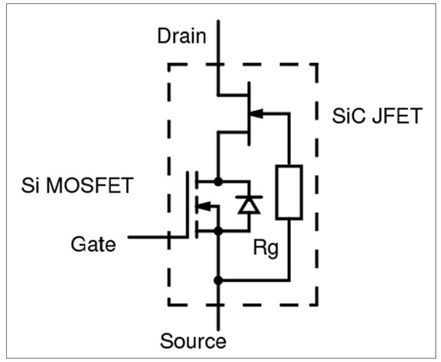


Figure 1: SiC cascode configuration

Directly replacing a silicon MOSFET with a comparable SiC MOSFET is not possible without additional revisions to the circuit, since SiC requires different gate-drive voltages. In addition, there are complications when current needs to flow in reverse, such as in hard-switched half-bridge or 'totem-pole' PFC circuits, because the SiC MOSFET body diode has a large VF of about 4 V that causes high dissipation. This could be overcome using a parallel SiC diode, which has low VF but brings space and cost implications.

As a potential direct replacement, a SiC JFET can avoid these issues but has one major disadvantage: it is a normally-ON device, whereas the silicon MOSFET is, of course, normally OFF. Normally-ON behavior has merits in an application such

as a circuit breaker, but is not preferred in power conversion.

Cascode: A Convenient Solution

Connecting a SiC JFET with a traditional silicon MOSFET as a cascode circuit can overcome this challenge at the same time as boosting efficiency, by combining the normally-OFF behavior and low-VF body diode of the silicon MOSFET with the low RDS(ON) of the WBG device. The control signal from the gate driver is applied to the gate of the MOSFET. When this a positive voltage, the MOSFET turns ON and so turns the SiC JFET ON by short-circuiting the gate to source. When the MOSFET is turned OFF, its drain voltage rises. When it reaches about +7 V, the SiC JFET gate becomes 7 V more negative than its source, which is enough to turn the JFET OFF.

Because the gate-drive signal is applied to the MOSFET, the cascode can be controlled using a standard gate driver. The voltage is non-critical, and typically can be up to ±25 V. Moreover, as a low-voltage device, the MOSFET has much lower RDS(ON) than the SiC JFET. In addition, the MOSFET body diode has fast recovery as well as low VF, and the overall combination has excellent short-circuit performance and avalanche robustness. Because most of the power is dissipated in the JFET die, the temperature capability is defined by that of the SiC technology. Theoretically, this is 250°C, although package limitations impose a practical maximum of 175-200°C.

A co-packaged MOSFET/SiC JFET cascode gives power designers a three-terminal device that combines the desirable characteristics of a high-performance silicon MOSFET with the faster switching performance, increased energy efficiency and greater temperature capability of SiC.



Figure 2: Micropower Group's Access 100 3-phase 8 kW charger

Practical Direct Replacement

SiC cascodes in standard power packages like TO-247 can directly replace silicon MOSFETs without requiring significant board redesign. Such devices are in the market now, in 650 V and 1200 V ratings, with current ratings up to 85 A.

With only minor re-optimization of external resistors, they can be controlled using standard IGBT or silicon MOSFET gate-drive circuitry. Although the faster turn-on/turn-off transition times, due to SiC technology, demand greater attention to EMI, this can be handled by controlling dV/dt and di/dt using suitable gate resistor values. On the other hand, gate drive power is significantly lower, which enhances both reliability and efficiency.

Micropower Group of Sweden has successfully designed SiC cascodes into a 3-phase, 8 kW charger (**figure 2**) for materials-handling applications, to replace standard silicon MOSFETs. The demand to redesign came about when the MOSFET supplier suddenly issued a last-time-buy notice indicating the devices were being made obsolete. With

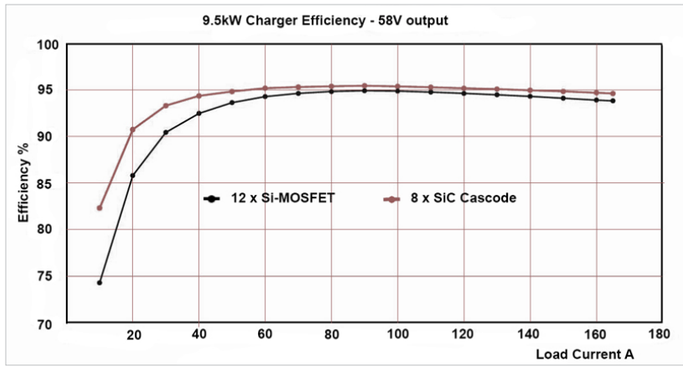


Figure 3: Efficiency improvements – SiC cascode vs Si-MOSFET

market demand for the chargers running at 7000 units per year, and no time to substantially redesign the system around new technology such as SiC MOSFETs, the engineering team sought a suitable drop-in replacement part.

The original design contains 12 silicon MOSFETs in phase-shifted full-bridge connection. Traditional planar MOSFETs were the first replacements to be considered, but their inherently lower current density would require multiple devices in parallel with a consequent increase in BOM costs. The team also evaluated super-junction transistors, although unexplained failures of prototypes undermined confidence in the robustness of the body diodes. Replacing the MOSFETs with IGBTs would prevent the chargers meeting California Energy Commission (CEC) specifications for minimum efficiency.

When evaluating SiC cascodes, Micropower's engineers found that they could use existing ±13 V gate-drive voltages, and benefit from greater than 66% reduction in $R_{DS(ON)}$ per device. In addition to adjusting the gate-drive resistor values, only a small change in driver dead-time was required. Among other minor changes, the team took the opportunity to use smaller, lower-cost snubbers, and added two Y capacitors to meet EMC standards.

Moreover, the devices – from UnitedSiC. – had 250 V higher voltage rating than the original MOSFETs and, unlike the super-junction transistors, there were no doubts about body diode ruggedness. The overall cost of the solution was no greater than that of the original MOSFET-based circuit.

Tests on the first prototypes showed an immediate efficiency improvement of 1% at operating load levels (**figure 3**). In an 8 kW application like this, such an apparently small gain represents a saving of some 750 kWh over five years of ownership. Light-load efficiency leapt by almost 10%.

Detailed analysis of switch behavior, radiated and conducted EMI, thermal cycling over 6 months, and repeated exposure (20,000 times) to voltage surges, output short-circuit/load disconnection and 'bouncing phase error' revealed no failures. The system also demonstrated a safe response to thermal stress from cooling-fan failure.

The entire project was completed within 12 months from start to production, and the redesigned chargers now deliver better performance than the superseded models at the same cost.

Conclusion: Drop-In Upgrade to WBG Advantages

SiC cascodes are ready now, to drop into existing power-conversion applications, delivering extra efficiency at no extra cost compared to IGBTs and silicon MOSFETs. Offering greater ruggedness and power density than alternatives such as planar or super-junction MOSFETs, and with flexible gate-drive requirements, they enable fast and easy access to the advantages of wide-bandgap semiconductors in high-power circuits.

United Silicon Carbide
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Ideal Package Design for Silicon Carbide & Wide-Bandgap Devices

Examining packaging trends and opportunities for power discretes & modules for power switching apps

By: Paul Koep, Alpha Assembly Solutions

The introduction of improved semiconductor devices, namely wide bandgap types such as Silicon Carbide(SiC) and Gallium Nitride(GaN) will enable significantly higher performance power switching applications, especially in applications such as automotive traction inverters.

SiC power semiconductor technology offers significant advantages over traditional silicon-based devices in power applications requiring low losses, high frequency switching and/or high temperature environments. For example, the dielectric strength voltage of SiC is about 10 times greater than that of Silicon. Low losses are critical to the performance ratio and SiC technology can reduce the power loss by up to a factor of five.

Some of the advantages of these technologies have been demonstrated and deployed, especially with Silicon Carbide in standalone charging station applications (high voltage) and more recently in traction inverter assemblies (high temperature, high switching frequency), emerging as a true "killer application" in the realm of automotive electrification.

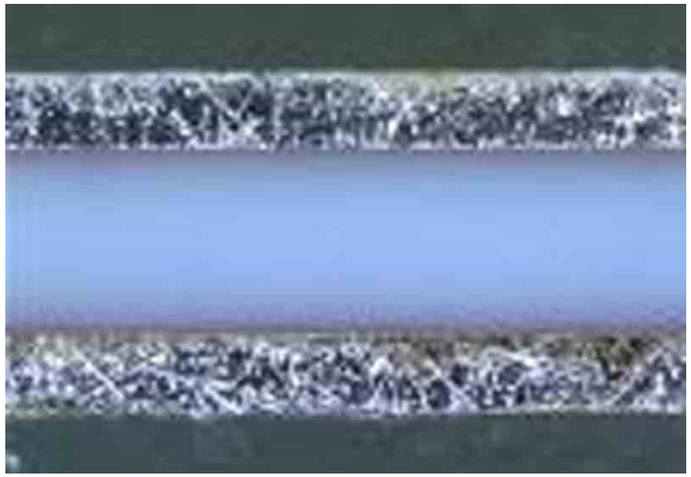


Figure 1a

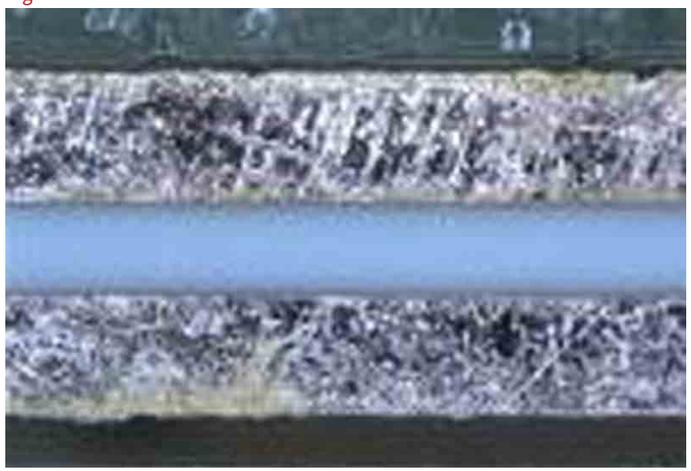


Figure 1b

Figure 1a & 1b: Variations in ceramic and copper thickness in DBC substrates

With the potential for drastically improved performance, a challenge for the industry remains. What new package innovations can be deployed to realize the full performance advantages of these promising semiconductor devices?

The first step in the evolution of improved power module package designs, even before the advent of SiC, involved the use of direct bonded copper on ceramic substrates, such as alumina and aluminum nitride to replace those made with pure copper. These ceramic substrates exhibit significantly lower coefficient of thermal expansion (CTE) characteristics, while still providing reasonable thermal conductivity.

As shown in **figure 1a** and **figure 1b**, the CTE can be modified by adjusting the thickness of the copper relative to the thickness of the inner core alumina, for example, resulting in 7-9ppm/degree C, which provides a much better match for mounting low CTE semiconductor dies. By so doing, the total CTE mismatch - die to substrate – is now 3-7ppm, rather than 13-15ppm, which is the case for a semiconductor die mounted to a copper lead-frame. The use of direct bond copper (DBC) substrates is very common in multi-die power module systems today, but copper lead-frames are also selectively used ,especially with single die devices.

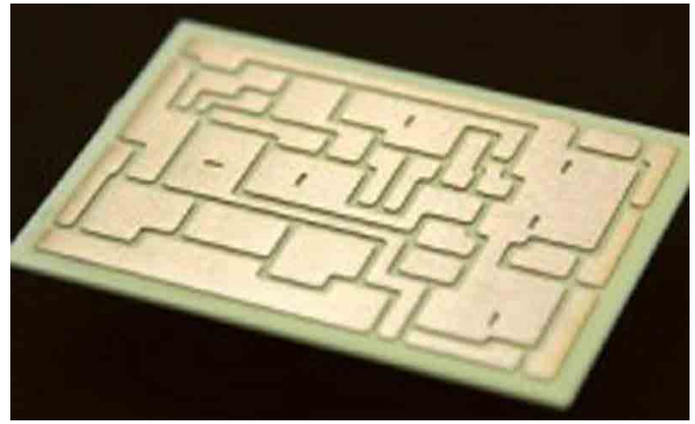


Figure 2: Etched topside direct bond copper on ceramic substrate

Another recent development is the use of aluminum as a metallization on ceramic – referred to as DBA. Vendors offering these materials claim improved thermal cycling performance compared to copper metallization.

As shown in **Figure 2**, the ceramic substrate topside metallization is etched to form a physical circuit, which can accept die attachment, followed by topside wire-bonds.

ENIG substrate finishes are also common, which provides robust surface protection prior to the die attach process, which often consists of solder reflow. Typical solders include the use of high lead for the die attach, and lower melting temperature solders deployed for the substrate bottom attach to the module heat spreader.

In the lead free arena, SnSbX alloys have found application due to their superior creep resistance and acceptable melt temperatures. Both step soldering and one step soldering processes are common, usually in a reduction environment, and sometimes with the aid of vacuum, to remove voids. Fixtures are deployed to control bondline thickness and to minimize die tilt. The use of solder preforms with built in bondline control features, such as Alpha's TrueHeight product are also used as an alternative to extensive fixturing.

These types of power modules, constructed as described here, are common for all types of high power AC motor control applications, with a good example being electric train propulsion.

In a similar manner, single die or double die packages such IGBT Diode pairs, have historically used a heavy copper leadframe, and topside wirebonds for power connections as well as control.

As shown in **Figure 3**, the aluminum bondwires can be replaced with a copper clip for improved die cooling. This configuration also



Figure 3: Aluminum wirebond topside power connections (left) and improved cooling with a copper topside clip (right)

provides improved thermal cycling performance.

As with single die packages, modules that replace the aluminum wirebonds with a more robust topside connection realize additional die cooling, greater current density, and improved power cycling. Double sided cooling of IGBT Diode modules was proposed more than 15 years ago (#1), and has found deployment in a number of automotive traction inverter assemblies used with hybrid electric vehicles. In modules that are based on DBC alumina or aluminum nitride, the topside connections are also achieved with the same materials, creating a sandwich architecture. Typical implementations, depending on topside die contact area, can result in a 30% decrease in the thermal resistance of the module.

Double sided cooling modules may need functions that can provide clearance for non- power oriented wirebonds, such as the small gate and current sense pads. In these cases, or when it is necessary to ensure a minimal air gap between substrates in higher voltage applications, spacers are used. The spacers can be constructed from thermally and electrically conductive materials, such as copper, but since the die sizes of conventional silicon can be quite large – 12mm x 12mm – there is concern about CTE mismatch when using large copper pieces connected with only a relatively thin solder bondline between the copper and the die surface. Here, the viable alternative solutions for the spacer include composite materials such as copper-moly and laminates, such as copper-invar-copper, or copper-moly-copper. The thermal conductivity of these materials is sufficiently high, and the CTE is a better match for direct die connections.

Figure 4 illustrates a cross section of a laminate material with a lower CTE compared to copper.

To ensure sufficient power cycling performance and longevity of the solder connections, the current load is distributed over numerous dies, reducing the current density per die. While this approach requires more devices for a given function, the derating is needed to ensure a robust installed product life.

As the industry transitions to Wide Bandgap devices, such as SiC, the packaging of these devices will be a critical factor influencing the reliability, performance and cost of new modules. SiC is more efficient at higher operating temperatures, and the ideal package design should support this fact to enable the improved die efficiency.

One of the most promising attachment materials being deployed with both silicon and SiC is sintered silver.

As **Chart 1 illustrates**, silver is a nearly ideal attachment material,

		Melting Point	Thermal Conductivity	Electrical Resistivity
Material	**Composition**	**°C**	**W/m°K**	**µOhm-cm**
Silver	100Ag	962	419	1.6
High Lead	92.5Pb / 2.5Ag / 5Sn	287-296	26	17
SAC305	96.5Sn / 3Ag / 0.5Cu	217-228	55	14.5
Gold - Tin	80Au / 20Sn	280	57	16
Sintered Argomax® Ag w/ density 85%		962	200-300	2.5-3.5

Chart 1 – Die Attach Material Properties

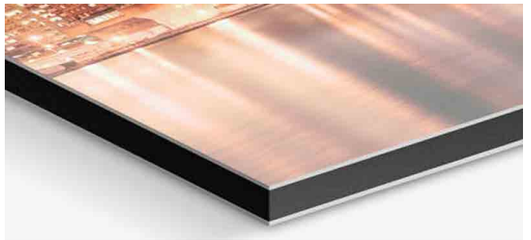


Figure 4: Copper-Moly-Copper laminate

but its melting point makes it prohibitive to use as a reflowed metal. Nonetheless, it has very high thermal conductivity, and exhibits attractively low electrical resistivity. All of these features are superior to solder, including power cycling capability, as will be discussed later.

The key to sintered silver is the use of nano particles which fuse at a temperature similar to solder reflow, when aided by modest pressure. Once sintered to a density of ~85%, a thermal conductivity of 200-300 W/mK is achieved. In addition, the interfacial losses are extremely low since the nano Ag also sinters to die and substrate metallization.

One study of note (#2) highlights the significant performance advantage that sintered silver die attach materials can provide for power devices. A comparison was done between a soldered and topside wirebond silicon die pair consisting of an IGBT – Diode (TO247 package) and a similar package and die combination that was constructed using a double sided sintered implementation. The sintered package was capable of switching 200A, compared to the soldered device, which was rated to 130A. Power cycling yielded a 15 X improvement with sintering, and the sintered package was still operational after 150k cycles of 15s on, 15s off with a delta Tj of 100C.

This type of performance and durability can have an immediate impact on existing silicon die implementations as well as setting the stage for the greater use of SiC technology. In addition, sintered silver can support significantly higher die operating temperatures of SiC, since the sintered silver is stable up to the melting point of Ag, which is 962 degrees C.

Another significant advantage of SiC technology is the much smaller die sizes required compared to silicon when switching the same currents.

As the different types of high volume production applications for sintered silver have grown, so have the material types. While the initial sintered silver applications relied on silver nano paste, film as well as preforms have emerged as viable product types, which have enabled new manufacturing processes. Wafer level lamination is now viable with nano silver film. Once the wafer is laminated, the wafer can be diced with standard equipment. An alternative process has also been developed that can laminate individual dies from the wafer and immediately sinter them on a target substrate. This is referred to as the Die Transfer Film process. The advantage of DTF is that only known good die are laminated and sintered, which can provide significant advantages when being used with SiC, which may have yield issues in the start-up phase of new wafer fabrication lines.

Summary

The use of materials such as DBC alumina and DBA alumina and well as double sided cooling enabled with top and bottom substrate are being deployed to advantage in power module designs. In order to realize the full advantages of Silicon Carbide technology, new die attach materials such as sintered silver are being deployed, enabling higher operating temperatures, increased current densities and enabling significantly extended power cycling performance. These advances will yield smaller, lighter, more robust power inverter designs for the new generation of traction inverter products for automotive and other uses.

Alpha Assembly Solutions
www.Alphaassembly.com

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Benefits of GaN in Power Electronics

Reducing cost, size, and weight, while increasing efficiency and reliability

By: Peter Di Maso, Director, Product Line Management at GaN Systems

The pursuit of higher efficiency has been a driving factor in industry progress since electricity was first harnessed. The introduction of solid state transistors in switching applications enabled the switching power converter and created a step function improvement in power conversion efficiency. Advances in switching power transistors has helped improve efficiency and reliability and reduce size and cost in power electronics applications. Wide Band Gap semiconductors, specifically GaN (gallium nitride) power transistors, are currently leading the drive to higher efficiency.

The markets and applications that benefit from GaN E-HEMTs (enhancement mode high electron mobility transistors), and therefore drive it, are comprehensive. Data center, industrial automation, wireless power transfer and charging, and renewable energy and transportation applications have benefited with the use of GaN specifically with 1/4th the power loss, 1/4th the size/weight, and substantially lower system budgets as compared to silicon-based systems. Before we discuss how GaN E-HEMTs add value to the key applications in these markets, let's review how GaN E-HEMTs work.

Introduction to GaN: similarities and differences to MOSFETs

GaN E-HEMTs are conceptually similar to silicon MOSFETs. GaN E-HEMTs are three terminal devices with gate, drain, and source nodes. Similar to MOSFETs, a positive voltage between gate and source on the E-HEMTs enables high electron mobility path between the drain and source terminals (see **figure 1**). When the gate is held at or below source potential, the high electron mobility path is interrupted and no current flows between drain and source. This is true only for enhancement mode devices. GaN power transistors using depletion mode devices typically in a cascode configuration are not considered here. The complexity of cascode implementation of GaN transistors, essentially multichip modules, has limited the market acceptance of this type of product.

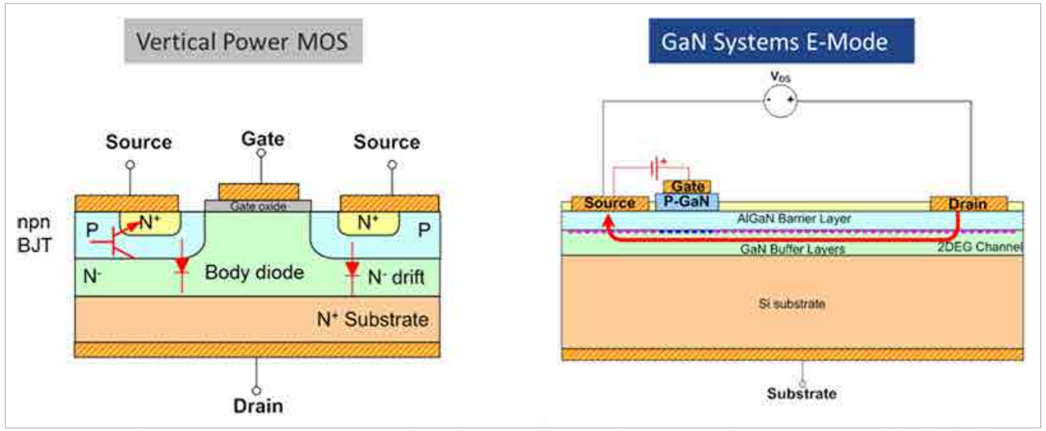


Figure 1: Similar to MOSFETs, a positive voltage between gate and source on the E-HEMTs enables high electron mobility path between the drain and source terminals.

The rated voltage, typically 650 V or 100 V, is the minimum voltage transistors will block or hold off. The repetitive avalanche characteristics of silicon MOSFETs is not as easily characterized in GaN E-HEMTs, however the characterized breakdown voltage of GaN E-HEMTs has shown them to be resilient to transient voltages.

Although there are many similarities, there are some key differences between GaN E-HEMTs and MOSFETs. Silicon MOSFETs are vertical devices meaning the drain to source current flows from the top (source) of the silicon die through the MOSFET channel to the drain substrate on the bottom. GaN E-HEMTs, on the other hand, are lateral devices so the drain to source current flows into the drain terminal on the top of the device, through the high mobility channel to the source terminal, also on the top of the device.

GaN power transistors are manufactured by growing layers of GaN and AlGaN (aluminum GaN) on silicon substrates – the same as standard Si MOSFETs used in high volume. The hetero-interface between GaN and AlGaN forms a two-dimensional electron gas (2DEG) and is the basis for a high mobility channel. The 2DEG formed has very high charge density and mobility which results in very low drain to source resistance, RDS(on), and very high-speed devices. The 2DEG is a native characteristic of the GaN-AlGaN interface so the gate of device must provide a method to interrupt the channel for use in power converter applications. This accomplished by creating a P-type GaN interface that depletes a 2DEG channel underneath the gate. This produces the normally off e-mode transistor, controlled with a positive gate bias turn on the 2DEG.

Switching Characteristics

The GaN E-HEMT structure has the added feature over Si MOSFET of having no body diode or parasitic bipolar junction transistor. The benefits in switching power applications is that there is no reverse recovery body diode loss and high and has voltage slew rate ruggedness, which are traditional weaknesses in Si MOSFETs.

The switching loss analysis of GaN E-EHEMTs is again similar to the analysis for MOSFETs. The main switching loss mechanism is set by the device capacitances and gate charge values. Since the values of gate charge and node capacitance are much smaller than MOSFETs, GaN E-HEMTs losses are significantly reduced. The input, output, and reverse capacitance of GaN deliver low-loss turn on and fast transitions resulting in no loss in dv/dt (Miller plateau) period during turn on. Effectively GaN E-HEMTs are similar to MOSFETs with much faster, more efficient switching, and reduced conduction losses.

Packaging & Layout

With the fast transition speed, high frequency ability, and high current capability comes the responsibility to use GaN power transistors effectively. Traditional plastic packaging for high power semiconductors like TO-247 and TO-220 are bulky and add significant resistance and inductance to the transistor die. Smaller transistor packages, like TO-263 or DFN packages have helped to reduce extrinsic transistor impedances but are effectively restricted to lower power application due to size and lead frame requirements. To get the best possible performance, GaN E-HEMT packages require extremely low inductance, small size, low inductance pin to die connections, and low thermal resistance, RθJC. GaN Systems uses GaNPX® package material, a high temperature epoxy-based PCB material that is similar to FR4 with a higher temperature rating. This embedded packaging technology allows the electrical connections to be made with the platter copper pillars and vias and no wire bonds, minimizing resistance and inductance. The thermal connection to the substrate also utilizes copper

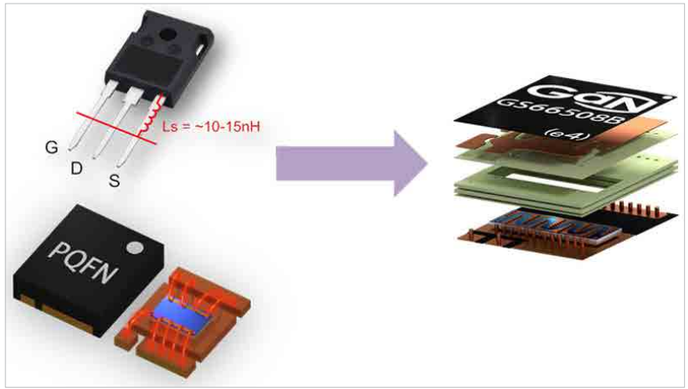


Figure 2: The thermal connection to the substrate also utilizes copper connections to make a very low thermal resistance between the transistor substrate and GaNPX® thermal pad.

connections to make a very low thermal resistance between the transistor substrate and GaNPX® thermal pad (see **figure 2**). The low inductance, low thermal impedance, small footprint package also improves system performance by enabling low impedance external connections to the GaN E-HEMT. The lower overall inductance and resistance can accommodate high slew rates and maintain with lo VDS overshoot and lower electromagnetic interference.

Improved System Performance with New and Enhanced Topologies

Power factor correction (PFC) circuits have conventionally been built with front end bridge rectifiers to begin the power conversion process of turning AC power into DC power and forcing the current to follow the AC line voltage. Eliminating the front-end rectifier losses is possible by implementing a bridgeless totem pole circuit (BTP) (see **Figure 3**). The BTP PFC topology uses switching transistors and attains much lower losses than a bridge rectifier implementation. Before GaN power transistors were available, silicon MOSFETs were the only choice for BTP configurations. Implementing BTP with MOSFETs saw only a slight improvement because reverse recovery losses of the high side synchronous MOSFET of the boost circuit all but erased the gains of removing the bridge rectifier. With no parasitic body diodes and the reverse conduction capabilities of GaN E-HEMTS, the reverse recovery losses in BTP PFC are eliminated and the true value of topology is realized. Increased efficiencies from 97.5% to 99% have been attained. With the lower losses, higher frequency and reduced part count, smaller, less expensive, cooler, and more reliable front-end PFC have been realized for applications needing PFC.

The most popular topology for isolated DC-DC converters is the LLC half-bridge that achieves

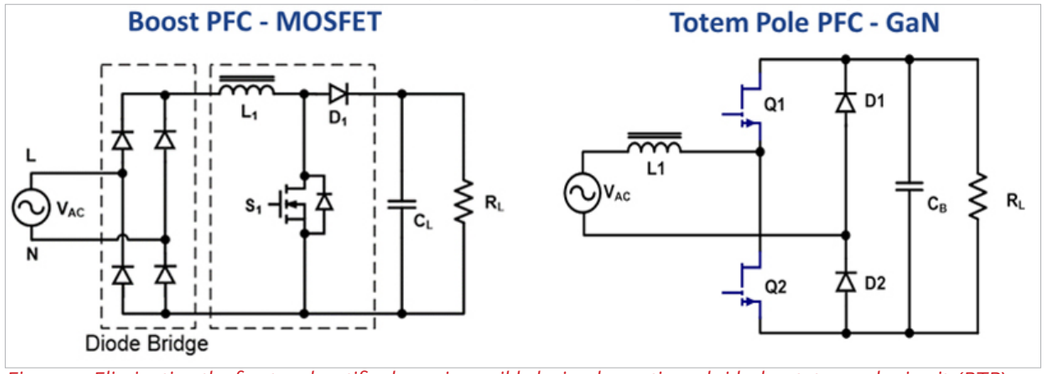
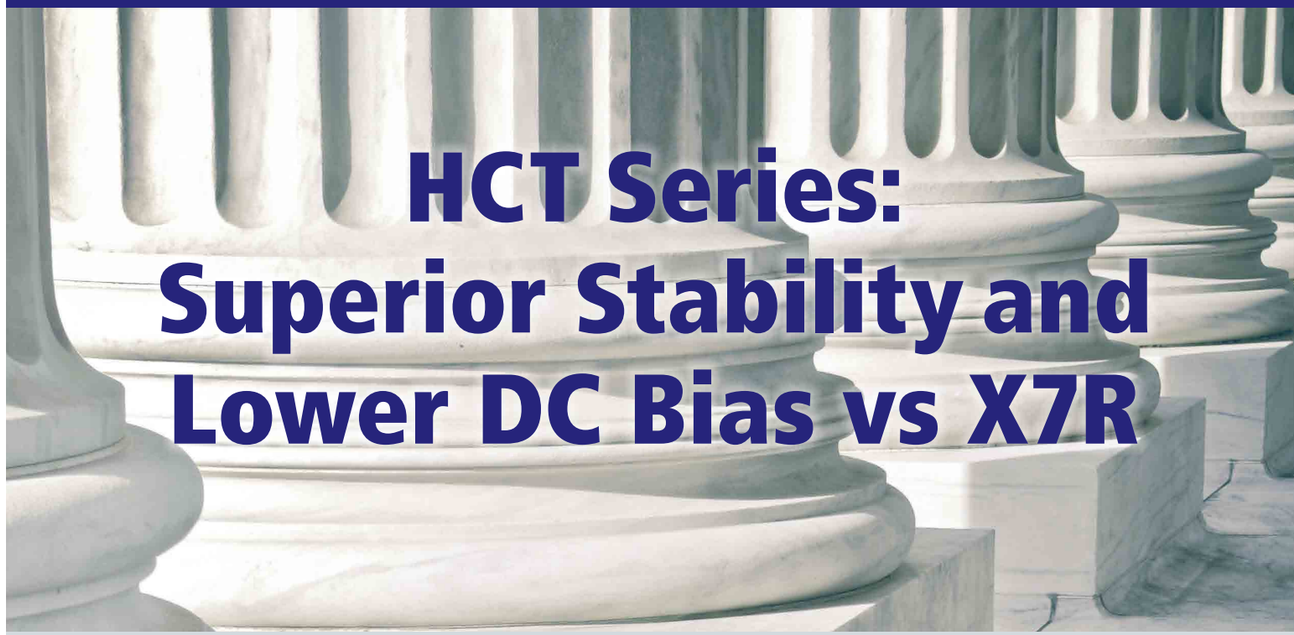


Figure 3: Eliminating the front-end rectifier losses is possible by implementing a bridgeless totem pole circuit (BTP).

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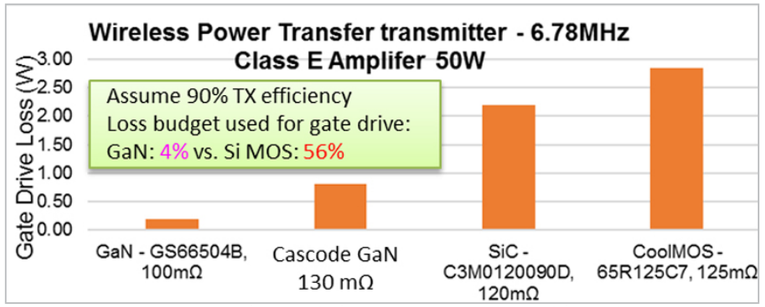


Figure 4: 50W, 6.78 MHz Class E wireless power transmitter with 90% target transmit efficiency would use 56% of its power loss budget to drive MOSFETs compared to only 4% when using GaN E-HEMTs

zero voltage switching (ZVS). It is widely used in power levels from 75 W to 750 W because it achieves high efficiency through resonant switching and elegant magnetic design. This topology has been extensively used for the last twenty years using standard Si MOSFET technology. GaN power transistors, with their very low output capacitance (COSS) and high switching frequency capabilities are further enhancing the value LLC. Sufficient dead time is required in LLC converters to achieve ZVS and reap the benefits of the topology. The dead time is a function of the value of the magnetizing inductance of the converter's transformer, the COSS of the switching transistors and the switching frequency, as shown in **equation 1**:

$$T_{dead} \geq 16 \times C_{oss(ER)} \times f_{sw} \times L_m \quad (1)$$

The significantly smaller COSS of the GaN E-HEMTs compared to silicon transistors allows for larger magnetizing inductance which equates to lower transformer losses. This also lowers the rms current through the half-bridge power switches and thus reduces conduction losses. The smaller COSS also allows for a higher switching frequency, smaller resonant tank, and therefore provides higher power density. Compared to Si MOSFETs, GaN E-HEMTs can reduce gate drive loses by a factor of 50 times (from 2.8 W to 50 mW) in a 200W LLC converter operating at 1 MHz – increasing efficiency by 1.5% by reducing gate drive losses in addition to lowering the losses in the LLC commutation circuit.

GaN Enabling New Applications

Wireless power transfer with spatial freedom and high power levels has been enabled by GaN E-HEMTs due to high frequency and high efficiency. Low gate charge, QG, is key to achieving high efficiency as switching frequencies increase. As an example, a 50W, 6.78 MHz Class E wireless power transmitter with 90% target transmit efficiency would use 56% of its power loss budget to drive MOSFETs compared to only 4% when using GaN E-HEMTs (**figure 4**).

GaNPX® packaging technology and GaN design and manufacturing know-how, produce the lowest $R_{DS(on)}$, lowest gate charge, lowest capacitance and lowest parasitics portfolio of enhancement mode GaN HEMTs for 650 V and 100 V applications.

Conclusion

GaN E-HEMT transistors have become mainstream in power electronics design. They enable and enhance topologies like BTP PFC and LLC. GaN E-HEMTs have made wireless power transfer and charging functional reality. The lower parasitics and thermal stress, and ease of use have created widespread adoption of GaN technology. Higher efficiency and higher density in datacenter, industrial automation, renewable energy, and automotive applications are highly valued. The benefits of GaN collectively lower system, shipping, installation, maintenance, and operating costs.

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In-House Processing Brings Cost-Effective AI

By: Ally Winning, European Editor, PSD

Earlier this year I wrote a blog on Google and its tensor processing units. The company had just launched the second generation of its powerful ICs that provide the computing power for its vast datacentres around the world. The processors are specifically designed for the complex AI computational tasks found in the cloud and can be trained to perform specific tasks. Having its own bespoke processing elements gives Google a competitive advantage over other companies who have to use off-the-shelf processors from companies, such as the current market leader Nvidia.

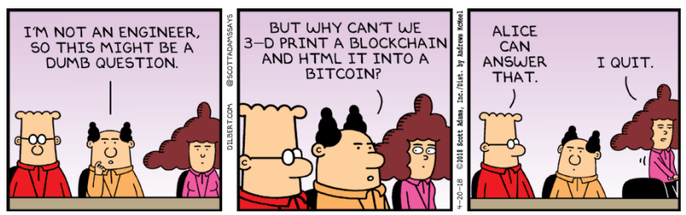
Now it seems other AI and cloud companies with heavy processing needs are looking to take a similar route to try and efficiently gain market share in the nascent market. Initially Facebook had been working with Intel on a new chip, but now the social media giant has begun advertising for ASIC designers, presumably to work in-house on an AI processor for the company's own datacentres. Then Chinese corporation AliBaba, which is currently better known for providing e-commerce solutions than cloud ones, followed that by employing former Qualcomm silicon designer Liang Han as an AI chip architect and then placing recruitment adverts for a team based in Silicon Valley to work with Han. The company confirmed that it was working on a neural networking processor, the Ali-NPU, that it hoped would be almost 40 times more cost-effective than off-the-shelf components.

Alibaba made further moves toward its new processor by buying fellow Chinese company C-Sky Microsystems this month. C-Sky is a developer of proprietary 32-bit CPU cores and makes the claim that it is the only high-volume CPU provider in China with its own instruction set. As well as designing its own processors, the company is a platinum member of the RISC-V foundation, which could allow it to easily expand into 64-bit cores or even complete neural networking devices. Alibaba is currently quite a small player in the global cloud market, but there is no doubt that it sees it as a huge potential growth area. Having its own processor would allow it to scale its operations up much more cost-effectively than through buying from chip manufacturers. It would also provide an easier supply chain to manage. With China's protected internal marketplace, Alibaba could scale up pretty quickly as Huawei and ZWE have done in the mobile telecoms market.

Other giant corporations are also working on AI processing. These companies include Apple, Microsoft and Tesla. Although not initially for datacentres, the experience of designing a low-power processor for a car, phone or headset would be an ideal beginning to expand into data centre processing. At the start of the computing age, companies built a chip and looked for a market. Now, in the information age, it seems the companies have built the market and now are looking for a chip.

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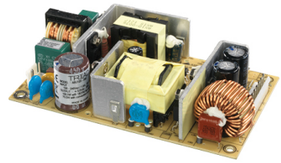


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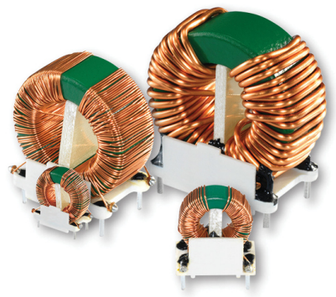
stray inductance to suppress differential mode noise. In effect, the CMF combines the features of two separate components into one.

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- Rated Current: 0.45 to 2.3 A
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- Resistance: 279 to 1970 mOhms
- Stray Inductance: 200 to 2100 mH

For info or to purchase, go to:
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CMT Common Mode Inductors

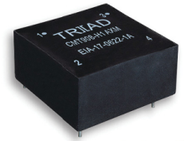


Triad's CMT Series Common Mode Inductors provide common mode EMI suppression for power supplies. They feature our precision coil windings to eliminate noise and to minimize the AC line transmitted interference often created by high frequency switching power supplies. They also meet various regulatory requirements and are constructed with UL rated 130°C materials.

KEY SPECIFICATIONS

- Min inductance: 1 to 50 mH
- Max current: 1.7 to 20 A
- Max DCR: 0.006 to 0.45 ohm

CMT908 Encapsulated Common Mode Inductor

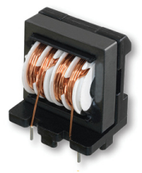


Triad's CMT908 Series Common Mode Inductor features a sealed encapsulated design that is ideal for rugged environments and where reliability is critical. It provides superior common mode EMI noise suppression for power supplies and other power devices.

KEY SPECIFICATIONS

- Min. Inductance: 2.0 to 16 mH
- RMS Current: 2.60 to 7.50 A
- Max DCR: 0.020 to 0.160 Ohm
- Minimum Leakage: 25.0 to 180.0 uH

UT/ET Common Mode Inductors



Triad's UT/ET Series Common Mode Inductors help prevent EMI/RFI in a wide range of applications. Features include low leakage flux, high self-resonant frequency, high impedance at applicable frequency and low stray capacitance in section winding. Precision coil winding ensures excellent performance and reliability

APPLICATIONS

- Min. Inductance: 0.45 to 120 mH
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ANALOG DEVICES

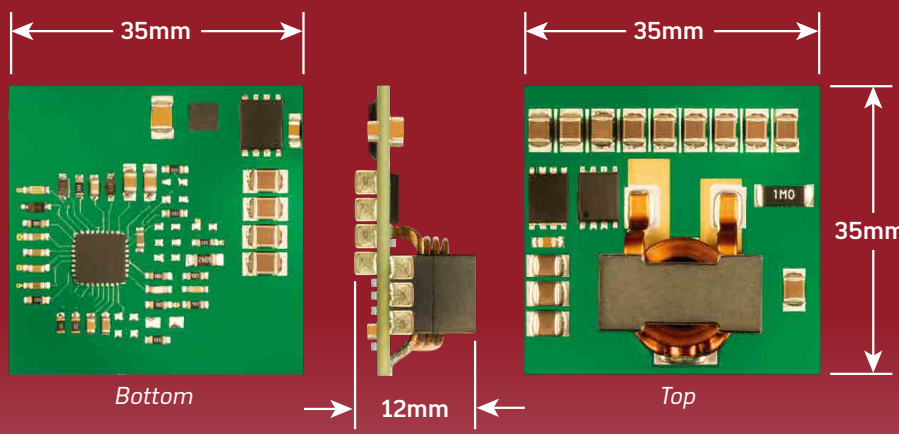
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